Course name- Analog VLSI Design (108104193)
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Institute – Indian Institute of Technology Kanpur
Week- 11
Lecture- 31, Module-1

We will come back, this is lecture 31. So in the previous lecture, we were in the last couple of lectures we were discussing differential amplifier and we are analyzing the structure and today we will continue the same with some more modifications. So this was the structure. So here we were taking the output and we assume that M1 and M2 are identical for our calculations. And I mean, you need not assume that this did not necessarily be the case all the time and we saw if that if M1 and M2 are not identical how to deal with it in the previous lecture. So the stuff that we did not, we have not assumed till now is or the stuff that is that might bother some of you is the fact that we have this ideal current source which is connected to this tail node.

Now the problem here is, I mean we all know that nothing is ideal, the current source will also have a output impedance associated with it. Note that till now we have assumed that incrementally because the current source is ideal, incrementally looking down it is an open circle into the current source. But if current source is not ideal then what happens? That is what we will see in this lecture. So by the way when we say that you have a non-ideal current source what do we essentially mean? We essentially say mean that how do we get this current source? So this is what type of biasing do you think is this? This clearly is similar to the biasing where we, this is similar to the structure where we bias the NMOS with the current source with the source terminal.

Remember this where this was V bias. So this you can assume this I0 to be split into I0 over 2 and I0 over 2 and each I0 over 2. So what I am essentially saying is you can think of this I0 as I0 over 2 and I0 over 2 in parallel and each and since the current is equally split between the two branches, so essentially there is no current to this short and we can assume that each of the transistors M1 and M2 are biased using constant current source, right, connected at their source terminal, right. So the reason I am saying is I want to draw the analogy of what did we do when we replace this current source? We essentially said that maybe we have a current source whose which I will, a master current source which I will use to copy the current and feed it to wherever is necessary, right. So in this structure the impedance looking down would have been rds.

I mean under the condition that rds is infinity then the MOSFET here is like a current source but in general we cannot assume that, right. Because as we said you cannot

assume something to be infinite when in fact the output impedance is finite, okay. So we will have to deal with this in this context and how do we deal with this? We essentially say that so maybe we have a current source somewhere and the current source is copied using a current mirror, right. And let us call this M0 and this is I0. So ideally this current will be I0.

Now we know that if we, this will be exactly equal to I0 if we neglect channel length modulation. If we do not neglect channel length modulation this will be something different from I0 because we, it is not necessary that the drain voltage of the transistor on the left will be equal to the drain voltage on the transistor on the right. So there can be some mismatch. But for the purpose of our analysis let us assume that the mismatch is not large enough and let us say that the quiescent current is still finite, okay. Okay fine.

So how do I go about analyzing this structure? So let us move into the small signal domain, right, so that analysis of the structure will become more apparent. Okay. So what do I replace this transistor with, the left transistor with in the incremental domain? So clearly the current source that we had here goes off because we are analyzing everything in the incremental domain. So incrementally what is the impedance looking into the gate of this diode connected transistor? It is 1 over gm to ground. So essentially we can replace this also.
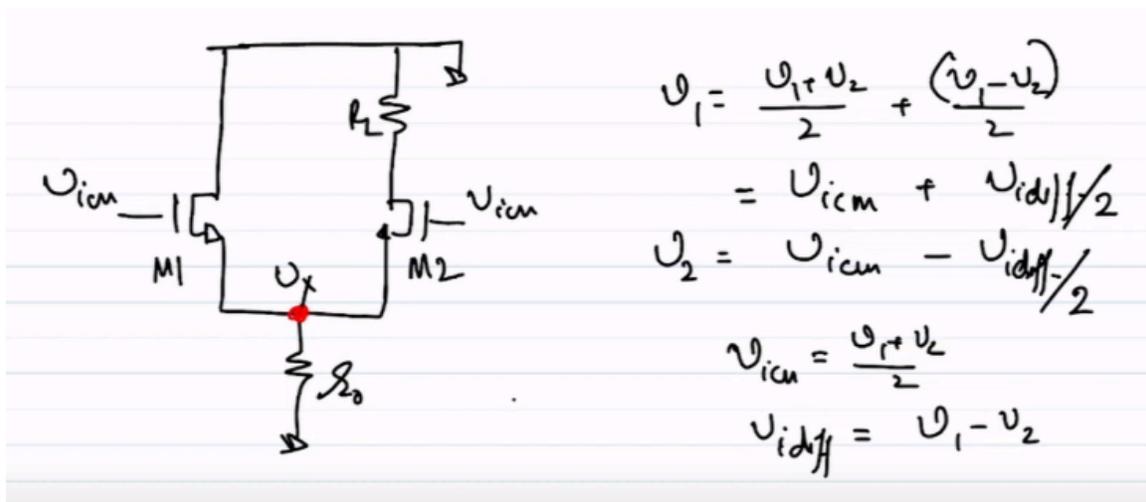
This also becomes 1 over gm to ground, correct, 1 over gm of that transistor. But I mean then what is the voltage here? What is the Vgs, incremental Vgs of M0? The incremental Vgs of M0 clearly is 0, right. So if the incremental Vgs of M0 is 0, the gm Vgs term goes to 0. However, there is a gds, right, there is a gds associated with it. So let me sketch it fully, probably that will make more sense.

So we have a gds and we have a gm Vgs, right. And if this is gate, this is source, right. What is Vgs? Vgs is 0. Since Vgs is 0, this goes off, only the gds remains, right. So what we will do, I will remove all this stuff and I will only let the incremental resistance rds is 0 or let me drop even the rds subscript because it might be messy going forward.

Let me just only say r0, right. And this is what the structure boils down to incrementally, right. And let us go ahead and do the analysis, okay. So if we do the analysis of this, now the question is, how do we go about doing an analysis? So let us do some assumptions. What assumptions will you do? Let us say that since we know that V1 and V2 can be broken down, right, into common mode and differential modes, right.

So let us say V1, we know that V1 equal to V1 plus V2 by 2 plus V1 minus V2 by 2, which means that I can express the first term as some V input common mode plus V

input differential mode, right. So we can also express V2 as V input common mode plus or minus V input differential mode, okay, fine. So sometimes you will see that in the literature, the differential mode, the differential signal is only referred to as V1 minus V2, right. If we have to follow the same convention, we have to then say that this is differential by 2, right. So what I am essentially saying is that VICM, by definition, if we say VICM equal to V1 plus V2 by 2, then V diff, V input diff is V1 minus V2 by 2, sorry, V1 minus V2, right.

$$v_1 = \frac{v_1 + v_2}{2} + \frac{(v_1 - v_2)}{2}$$

$$= v_{icm} + v_{id}|/2$$

$$v_2 = v_{icm} - v_{idf}/2$$

$$v_{icm} = \frac{v_1 + v_2}{2}$$

$$v_{idff} = v_1 - v_2$$

So this is a matter of definition. We just have to keep track of where the factor of 2 comes and where it does not, okay. So why are we doing this? We are doing this because ultimately, because the structure seems to be symmetric, right, because M1 and M2 are identical, we will apply V input common mode once and then we will apply V input differential again, right, and then do the analysis and then combine them to find out the final answer, okay. Okay, so let us do this. So if this is what it is, what do you think will be the incremental current through M1 and M2? So if we have to find out the incremental current through M1 and M2, what do I need? I need to find out the incremental voltage at this node, at the tail node, let us call this Vx, okay.

Okay, so what will be the incremental voltage at the tail node? Again we can use superposition, right. So let us use superposition for now, then you will see that we can play some more trick also, right. So if we use superposition and we say that we will only have, let us put a different page. If we use superposition, let us incrementally ground this guy, right, and what are we looking for? We are looking for the incremental short circuit output current, okay. We are looking for ISC, short circuit output current.

Note that this is in the incremental domain, even though I have not replaced the

transistors physically at the back of your mind, you should remember that we are doing the analysis of an incremental picture, okay. So if in this case, what do you think, how should we go about analyzing this? We have done this before, what is the impedance looking in here? Impedance looking in here is 1 over gm, right. What is the impedance looking here? Impedance looking down is R0. So what does M1 see? So if I sketch the condition on M1 separately, so what is M1 seeing? M1 is seeing an impedance of 1 over gm and an impedance of R0, correct? And this node here is Vx, okay, okay, fine. So if this is Vi is here, then what is Vx? So note that the parallel combination of 1 over gm and R0 is almost equal to 1 over gm, right? So this is almost equivalent to saying that if we are interested in the node voltage of Vx, then we can say that this is almost equal to this.

So what is Vx? We have done it in the previous lecture. What is Vx? Vx is Vicm over 2, right? So if Vx is Vicm over 2, what is the incremental current? incremental current is gm of M1, this is gm M1 times Vicm minus Vicm over 2, which is gm 1 times Vicm over 2, right? Okay? But there is a slight catch here. Okay, before we come to the catch, let us go back and put these values here, right? So what is this voltage? This voltage becomes Vicm over 2, right? Okay. So now, if this voltage is Vicm over 2, what do you think is the current that is flowing into R0? What do you think is the current that is flowing into R0? So this current will be Vicm over 2 R0, correct? Okay, so you might wonder that where from did this Vicm over 2 R0 come into being suddenly, right? Right? So this guy, where from did it come? It came because the voltage at the Vx at the tail node is moving because the voltage at the tail node is moving and there is a resistance attached between the tail and the ground that resistance will take up some current. It is not an ideal current source anymore.

But where did I, I mean, suddenly how did I come up with this structure? I mean, in one place I said that I will neglect this and then I will find out what is the current and then at the next, I mean, couple of minutes later, I say that I will not neglect the current. So what is it that is happening? So note that the approximation that I made here is the current that is coming from this transistor, right, current that is coming from M1, right, is being determined by whatever is getting load, whatever is loaded at the source, okay? So what is loaded at the source? Thus, thus loading at the source is approximately equal to or not approximately is equal to parallel combination of R0 and 1 over gm, which means that it is almost equal to 1 over gm, which means the total current that will come through the transistor will be function of will be approximately equal to whatever we got, the gm1 dicm by 2. But note that this is an approximation because we had neglected the loading due to R0, right? So this is an approximation without considering the effect of R0. But this approximation is not a bad approximation because now we are neglecting a small amount with respect to this current, okay? But when we are trying to find out the

actual current through R0, then we are trying to figure out that small amount. So since we are trying to figure out the small amount, we cannot know any more neglect the current through R0, okay? So what is the, I mean one way to do, one way to go about doing this is putting everything together to a brute force analysis.

$$U_{xp} = U_{icm}/2.$$
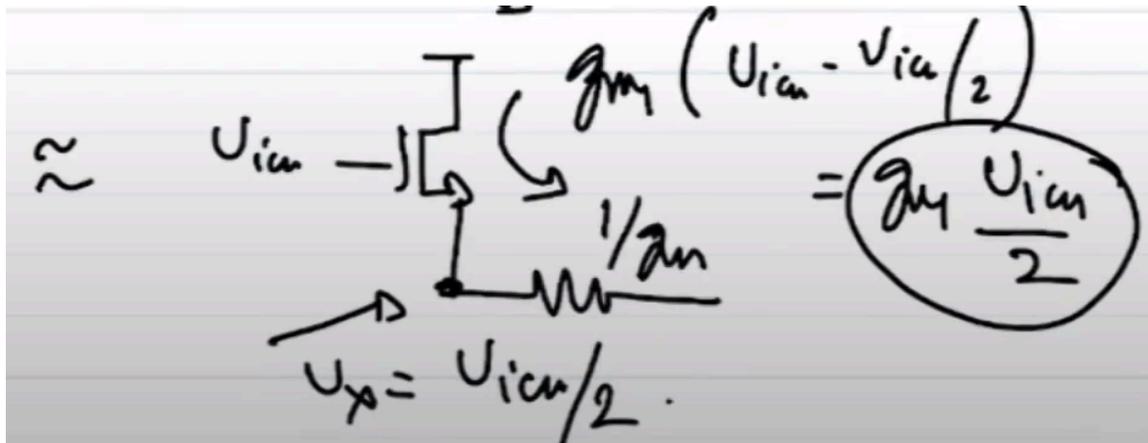
It is not very difficult in this case, but what I am trying to point out here is that there is a simpler way of going about doing this analysis as long as we know which transistor, which register is the dominant loading factor, right? And that is what we are doing here, right? So in order to establish that, what we essentially said, the voltage at the tail node is being set by the dominant loading term and the dominant loading term is 1 over gm. Now that voltage at this node is set, then we will be using that information in order to find out what is the current through R0, right? That is what we are doing. So granted that there will be a difference in the actual amount of current, right? That we, that is for sure, but whether the difference is significant or not, that we will have to, that we have to see, okay? Okay, so let us go ahead with this. So what is the current going into M2? The current going into M2 is, this is approximately gm1 Vicm by 2 in the direction flowing upwards, right? And the current going down is Vicm by 2 R0, okay? So one might say then that the current through this transistor is Vicm by 2 R0 plus gm Vicm by 2, right? So essentially, this essentially means that this current is Vicm by 2 R0 plus gm Vicm by 2, correct? Basically KCL at that node, okay? Okay fine. So what is Isc or let me say Isc1 this case.

The Isc1 essentially is the current, this current which is gm Vicm by 2 and this is Isc due to what? Due to only when the input is applied at M1. So what we will do, we will try to see what happens when input is applied at M2 and we will short this, right? So what will be Isc2? What will be Isc2? Note that it will, I mean we can do the same analysis as we
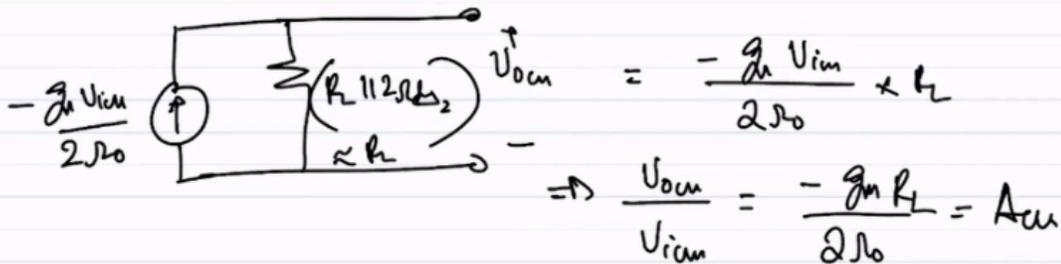
did and what will we come up with? We will come up with the fact that this current will be equal to Vicm by 2 R0 plus gm Vicm by 2, this voltage will be Vicm by 2 and this
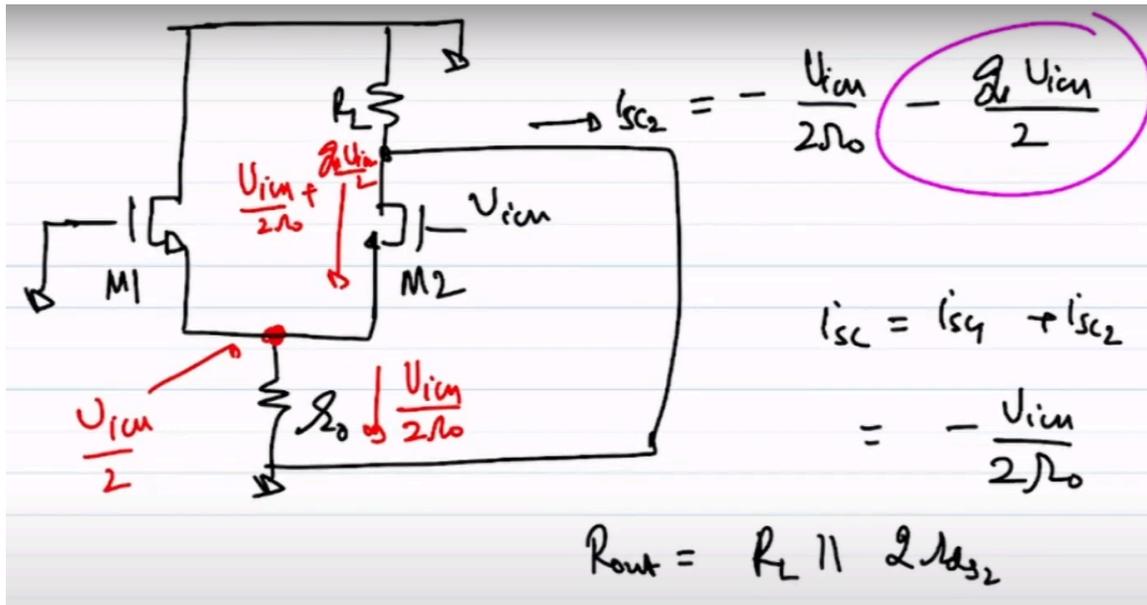
current will be Vicm by 1. Make sense? Essentially this analysis is same but done for different transistor, correct? So what is Isc2? Isc2 in this case is what? So let me go back to the previous one. So in this case Isc1 is gm Vicm by 2. In this case Isc2 is, because the direction is in the opposite direction, arrow is pointing in the opposite direction to the current flow, so it will be minus Vicm by 2 R0 minus gm Vicm by 2.

So what is Isc then? Combined Isc is Isc1 plus Isc2 which is essentially this term and this term cancels off and we are left with only one term which is minus Vicm by 1, right? And in order to find the R out we have to do the same thing as we did earlier and so we basically borrow the same expression and what was R out? R out was RL parallel, RL parallel the resistance looking into the drain of M2. What was the resistance looking into the drain of M2? It was twice rds of 1, 1 or 2, right? So in this case I can simply write 2 rds2, correct? So what is the gain? What is the Norton's equivalent? The Norton's equivalent for a common mode excitation is, so Norton's equivalent common mode excitation is what? It becomes, so this is minus gm Vicm by 2 R0 and this is RL parallel 2 rds, correct? So this becomes the Norton's equivalent. What is the output voltage then? What is the output voltage? Output voltage becomes minus gm Vicm by 2 R0 times RL, right? Because this is approximately equal to RL because generally rds is much higher, right? Than RL, okay? So what is the common mode gain? So I should also say this is probably Vicm because we are talking about common modes, right? The common mode inputs, the common mode output becomes Vicm by Vicm becomes minus gm by 2 R0 times RL, okay? Fine. So this becomes the common mode gain. This is the common mode gain of the structure, okay?

Norton's equivalent for common mode excitation

$$V_{ocm} = -\frac{g_m V_{icm}}{2R_0} \times R_L$$

current source: $-\frac{g_m V_{icm}}{2R_0}$; resistor: $R_L \| 2R_{ds_2} \approx R_L$

$$\Rightarrow \frac{V_{ocm}}{V_{icm}} = -\frac{g_m R_L}{2R_0} = A_{cm}$$

But this is not all, we will have to also find out what is the differential mode gain, right? So, for that we will have to apply a differential signal.

Let us apply differential signal, let us say this is V diff, this is minus V diff and we do the same analysis, we have to find out isc. In order to find out isc what can we do? We can again break it down into V diff, I mean one input at a time. So if we do that what we see, note that we will see something very interesting. So let us do that. So let us apply only at input at M1 and ground M2 and let us call this isc1, right? So for this, the analysis is exactly similar to the common mode case, right? We were doing part by part.

What is Vx? Vx will be V diff over 2, correct? What will be this current? What will be this current? This current will be Vx over R0 which is V diff by 2R, right? What will be this current? What will be isc1? Isc1 will be what? Isc1 will be equal to gm times V diff over 2, okay? Fine? Okay. So let us now go ahead and apply the other input, right? So what is the other input? If I apply the other input, so that is V, let us apply isc2 or rather let us try to find out isc2 while applying input at this end which is minus V diff. Let us say this is grounded, right? So this is when input at M1. So when input is applied at M2, what should we see? We should see Vx to be equal to V diff minus V diff over 2, right? So when you see input to be equal to minus V diff over 2, let us pause here for a second and apply superposition on the node Vx, okay? So if this is indeed the case, so using superposition, so in this case, where will the incremental current flow? So in this case, the incremental current flow will be upstairs going upwards and it will be V diff over 2 or not flowing, yeah V diff over 2 or not flowing upwards. In the earlier case, when it was applied at M1, when input was applied at M1, the current going down was V diff over 2 or not going down, right? Okay, let me color code this also, okay? So this is, okay, so if that is the case, what is the incremental current that is flowing in through R0 using superposition? Using superposition, what is Vx? Vx will be V diff over 2 minus V diff over 2 which is 0, correct? So Vx will become 0.

If Vx becomes 0, right, in the presence of both the inputs, right, so let us apply both the inputs. This is V diff, the other one is minus V diff, okay? So diff by 2, right, we are applying, no, are we applying diff by 2 or diff? So let me, I am sorry, we were applying V diff by 2, right, because that is what the terminology was. So let us make the correction, so this becomes V diff over 2, so the other guy becomes V diff over 2. So this Vx becomes V diff over 4, y is C1 becomes V diff over, gm V diff over 4, so everything scales by a factor of 2 more, right? Okay so if Vx becomes 0, right, if Vx becomes 0, what can you comment on the incremental current through M1? So the exact incremental current through M1 in the presence of both the inputs, in the presence of both the inputs, then Vx, let us sketch it again. In the presence of both the inputs, when we have V diff over 2 here and minus V diff over 2 here, Vx goes to 0, which means R0 is irrelevant, which means I can say that Vx is essentially 0.
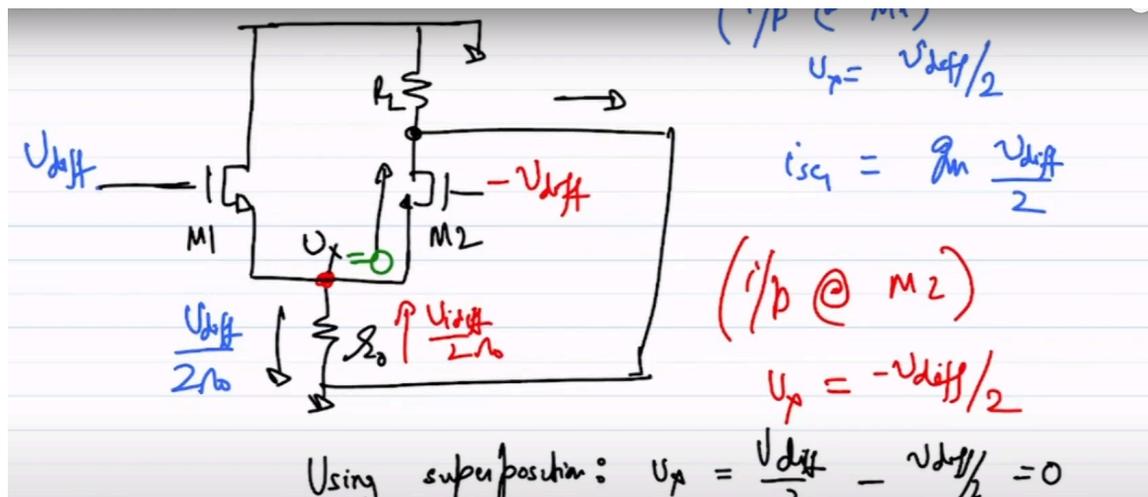
So if Vx is 0, right, when you are applying an anti-symmetric input, if the Vx is 0, then I do not have to analyze both the circuits, I mean these circuits in a combined form. What I can essentially do is say that these are both incrementally grounded, right, and I will try to find out what is the short circuit condition, right? So note that this is not an exact ground, I should not be connecting them like that. So this is the ground, this is actually like this, but this for the purpose of the analysis, this voltage is essentially 0, right? This voltage is essentially 0 when we apply a differential signal, which means that when we apply both the signals together, right, V diff and minus V diff or V diff by 2 and minus V diff by 2, then this current becomes gm times V diff by 2 flowing downwards and the other current becomes gm V diff by 2 flowing upwards, right? So what is the short circuit current? This is gm times V diff over 2 flowing in the direction shown, correct? So what is the Norton's equivalent? The Norton's equivalent for this

becomes gm V diff over 2 and you have the same output resistance which is RL parallel to RDS2, right? So what is the output differential voltage? What is the output differential voltage? Output differential voltage becomes gm times V diff over 2. What is the differential gain then? So the differential gain that is A diff is V o diff output differential by input differential. What is the input differential voltage? Input differential voltage is V1 minus V2, which is V diff, which becomes gm times RL over, right? So what is the summary of whatever we have done till now? The summary of whatever we have done till now is the differential gain does not get affected even if we use a non-ideal current source, right? So the key takeaway is differential gain is unaffected even if the current source is not ideal.

Why? Because Vx tends to 0. But what gets affected? The common mode gain, right? ACM or write it out, common mode gain that is ACM is non-zero and is inversely or rather is proportional to 1 by R0 of the current source, okay? Okay, right? So these are the key takeaways. So one of the ways of expressing both these things, both these parameters together in a compact format is called common mode rejection ratio and that is called the common mode rejection ratio or CMRR, right? I mean, this is essentially a definition of how, it is a definition of the gain, differential gain over common mode gain, right? So why is this definition important? This definition is essentially telling us that higher the common mode ratio, rejection ratio, then it will naturally mean that either the differential gain is high or the common mode gain is low. Ideally, what do you want the common mode gain to be? In presence of a ideal current source, we want the common mode gain to be 0. Essentially, ideally we want CMRR to be infinite. However, in the presence of a non-ideal current source, the common mode gain is no longer infinite and no longer 0.

In fact, this is equal to minus gm RL by twice R0 because it is not, by the way, this all mod, right? I mean, we are talking about a modulus quantity. So essentially, the effect of putting a non-ideal current source is to make, what is the effect? The effect is the CMRR goes from infinity to a finite value, right? And why is CMRR important specification? Because CMRR is important because, note that, note that if the quiescent, if we have identical voltage swings at M1 and M2, right? If we have identical voltage swings at M1 and M2, you do not expect V0 to change, right? Because this is ideally supposed to be a differential amplifier, is not it? It is ideally supposed to be a differential amplifier. So, if we have a common mode swing, that is the gate voltages of M1 and M2 are both swinging, then we do not expect the output to change. However, if we have a finite common mode rejection ratio, right? Which means V0 responds to a common mode input, right? When I say common mode again, what I essentially mean is, the gates of M1 and M2 are swinging in unison in the same direction, even then V0 will change. Granted, it will not change by a large amount, but it will still change, right? And that is,

how much will your differential amplifier respond to a differential input or rather, yeah, so how much your differential amplifier will respond to a differential input as opposed to a common mode input, right? So that, that metric is captured in a single nice formula and that formula is the ratio of the differential gain to common mode, ok. .