Course name- Analog VLSI Design (108104193)
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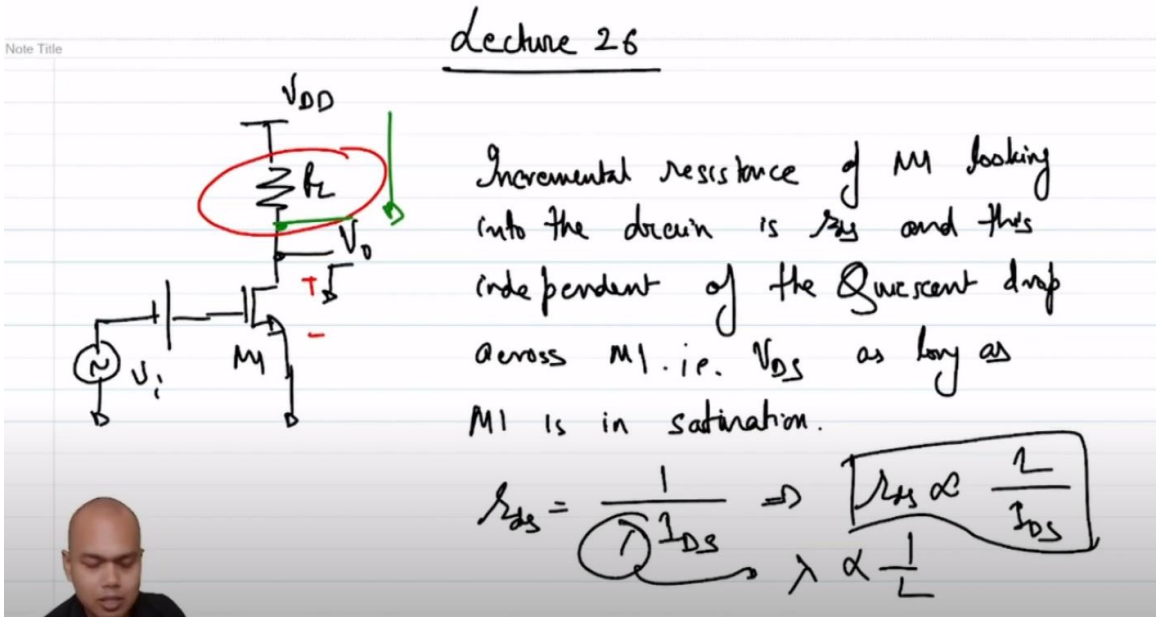
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 9
Lecture- 26

Welcome back, this is lecture 26. So, in the last lecture we were seeing how to replace or to increase the gain of our common source amplifier and what was the bottle neck and what are the potential solutions right. So, so we saw that if this is our classical common source amplifier, the gain that we were supposed to get. So, the gain that we were supposed to get between this node Vo and Vi is gm times RL right and in order to get larger gain we have to use larger RL right. So, if we have to use larger RL if I then we saw that it is not in our control to keep on increasing RL right because if we keep on increasing RL then what is going to happen? If the power supply is fixed and if I keep on increasing RL then that voltage drop the quiescent voltage at Vo will keep on going down and after certain after some value of RL the drain voltage of the transistor will go below the overdrive voltage and which essentially means that your transistor is gone out of linear. So, what was the mood point? The mood point was it seems like the gain is related to the quiescent drop across the RL right.

So, if gain was related to quiescent drop across RL which means that if I need larger gain I would have to deal with larger quiescent drop across RL which means that if I have a power supply fixed power supply which means then it will naturally mean that there is a maximum certain amount of gain that I can get from this configuration and not beyond that. Now, the question is what if I want to get more and more gain higher and higher gain what will be the limiting condition? The limiting case here is the fact that we have to search for a solution in which the gain is independent of the quiescent drop across the load. So, essentially we were trying to figure out can we replace this guy with something so that the incremental resistance or whatever that thing is independent of the quiescent drop across that thing right. So, and we did not look too further because if we look at this transistor M1 right, we look at this transistor M1 what is the incremental impedance looking into the drain is rds right.

So, we saw that incremental resistance of M1 looking into the drain is rds and this is independent of the quiescent drop across M1 right i.e. rds right. So what is the key takeaway from here? The key or I should not write independent of the quiescent drop I should write so rds right. So, it is independent of the quiescent drop across M1 as long as the current is fixed or even I do not have to write current is fixed as long as M1 is in saturation right.

So, as long as M1 is in saturation what is rds? rds is 1 over lambda ids right. So what happens if I increase lambda sorry what happens if I increase ids? If I increase ids then naturally the it seems like the rds is decreasing right. However, we note that we have one more handle what is the handle that we have? This lambda is proportional to 1 over L right. So, in other words I can say that rds is proportional to L by ids. So, if you increase L in order to keep rds constant sorry you know if you increase ids in order to keep rds constant I have a handle that I can increase the length right.



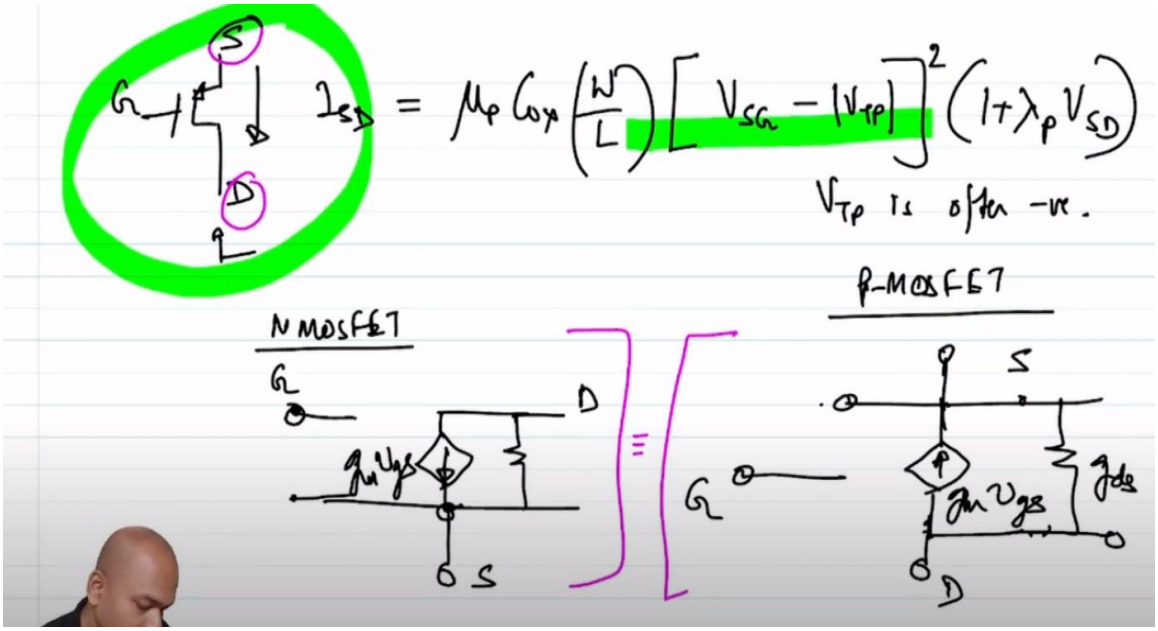
So, in essence this gives us a we already see there is a solution, but the solution is looking into the drain of the of M1. However, we were trying to figure out if we can replace RL with another transistor whose drain will be located at V0 and note that the drain has to be at for this new transistor the drain has to be at a lower potential right. So, since the because the current ultimately has to flow from top to bottom since this guy has to be at lower potential right. So, drain has to be a lower potential which means we cannot use an n MOS transistor. So, we went in search for another device and as it turns out a complementary device exists is called the p-MOSFET right and what were the characteristics of the p MOSFET? The p-MOSFET characteristics where the current that flows from the higher potential to the lower potential that is Isd in saturation is equal to mu p times Cox times W over L where mu p is the mobility of the carriers which is whole in this case times Vsg minus mod of Vtp whole squared times 1 plus lambda_p Vsd right.

Note that in these cases in the case of cases of MOSFETs, p-MOSFETs that we will be dealing with Vtp is often negative. However, we will be using mod of Vtp simply because we want the equations to look similar to that of a n-MOS transistor and we do not want to learn a whole new bunch of equations right. So, that was a whole reason of this of investing time in this and what is a good thing about this p-MOS transistor? The higher potential is

source, lower potential is drain and if it is biased in saturation the incremental impedance looking into the drain right will be rds p which can potentially be as high as the rds of a of an n-MOS transistor and as long as we can keep the p-MOS transistor in saturation right. As long as we can keep the p-MOS transistor in saturation then we can get high enough rds which is independent of the quiescent drop across the source to drain voltage right. So, and then we said that we also implemented the or rather we also analyze the incremental equivalent of this structure and we said that and we saw that incremental equivalent for an n-MOSFET right for an n-MOSFET the incremental equivalent was this.

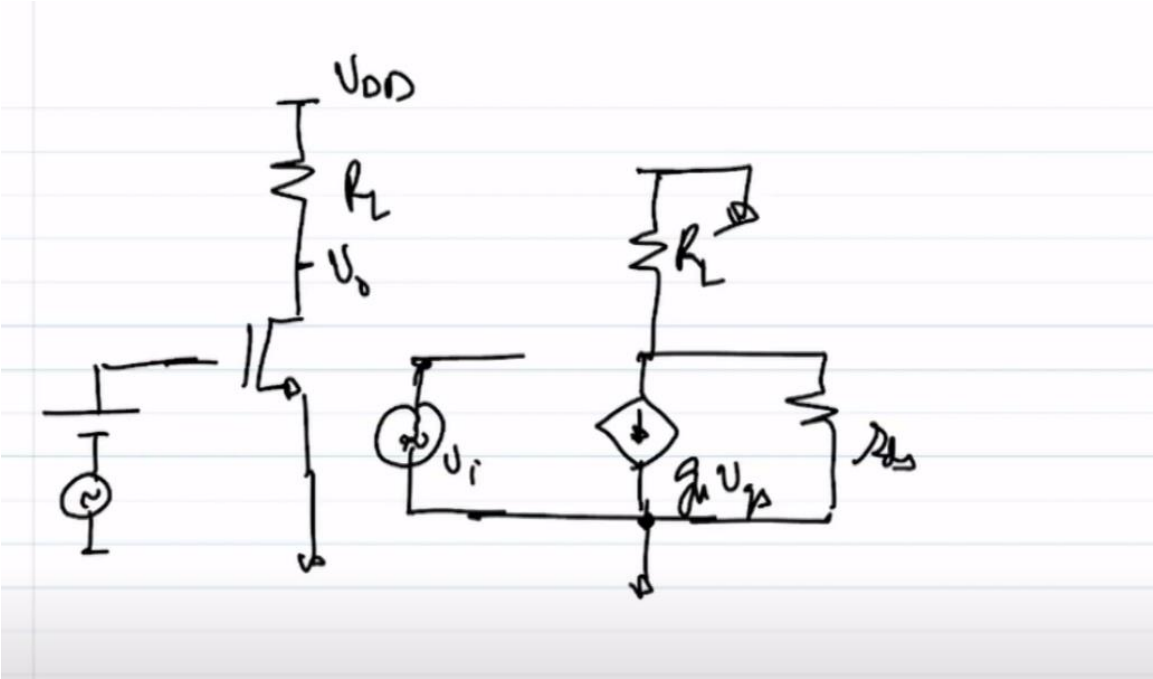
So, this is source gate drain this is gm times Vgs right. In case of a p-MOSFET the incremental equivalent was exactly the same things, but in a, but flipped right. So, since the drain is in the actual picture the drain is in the bottom. So, we would like to have the drain connected at the bottom. The gate is wherever the gate was the source comes out to be MOSFET ok.

So, this is the drain terminal and you have a you have a current source this is a source ok. And we should also say that the voltages are taken between gate and the source just like in case of in case of an n-MOSFET ok. And what is this what is this value of this current source this has to be again gm times vsg right. If we because our because this equation has vsg right, but if we say that we want an equivalence between we want an equivalence between the n-MOSFET incremental model and the p-MOSFET incremental model we do not want to remember anything new. Then we will say that we will use gm times vgs right and what will be the current direction? The current direction will be will be looking up right and then we will be having at this resistance here which is again vgs right ok.



So, these two are kind of increment these two incremental models are broadly the same things we have again the gates terminal source terminal drain terminal we have gm vgs in

both sides right and we also have the current flowing from drain to source right. We have also have the current flowing from drain to source. So, in both cases so essentially these two are these two are incrementally identical right you have gm vgs current flowing from drain to source in both cases, but the way we tend to sketch these incremental models is we flip it right we flip it because ultimately in the we know that ultimately in the in the full in the actual model right in the actual model in this in these guys the drain is at a lower potential right. So, just because we want to have an equivalence it is better to follow this flipped flipped mode right ok. So, now where we stopped in the previous lecture was here that what was the incremental model of of this guy incremental model was the same old same old.

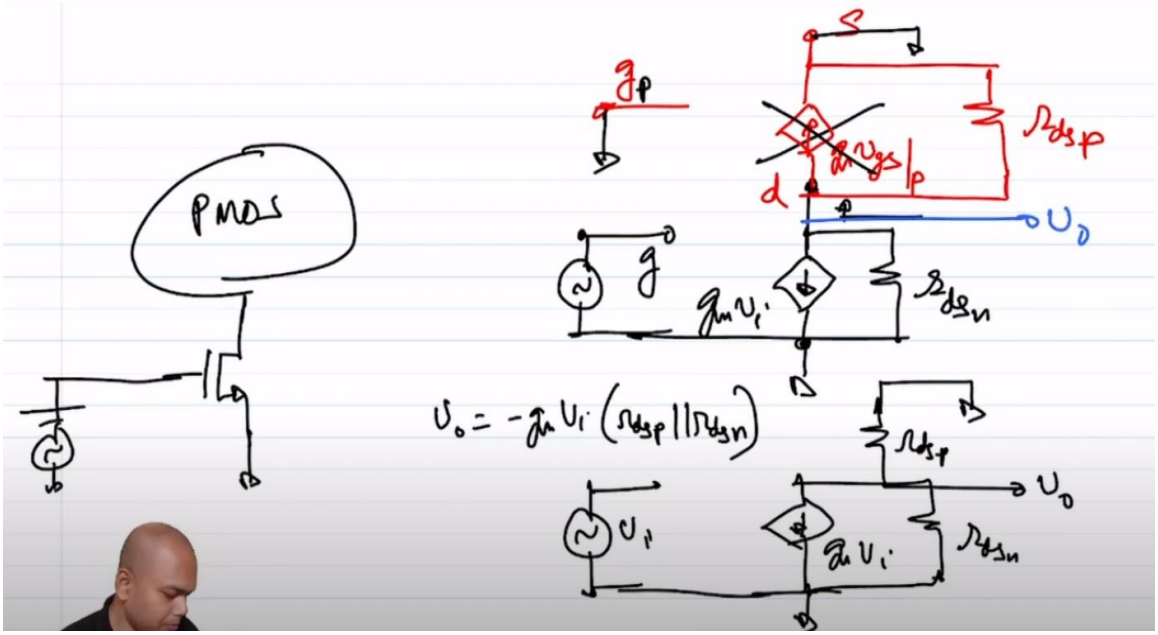


So, we have Vi here gm vgs where vgs is equal to Vi we have rds and we have rl which is incrementally connected to ground right. The whole issue is I mean the whole song and now that we are doing is because we wanted to replace replace this rl ok. So, incrementally what was the solution that we came up with incrementally the solution was to replace rl with with something which is the drain of the transistor and we said that maybe the PMOS equivalent is a is the equivalent is a good way to go. So, what would have been the PMOS equivalent in the incremental sense? So, this also what we would do is we retain the nMOS side rdsn right and this is gm times Vi this is 8 and here on the top side we will we would like to look into the drain of another transistor which we know now has to be a PMOS transistor. So, so what we will do we will replace we will replace the rl with the incremental equivalent of a PMOS transistor.

What is the incremental equivalent of a PMOS transistor that we just did? So, drain this is gmVgs for a for the PMOS right then you have gds or rdsp right and you have the gate here

this is the source this is the drain the current direction is going from drain to source as usual ok. What do you think should we do with the source or rather if we want to let me ask you this if we want to only see if looking upwards right looking upwards if we want the resistance to be only rdsp right looking upwards if we want to see what resistance of only rdsp then what do you think should happen to this gmVgs guy? The gmVgs should be should be 0 right. So, gm cannot be 0 gm of the PMOS transistor cannot be 0, but as a designer we can set the Vgs to be 0 which means the gate has to be the voltage difference between the gate and source has to be 0. So, what is the easiest way to make the incremental voltage difference between the gate and the source to be 0? I will make the incremental gate to be 0 and I will make the incremental source to be also 0 right. So, incremental gate to be 0 means what? So, let us do the incremental gate 0.

So, so we ground the incremental gate the source is also incrementally grounded if that is the case then this guy goes off if this guy goes off what do you think will be the voltage at this node? What do you think will be the voltage at this node? The volt so the so equivalent if I simplify this circuit if I simplify this so this I should say this is gate of e right. If I simplify this circuit what do I get? I get Vi here, gmVi here, rdsn here and on top what do I get? I get rdsp to the other side is incrementally grounded. So, what is V0? So, clearly this rdsp and rdsn are coming in parallel right. So, your V0 will be V0 will be minus gm times Vi rdsp parallel rdsn ok. So, so since we are looking into the drain of both the transistors right hence it is possible to get a large value of gain right as long as we keep the transistors in saturation ok.



So, this is as far as the incremental picture was concerned, but we also need to need to ensure that the incremental picture of the MOSFET is replaced by the actual picture of the MOSFET right actual symbol of the MOSFET including biases. So, so that is the next thing

that we should concentrate. So, let us do that the NMOS side we know how to go about doing how to go about biasing. So, we would not spend too much time using on that, but on top we need to put a PMOS transistor. So, here I have to put a PMOS transistor and we have to ensure that the PMOS transistor is in saturation right ok.

So, let us let us break the problem into multiple parts. Let us say that I have a PMOS transistor ok. Let us say that I have a PMOS transistor and I would want to bias it in saturation right. So, what is the what is the strategy? So, what do we know we need to ensure that Vsg is greater than 0 or rather greater than some mod of Vtp right. Vsg has to be greater than some mod of Vtp.

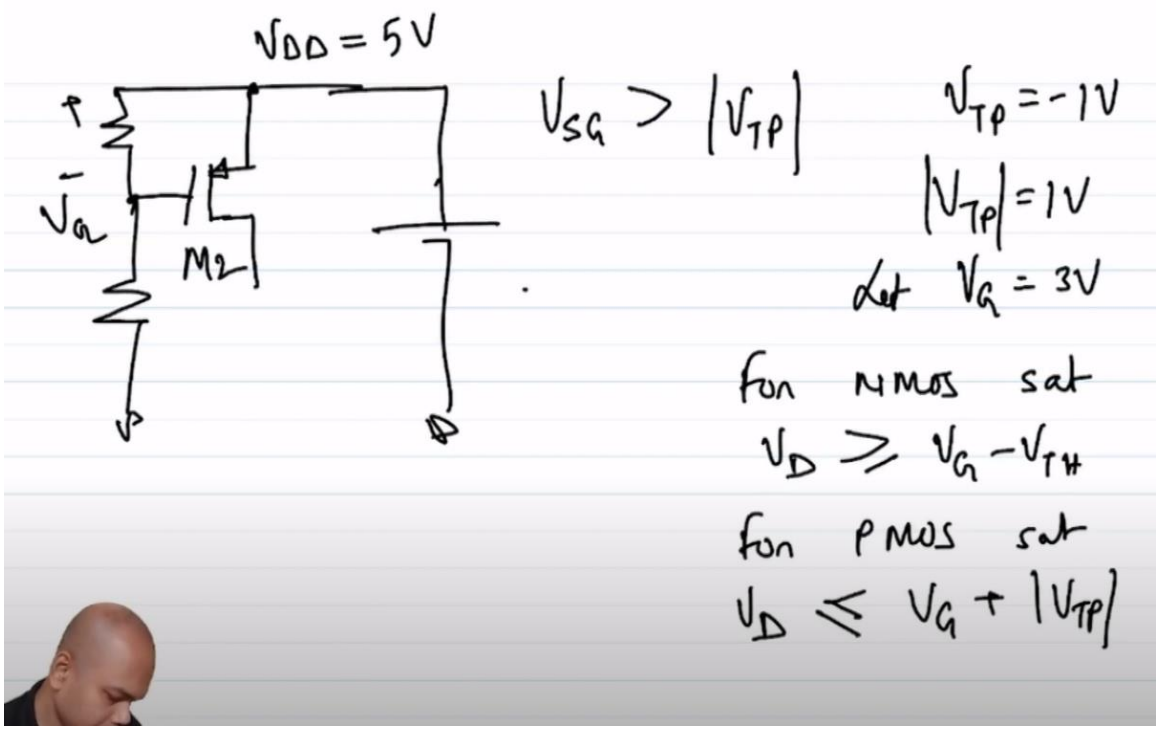
So, which means what we need to apply we need to apply a battery between the gate and the and the source. So, now we know that floating battery is impossible, but fixed battery is possible. So, what should we do? So, let us put a Vdd here and what do we need to do to the to the gate? We need to put some some voltage let us say Vdd equal to 5 volt right. We need to put and let us say we want Vs let us say Vsg is let us say mod of let us say Vtp equal to minus 1 volt, where mod of Vtp is equal to 1 volt. So, which means we need to apply a gate voltage which is lesser than 5 volts to make the transistor on.

So, let us choose a gate voltage of let Vg be 3 volts which means we need to put a battery of 2 volts between the drain between the drain and the gate of the device right. So, we know that this is again not possible, but we also know multiple ways of biasing right. We can say that we will put a resistor divider right. So, that the voltage difference between these two node is 2 volt right.

So, let us say we did that. What what should we do with the drain voltage then? What should we do with the drain voltage to ensure that this transistor M2 is in saturation? What is the constraint on on M2? So, this is Vg. What is the constraint on M2? In case of an nMOS what else the constraint? For nMOS transistor for nMOS the constraint for saturation was Vd had to be greater than equal to Vg minus threshold voltage. For pMOS what is the constraint? Saturation what is the constraint? The constraint is since everything is flipped right everything is flipped. So, this has to be Vd is less than equal to less than equal to Vg plus mod Vd right ok. Why less than equal to? Because because the condition for nMOS was the drain voltage can what is the how low we can get the drain voltage close to the gate voltage right.

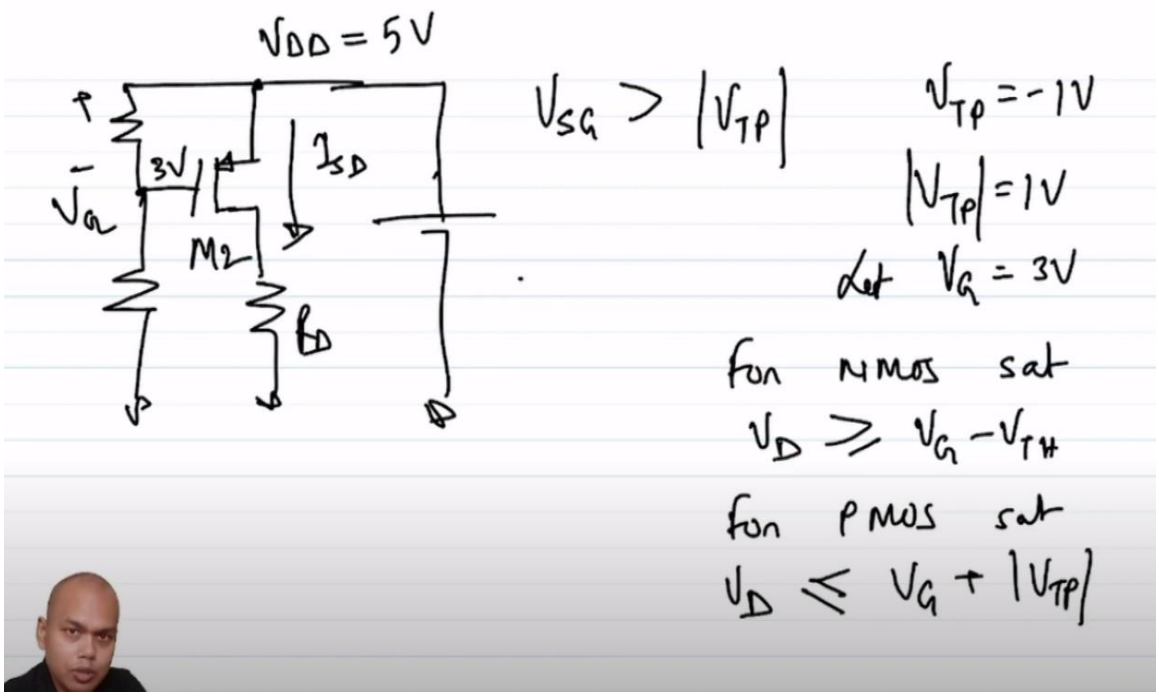
We saw that if the gate voltage is let us say 2 volt we can get the drain voltage one threshold voltage below the gate voltage right. If we keep the drain voltage if I lower the drain voltage below threshold below the gate voltage below one threshold voltage then I have I am having trouble. But note that pMOS is just the flipped pMOS goes the other way other

direction right. Since the pMOS goes the other direction what is happening? All the conditions are also flipping. So, in case of an nMOS there was a minima condition for for the drain voltage.



In case of an pMOS it will be a maxima condition for the drain voltage. So, how high you can bring the drain voltage above the gate voltage right. So, hence since this is a maxima condition which means the constraint is the drain voltage has to be less than something and as it turns out in this case using the same set of equations we can show that the drain the drain voltage has can cannot go higher than one threshold voltage above gate then you are in trouble right. So, the pictorial form of remembering this is if for an nMOS for nMOS transistor. So, let us say this is let us say this is the gate voltage let us say this is the color code this is gate this is drain source I am not sketching.

So, let us say this is the gate voltage that is fixed and let us say threshold voltage is positive which means that the drain voltage can be can go anywhere between higher than I mean can go as low as as low as one threshold voltage below the gain voltage right. So, for saturation if you go below this, this will be linear for a pMOSFET for a pMOSFET this is again gate this is drain right and again let us say our gate voltage is the same as in case of an nMOSFET, but the constraint here is the drain voltage can start from a lower voltage than gate and can go higher by one threshold voltage mod of threshold voltage. Note that threshold voltage of a pMOS is negative this is the mod of threshold voltage and if you go this side this will be linear right. So, this we are starting from a higher value and going down in case of a nMOS and we are starting from a lower value and going up in case of a pMOS right. So, this is towards linear this is towards ok fine.

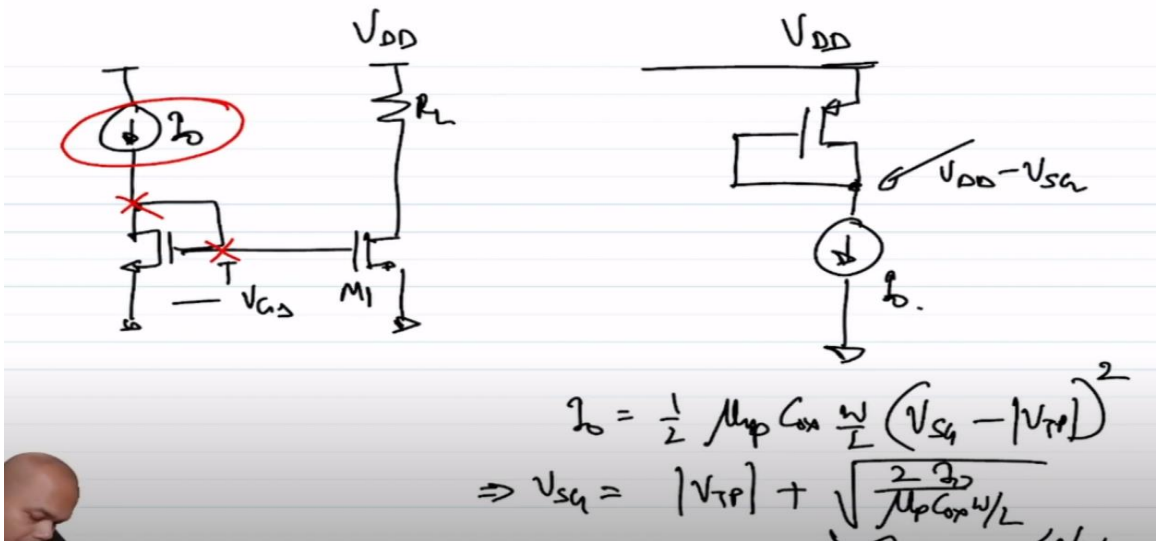


So if that is the case in this case let us say this is 3 volt let us say we figured out that this is 3 volt what is the maximum value of the drain voltage of M2 till which the transistor will be in saturation the maximum voltage will be 3 volt plus 3 volt plus the mod of VTP right. So, this is 3 volt plus the mod of VTP right. So, this will be maximum is 4 volt. So, all you have to do is to ensure that this voltage of M2 does not go above 4 volt and then the transistor is in saturation right. And what is the current direction? The current direction here is from source to drain and if the transistor is biased in saturation this is the voltage control current source the volt the current is some I0 some Isd right.

And if how do you bias I mean now we know multiple I mean we can simply put an Rd here and stop, but now we know multiple ways of multiple ways of biasing our transistor right using constant current source and that is something that we should we should explore as well right. So, let us let us explore that. So, in case of an NMOS what was the most what was the most convenient way of biasing a transistor using constant current source? Obviously, in case of an NMOS the most convenient way of biasing was I mean one of the most convenient ways of biasing was to a diode connected transistor right. This diode connected transistor creates a Vgs and we were feed it feed is VGS equivalent to the current source I0 and we then feed this Vgs back to our one of the transistors of interest and we and we bias a second transistor like this right. So, if we have to do the same thing for our PMOS transistor what should we do? We note that we have this PMOS transistor here right we have the PMOS transistor in case of in case of the NMOS transistors in case of the circuit on the left what were we doing? We were feeding a current into the drain of drain

of the device in case of the PMOS transistor we will have to do the exact opposite what is opposite because everything is flipped we will have to take current out of the drain of our PMOS device which means the constant current source will be connected at the drain right.

So, let us say I0 in case of a NMOS transistor what were we doing? We were connecting how was the negative feedback across the transistor getting satisfied we were connecting the drain and the gate. So, we will do the same thing in case of the PMOS transistor we will connect the drain and the gate right ok. So, why when we did when we do this right when we do this what will be the what will be the gate voltage easiest thing to do is to say what is to find out the Vsg what will be the Vsg? Vsg will be note that note that the current I0 in this case is half U P Cox W over L Vsg minus mod of Vtp whole squared which means that Vsg is equal to mod of Vtp plus under root of 2 I0 by mu P Cox W over L where this is the overdrive of the transistor right ok. So, in this case if this is the Vtp this is the Vsg what will be the what will be the gate voltage or the drain voltage in this case because gate and drain are shorted this will be Vdd minus the Vsg right. And what will happen to this voltage if let us say threshold voltage changes this voltage will adjust itself in order to keep give us constant current because this has been biased with a with a constant current source correct ok.

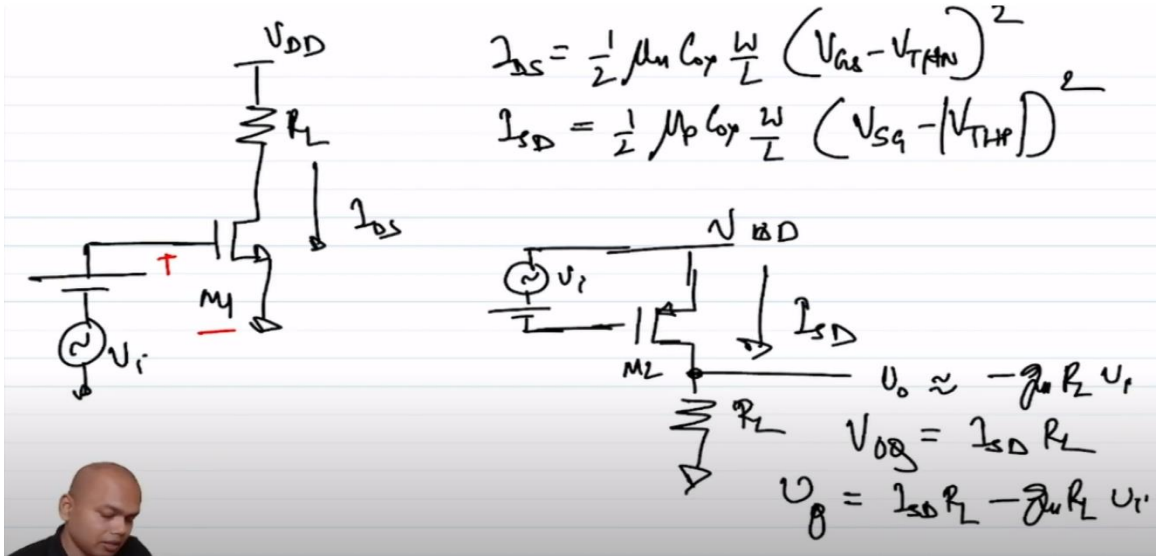


So, this is as far as the equivalence of this is as far as the equivalence of this structure and this structure is concerned correct. What about this structure what should we do? This is VDD let us say this is RL and let me call this M1 right. So, we need we need an equivalence of this correct. So, how do I get to the equivalence of this? So, let us let us take this let us take a general case of a common source amplifier of an NMOS and we will we will try to reason our way out of what is the equivalent of common source amplifier in case of a PMOS transistor right. So, so this is a let us do the biasing first ok.

So, this is M1. So, current is flowing from drain to source right. Let us say I want to keep the same current in in a PMOS transistor and I want to make up PMOS common source

amplifier using a PMOS transistor then what will what will you do? We know that these two are equivalent right. We know that these two are equivalent. What is the equivalence? Equivalence is Id in case of a NMOS the equivalence is Ids is the current equation is Ids is half mu n C ox W over L P G S minus threshold voltage whole square. In case of a PMOS it is Isd the current flows from source to drain half mu p C ox W over L Vsg minus mod of Vthn Vthp let me call it Vthp whole square correct.

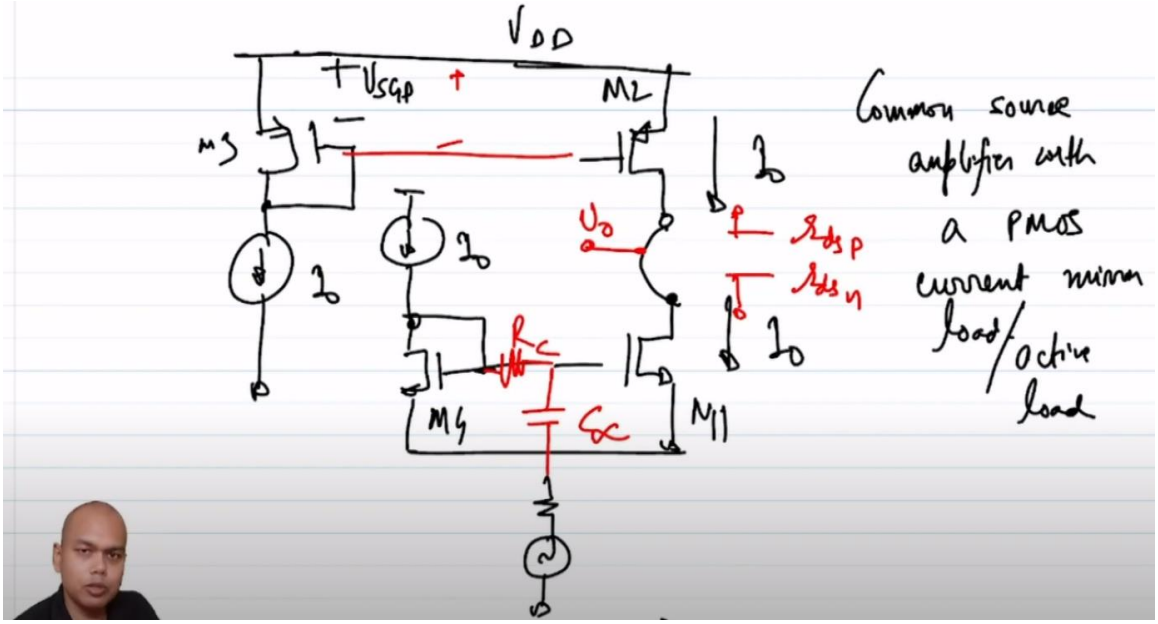
So if so, so what is the equivalence now? The current in the case of an in case of a NMOS flows from drain to source in case of a PMOS it goes both it flows from source to drain. So let us sketch the PMOS first and we also know that the source is of is at a higher term higher potential and in order we also know that in order to in order to ensure that this behaves like a common source amplifier the drain has to be connected to the sorry that load resistance has to be connected to the drain right. So load resistance connects to the drain R L and we know that the current flows from top to bottom this has to be the Isd right and we also know we also know that we need to hold if we if we want equivalence of Ids and Isd we need to have some value some held value between the Vgs of M1 and the Vgs of let us say M2 right. So as long as I mean I neglected the fact that I mean I have not really mentioned till now that mu n and mu p are not similar numbers, but if mu n were equal to mu p right and both of them have the same W by L both M1 and M2 have the same W by L then having the same Vgs or Vsd in both cases would have provided us the same drain current right. So let us say I need some Vsd so what was what is the easiest way to get the Vsd so equivalent thing is to say I will connect the Vdd here and we will we will apply the equivalent Vsg here and what should we do with that what should we do with the R L the other side of Rl the other side of Rl should be incrementally grounded in this case there is no difference between an incremental ground and absolute ground.



So this becomes a this becomes a biasing of the equivalent biasing for a PMOS transistor and now in case of an in most transistor if we want to turn this into a common source amplifier what we need to do we need to put a voltage source in series with the in series with the battery. So in case of a PMOS transistor we can also do the same thing we can put a voltage source in series with the battery and we take the output from the drain of the device right. So what should we expect what should we expect this incremental Vo to be the incremental Vo should be the incremental Vo should be minus gm times RL times Vi what will be the quiescent Vo the quiescent Vo will be Isd times RL. So what will be total Vo total Vo will be Isd times RL minus gm RL times Vi right. So why are we doing all these things we are doing all these things because ultimately we have to go back to we have to go back to our requirement of requirement of how should we replace the load resistance and put up PMOS on top correct.

So let us which essentially means that we have to we will have to go back to our original circuit. So let us sketch the circuit here so if we only concentrate on the biasing picture and let us say M1 is in saturation right if M1 is in saturation what is the we have some current Io flowing through flowing through M1 and we want to replace we want to replace the load resistance with the PMOS transistor on top right. If we want to replace the load resistance with the PMOS transistor on top and we also want the same current to flow through flow through it and I also want the drains to be connected to each other. So let us do the most obvious things first let us connect the drains together for the PMOS transistor. So if we want let us say this has some Vgs so let us say this is call it Vgsn right and after doing some calculations we figured that we want some Vgsp on the PMOS transistor on M2 we want some Vgsp for it to source a current of Io then we should do we should put a battery of Vsg which is equivalent to the voltage that is required to source a current of Io.

So now what is the most convenient way of generating this Vsg we do not want to put a battery we also do not want to put a resistor divider because all the problems of resistor divider in case of an NMOS will also come in case of a PMOS. So what is the other way of biasing what is other way of generating the Vsg other way of generating the Vsg is this right is this. So you will basically steal this architecture and what we will do is that we will say that we have a constant current source Io I will diode connect it right and this voltage will naturally become Vsgp the voltage difference between the Vdd and the gate will naturally become Vsgp all we need to do is to apply this voltage difference not that not the voltage itself but the voltage difference so that we can simply do by sharing both the source and the gate terminals of these two transistors let me call this M3 right. So essentially what will happen if we if we if we bias our transistors like this what will happen what is going to happen we will see that as long as as long as we are getting as long as M2 and M1 are in saturation as long as M2 and M1 are in saturation that is a critical if right right. So we will see that the current through M2 and the current through M1 will be equal to Io right



but again I this is not the full story because we cannot also bias M1 with a with a constant with a constant voltage source because of problems we have discussed before.

So what is the other way of biasing this we can say that we let us take another current source and generate this voltage that is required to bias M1 right the current mirror bias you remember right. So let me call this M4 ok ok. So and this current source become Io right. So the current mirror biasing between M1 and M4 is ensuring a current of Io and the current mirror biasing between M2 and M3 are also ensuring a current of Io. So the current through M2 is also Io current through M1 is also Io these two are match as long as we can ensure that M1 and M2 are in saturation then what then we know that that looking in impedance the incremental looking in impedance into the drain of M2 is rdsp and the incremental looking in impedance at the drain of M1 is rdsn.

But now the question is how do I apply an input I mean we know how to an apply an input to the n MOS side and then we will essentially do that. So let us copy one of the when we will basically use one of the earlier methods that we had right. We apply an input and what was that if we have this guy all we need to do is to AC couple our input here this is some C infinity and we put a resistor here some RC right. So this will give us this will give us the architecture for a common source amplifier right with a PMOS load right. So this is a this is a common source amplifier with a PMOS load right.

I should say PMOS current mirror load this is also called that this load is not a physical resistor this load is the load the the incremental loading that M2 is providing is through a PMOS it is an active device right because it requires a VDD to get biased properly. So this is also often called active load right or active load ok. So what I request you now is to is to

sketch the incremental equivalent of this entire model right do it yourself. So basically all you have to do is to is to replace each of these transistors all the four transistors with the incremental equivalent right. Assuming M1 and M2 are in saturation right that is not guaranteed assuming M1 and M2 are in saturation we put the sketch the incremental equivalent of this and find out find out the gain what where where will you take the output clearly we will be taking the output at this node because this is the drain terminal of M1 and M2 right yeah .

So please do it and I will see you in the next class. Thank you. you