**Course name- Analog VLSI Design (108104193)**
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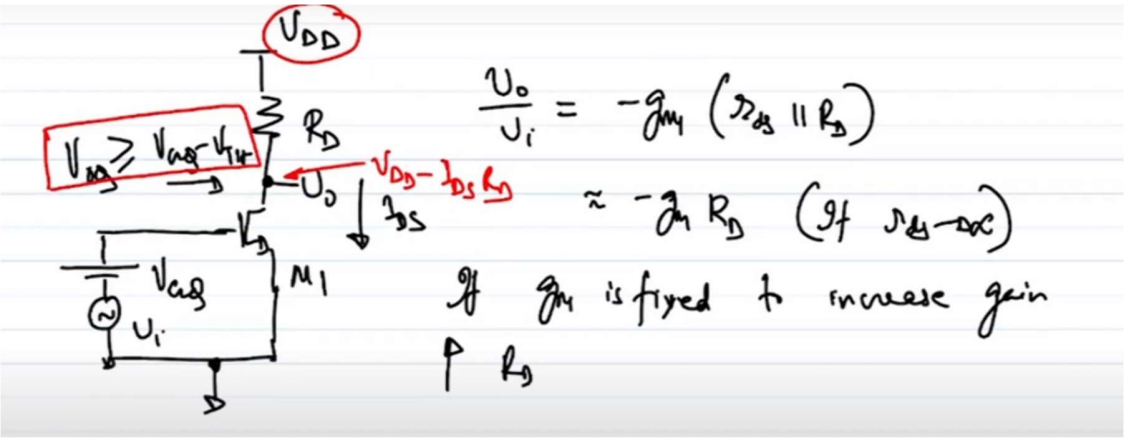
**Week- 9**
**Lecture- 25, Module-1**

Welcome back, this is lecture 25. So a quick summary of what we have been doing throughout this course. So we started off with the need of a non-linear element in order to get, in order to make a device which in order to make a net circuit which can give us power amplification. Then we saw that a certain type of non-linearity is required, not all non-linearities will give us power amplifications and based on our requirements we zoomed into the fact that the device that of our choice required certain characteristics which had very high output impedance, very high trans conductance, very high input impedance right and no and very small reverse conductance like between port 2 to port 1 and then we saw that we could do that using a MOSFET, in particular we used an n MOSFET right. So and in order to then we further extended the arguments and said that now that we have a MOSFET to make an amplifier, we would also want to ensure that the amplification factor or the factors that control the amplification like gm, gds and so on, we would like them to be stable with respect to change in ambient conditions. In other words, we wanted those factors to be robust to any change in ambient conditions, especially temperature, especially voltage swings and so on and so forth right and then we saw certain types of biasing, we saw that we required constant currents biasing for that we had to devise current mirror based biasing and so on and so forth.




So however, there is one still niggling problem and that is what we would like to see in this lecture. So now this is our humble common source amplifier and by now we know how to bias this guy, so in various ways, so we will not bother about that for the time

being and we will go back to our classical way of biasing the common source amplifier right with a voltage source with the, but we should always keep it at the back of our mind that there are multiple ways of biasing right. So this is easy to draw, so I drew this. So this is Vdd, this is RL, Vgq, Vi and we need V0 here and we saw that the gain that is V0 over Vi in this case a small signal gain was the gm of the transistor times rds of the transistor parallel RL right and if we say that rds is much higher than RL like in case of an ideal transistor rds is infinity right, this becomes approximately equal to minus gm1 times RL if rds tends to infinity correct ok.

So now if we look at this for that if we stare at this equation what is it telling us? It is essentially telling us that the gain is proportional to two things, one is the trans conductance, trans conductance of M1 and other is the load resistance RL right. So now or let me say let me call this the drain resistance excuse me, let me call this a drain resistance Rd because by definition the load resistance is not a variable right. So let us assume this is a drain resistance Rd ok. So what does gm depend on? gm depends on the size of the device, gm depends on Vgq the overdrive voltage and so on and what does Rd depend on? Rd is the biasing resistance on top. So if I have to increase let us say I fix the value of gm right and if we have to increase again what should we do? If gm is fixed, if gm1 is fixed to increase gain we need to increase Rd.

So fine this is ok, this is alright we can do that, but do you think we can do it indefinitely? For example, if I want let us say I have a gain of 10, I want a gain of 20, I doubled Rd then I want a gain of 40, I doubled it further, I want a gain of 80, I doubled it further and I kept on going and if I keep on increasing Rd do you think this architecture will work or there is something that can be problematic? Clearly there will be something that will break and I am sure you have already identified it, what will break? The biasing condition of the transistor M1 will be a problem right. So under we all know that M1 should be in saturation right. In saturation what is the characteristics of a transistor in saturation? The characteristics of transistor in saturation is that the current through the transistor IDS is not dependent on the drain voltage right, if that which means this is a current source. If it depends on the drain voltage then it does not become a current source. So in a transistor in saturation for a transistor in saturation IDS is independent of the drain to source voltage right which and what is the limit of saturation voltage? The limit of saturation voltage is the quiescent voltage at this node V0Q should be greater than equal to Vgq minus threshold voltage.

Now if you fix VDD, if you fix VDD, VDD is fixed and if you keep on increasing Rd what is happening to the quiescent voltage? The quiescent voltage at V0 is going down lower and lower and lower right. So if it goes lower and lower ultimately it will hit this limit and the transistor M1 will no longer be in saturation. If it is no longer in saturation

then the output resistance of the transistor drops dramatically hence the gain will start to drop as well. So what is the solution to this? The solution to this one of the solutions to this is to say that hey looks like the only thing that we need to do is to ensure that the voltage at the drain of M1 should be always be higher than Vgq minus threshold voltage. Now what is the voltage for a fixed IDS what is the voltage at the drain of M1? This is VDD minus IDS times Rd and if we have to keep this above certain limit of Vgq minus threshold voltage while I will increase Rd what do we need to do? We need to keep increasing VDD as well right.

So what is the conclusion? The conclusion is to ensure M1 is in saturation even after increasing Rd we need to increase VDD. So since and that is why in some of the problems that you have already done in this course you would have seen that sometimes the choice of VDD is 5 volts sometimes the choice of VDD is 7 volts sometimes the choice of VDD is 10 volts. The different choices of VDDs are there so that we can ensure that the transistor in question remains in saturation. However, this is a problem right. The problem can be expressed in two fronts one is we seldom have a choice of VDD in modern in several technologies or in almost every chip set that you will see there is typically one battery that powers the entire system and the battery is of some value maybe 3.

3 volt maybe 5 volt maybe 1.2 volt there will be some battery which powers the entire system and you will have to run everything along you have to run the entire circuit by drawing current from the battery. So if that is a problem I mean that will become a big problem because now essentially what we are saying we are saying that we cannot keep on indiscriminately increase the value of RD because there will be a certain maximum value of RD beyond which I will not be able to keep the transistor in saturation. Now if that is the case that limits the maximum amount of gain that I can get out of a configuration of a common source amplifier right. So which means that for a fixed VDD or a fixed therefore for a fixed VDD we cannot increase RD indefinitely right.

This will not be able to increase VDD RD indefinitely this limits the maximum possible gain from a common source amplifier okay. So now that raises a problem that I mean what should we do? Should we say that okay this is what it is we cannot do anything or should we explore further? As it turns out we can do something and whatever we can do is based on one critical observation and the observation is as follows. So if we are trying to figure out what is the incremental output impedance at this node right. What is the incremental output R out? What we see the incremental output impedance is a parallel combination of the impedance that we see looking up and impedance looking down right. What is the impedance looking up? This is RL.

What is the impedance looking down? This is RDS right and since RL is less than RDS in case of most devices RL will be much much less than RDS. This approximately becomes RL since RL is generally much less than RDS right or rather say if RL is much greater than RDS which generally is the case and why is why do we generally have RDS to be very high? Because the drain impedance the impedance looking into the drain of a transistor is ideally infinite right. So this is because the RDS for a MOSFET in saturation tends to infinity right ideally. This is ideal. So essentially what we are saying is in place of this device RL if we can put another transistor right whose drain terminal is connected to this node right whose drain terminal is connected to this node then we are all set right.

So essentially what we are saying is if we can replace RL with a transistor whose drain is connected V0 right then R out would be equal to RDS let us say this is M1 RDS1 parallel some RDS2 where RDS2 is the output impedance of the second transistor right. Then it is possible to do so and why is it a why this is a lucrative thing to explore? It is a lucrative thing to explore because at the end of the day the RDS does not depend on RDS does not depend on the voltage across that between the drain and the source of the transistor right. So what I am essentially what we are essentially saying is in this architecture in this architecture the gain is dependent on the quiescent drop across RD right or yeah so in this case R okay we are using RL so let us use RL. The gain is dependent on the quiescent drop across RL because moment we increase RL to get higher gain then actually the drop across RL increases. However if however that the quiescent drop across a transistor does not determine RDS right so this is possible right.

So note that the quiescent PDS does not affect RDS as long as PDS is greater than equal to PGS minus threshold voltage right. So this is a big positive right so in essence we will be able to decouple the gain from the quiescent conditions. If we can decouple the gain from the quiescent conditions then it is probably possible to get higher gain with a limited power supply. Now in order to get higher gain we have no other option but to increase the power supply. However now if we are able to use MOSFETs right if we are able to use MOSFETs in place of RL then it is probably possible to decouple the biasing condition from the achievable gain right.

So let us see if that is possible so what should we do? So let us sketch our common source amplifier once again. So what do we need to do? Here we have VDD so here we need to put something we need to put a transistor whose drain is connected to V0 right. So let us since we know that the transistor physically is symmetric device geometrically there is no distinction between the drain and the source right. So we can just put a device here and let us assume something is biased here right. So let us say we this is biased with some voltage P2 it is a n MOS transistor and let us assume this is in saturation right.

So do you think this is going to work? So before we get into the understanding of whether this is going to work or not let us first identify which is a drain and which is a source terminal of this transistor right. So what determines what is a source and which is a drain? The higher potential is always the drain in an n MOS transistor right. And also the Poisson current flows from higher potential to lower potential the current will flow from top to bottom which means naturally this terminal becomes the higher potential and this terminal becomes the lower potential. So this terminal becomes the drain and this terminal becomes the source which means that the arrow right that determines the source goes at V0. So what is the consequence of this? What is the impedance of the transistor looking up into the source? What is the small signal impedance? So let me call this M2.

So I am asking what is the this is M2. What is the small signal impedance R in looking up into the source? So you can replace this guy with its equivalent impedance we have done that multiple times and what impedance do we see? The impedance that we see is R in is equal to 1 over gm plus gds or gm2 plus gds2. So this is nowhere close to rds right. This is much lesser than rds of the device. How could we have gotten rds? We could have gotten rds had this terminal had this terminal been the drain terminal, but this is unfortunately not and that is because the making of the n MOS transistor is such that that the structure of the n MOS transistor is such that the lower potential is always source.

But fortunately we have another device which we have not introduced till now, but it is time to introduce the device and it is a device which is a complement which complements the n MOS transistor and that is called a p MOS transistor. So let us get the n MOS transistor cross section first. So let us say we are going back to the device cross section of a transistor once again. So let us say we are trying to make a n MOS transistor. We have a p type wafer then we have a oxide layer on top of that we have poly silicon layer you have a gate you have let us say we call this source we call this strain right and if and let us say this is body n plus n plus e plus and let us say the body and the source are connected for the time being.

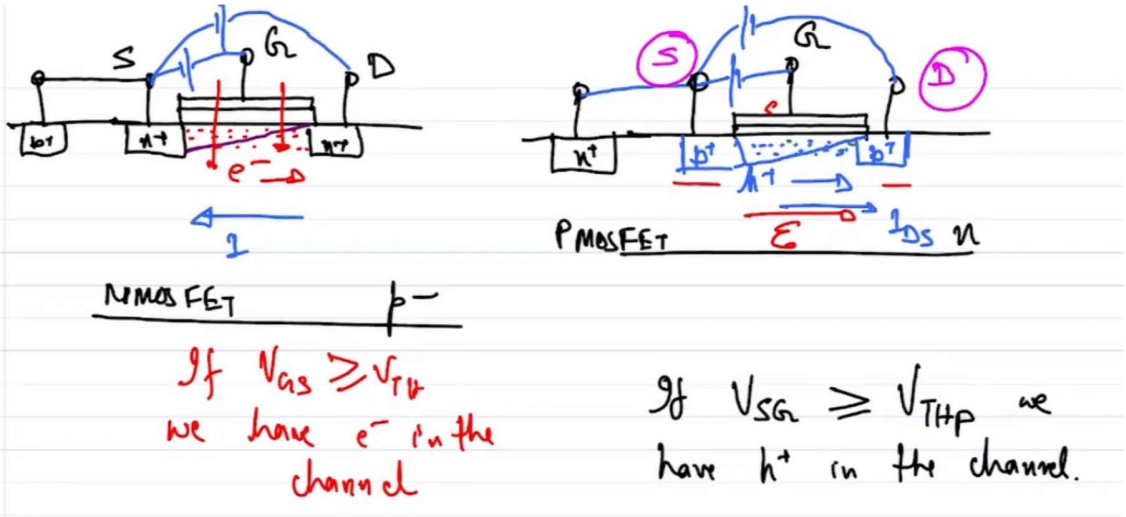
So if in this case if V g s is greater than equal to threshold voltage we have electrons in the channel right we have electrons in the channel. For the time being let us also assume that let us also assume that the source and drain are connected and there is a voltage between gate and the source right. So if V g s is greater than threshold voltage we have electrons in the channel right and then if we apply a drain to source voltage and then if we apply a drain to source voltage right the electrons tend to gravitate towards the drain so the electrons move this way and we get a current that flows from right to left right so this is I right and if we keep on increasing the drain to source voltage we start having

pinch off and since we start having pinch off we are no longer able to influence the channel charge from the drain and hence we have high impedance from the drain terminal. So as it turns out we also have a complementary device where everything all the dopings are of the opposite polarity right by that what I mean essentially is so we have a device where the base is n-type and we have a doping here of p-type and we have oxide on top and we have metal layer on top of that we have gate then we have terminals connected here and here and we have a body terminal right we have a body terminal and body is also of n-type ok. So now let us see what is going to happen.

So now what do you think I mean let us further assume like in case of the n MOS transistor the two terminals which we will be calling source and drain eventually are connected and let us also assume that these two terminals are connected just like in case of a n MOS transistor by the way this is called a p MOS transistor this is called a p MOSFET just like this is called an n MOSFET this is called a p MOSFET ok. The reason this is called a p MOSFET will be apparent just now. So what do you think will be what do you think will happen if we apply if we apply a voltage a negative voltage between or rather if we apply a voltage such that the that one of the terminals is at higher voltage than it right. So by the way I have sketched what do you think will happen so the volt the electric field in the vertical electric field will so this becomes a higher potential and this becomes a lower potential right right because the body of the p MOS becomes higher potential than the gate the electric field will go from the body to the to the gate right. So the electric field will go this way since the electric field will go in this way right the all the holes let me use a different color all the holes which are available here these are holes H plus will all the holes will tend to accumulate under the channel right.

So just like in case of in case of a in case of the n MOS transistor the electric field was going from top to bottom since the electric field was going to from top to bottom right all the holes were waiting pushed out and the electrons were getting attracted in the channel. The exact opposite is going to happen in this case if we have a if we have an electric field whose direction is reversed all the all the holes will get attracted to the channel and the electrons will get repelled right the electrons will get will get repelled from the from the channel. So eventually what will end up happening is we will be having a channel of holes right a channel of holes that connects these two terminals. So in other words in this case if V s g right so which I mean we can talk about which is source which is drain later on but everything is connected right now if V s g is greater than equal to certain threshold voltage let me call this V t p right we have holes in the channel right and just like in case of n MOSFET what is going to happen if we let us say if we let us say add potential between one of these two terminals right. Note that this is a higher terminal we are making this guy as a higher terminal and this guy as a lower terminal which means the electric field will go in this direction which means the holes will move in this

direction which means the current will also move in that direction right the current will also move in this direction right.




So I d s will be moving in this direction and what is the definition of drain and source the definition of drain and source is source is essentially that terminal from which all the all the carriers are originating in this case the carriers are originating from the left terminal and moving towards the right so this becomes the source terminal right so this becomes the source terminal and this becomes the drain terminal and if we have if we keep on increasing the V s d right in other words if we for a fixed source voltage if we reduce the drain voltage or for a fixed drain voltage if we keep on increasing the source voltage right what is going to happen you are going to have you are going to have we are going to have a pinch off where which side are you going to have a pinch off clearly again towards the towards the drain side right. So essentially what is going to happen is we are going to have a pinch off towards the drain side because why because note that the channel is in this case is formed as long as the difference between the gate and the channel is negative right negative beyond some value right so the gate has to be at a lower potential than the channel by a threshold voltage then only the we will have a will have a will have in the holes in the channel. Now if the drain voltage if the drain voltage is if the drain if the gate voltage is not sufficiently lower the gate voltage is not sufficiently lower than the channel voltage right you are not going to have inversion you are the the transistor will be in cut off region right the same thing happened in case of an nMOS transistor so we are what we are doing is trying to draw an analogy between an nMOS and a pMOS transistor ok. So the only other thing that we need to address is it looks like in case of an nMOS in case of a pMOS transistor the body needs to be of n type whereas in case of an I am sorry in case of a pMOS transistor the body needs to be of n type however in case of nMOS transistor the body needs to be of p type but does that mean that we cannot make everything on a single p substrate that would have been a

that would be a real really problematic situation as it turns out no we can do that so for that we just need to ensure that the pMOS has a separate well so the pMOS is normally guarded off with a separate well of n type on and that local well becomes its own well in which it can reside in ok. So this is as far as the very rudimentary introduction to the device of pMOS is concerned but more importantly what we are interested in is the is the is the working of the pMOS transistor right that is what we are going to that is what we are going to see next. .