Course name- Analog VLSI Design (108104193)
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Institute – Indian Institute of Technology Kanpur
Week- 08
Lecture- 24, module-01

Welcome back, this is lecture 24. So, in the previous lecture, we were discussing the use of a cascode configuration that is a combination of common source and a common gate stage or another way of saying the same thing is that combination of a common source at a current buffer stage in order to increase the output impedance of the amplifier right. So, this is what we saw. Let us sketch both the configurations together and we will do a comparison. So, the original structure that we had was this right, let us call this M1, D and we had to bias this, apply an input and take the output from this node right. So, but then we saw that the output impedance of M1 right, the output impedance of M1 that the impedance looking in was rds which was equal to 1 over lambda ids and depending upon what ids is and depending upon what lambda is depending upon what the channel length of the transistor is, you have we might end up having a reduction in gain because now in on top of on top of this RL, we are getting an addition in rds in parallel to rds right.

So, then natural question was to ask, what can we do to increase the output impedance and then we argued and we saw that one way to increase our output impedance was to put a current buffer incremental current buffer on top of M1 and that is what we did. Let us say this is called this is called this M1 again, we call this M2. So, we saw that this this configuration would have helped provided of course, M2 is also biased in saturation right and how did it help? It helped by it helped by increasing the output impedance here, it helped by increasing the Rout from rds to approximately let us write the full alone then we will do the approximate it from Rout to from rds to rds1 plus rds2 plus gm rds2 times rds1 right. So, what was this rds? So, let us sketch that also.

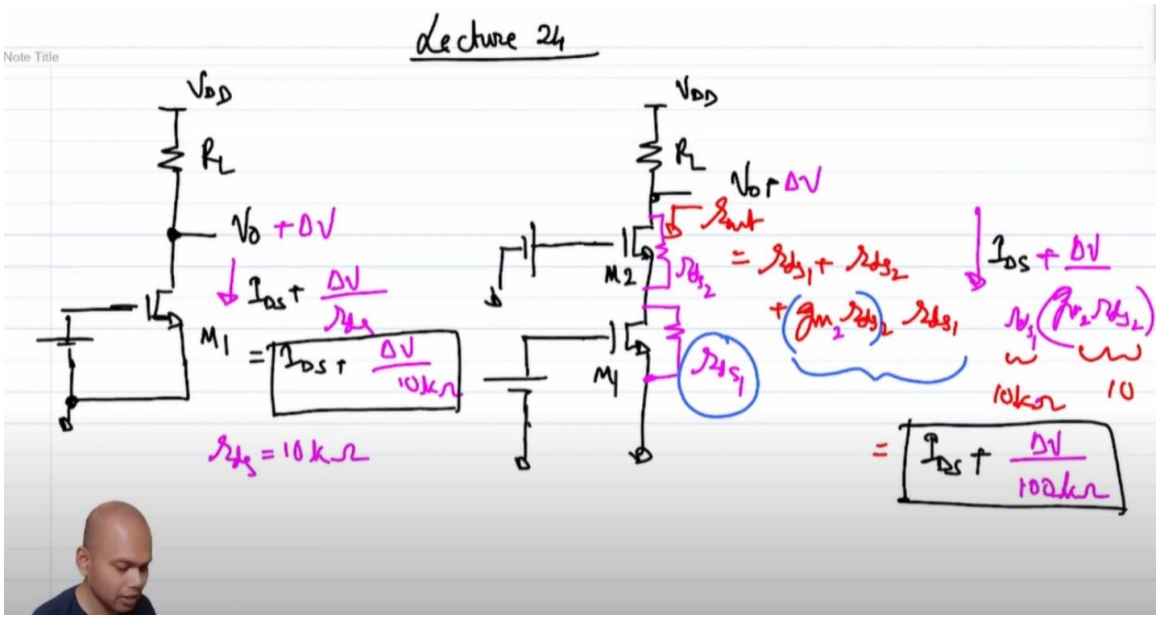
So, this is rds1. So, this was this was rds2 right. So, our Rout increased from Rout increased from being a mere rds to this to this value. This is clearly some of the rds of two transistors, but that is not the important part. The important part is we were getting an additional term which is a dominant term which is the original rds1, the original rds1 amplified by the gain of the intrinsic gain of the cascode transistor M2 ok.

So, this is an useful configuration and we also saw the requirement of what was the requirement in order to keep both M1 and M2 in saturation we had to we had to size them appropriately also we needed to apply appropriate voltages at the gates of the at the gates of the transistors. We also saw that since this current is current in this stack through M1

and M2 is controlled by the Vgs of M1 right. Now to a large extent it is controlled by the Vgs of M1. So, the Vgs of M2 becomes fixed. So, if you change the gate voltage of M2 the source voltage of M2 also modulates accordingly in order to keep Vgs fixed right.

So, then we from that intuition we could figure out how to bias the gate of M2 just to ensure that as to ensure that M1 and M2 both are in saturation ok fine. So, let us to drive home the point let me take some numbers and let us consider this for few more minutes. So, let us say for example, let us say rds1 let us say this rds for certain bias current ids and for certain lambda is equal to 10 kilo ohm right. I just pick a number let us say rds is 10 kilo ohm. Let us say rds equal to 10 kilo ohm and let us say V0 changes by some delta V right.

So, V0 changes from some Y-s and V0 to V0 plus delta V. How much do you think the current through M1 will change and let us for this case let us assume that since we are only concerned about the since we are only concerned about the output impedances let us short the incremental input. So, let us assume that we know I mean V0 goes from V0 to V0 plus delta V. How much current has changed? So, this current this current change from ids this current change from ids to ids plus delta V over rds right. That was that essentially was the incremental current that is I mean incremental current is basically incremental voltage divided by the incremental output impedance and that is what this is.



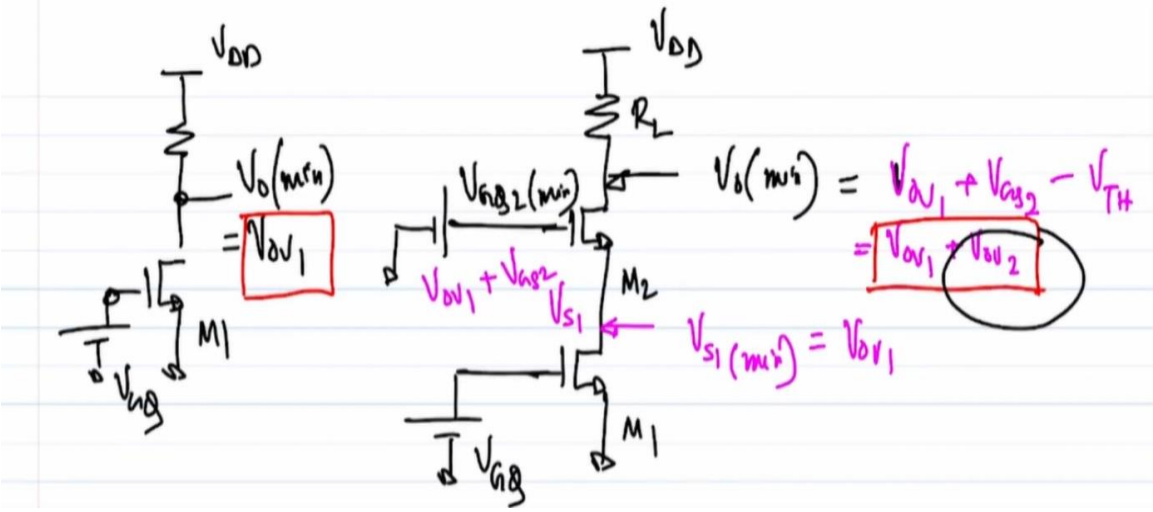
What is the what is the total current here? What is ids here? Originally the ids was same in both the branches but now let us say the output V0 changes from V0 plus delta V. How much will the current change by? Really in this case the current will change by delta V over the new output impedance which is approximately gm2. So, this is 2 right gm2 times rds2 times rds1 correct. So, clearly so in this case if rds1 was 10 kilo ohm and let us assume the gain of intrinsic gain of the transistor was also approximately 10. So, this becomes the

total current becomes ids plus delta V over 100 kilo ohm right.

In this case the total current would have been ids plus delta V over 10 kilo ohm. So, sorry for the yeah ok. So, from the change in ids would have been of delta V over 10 kilo ohm. In this case the change in ids is from ids to delta V over 100 kilo ohm. So, clearly you see that there will be a considerable amount of change in the incremental current.

This is obvious because this is the backhanded way of saying that the output impedance of our configuration has increased right has increased by a factor of 10 in this case which is equal to gm2 times rds ok. So, now let us dig deep further in this configuration and see some more interesting things. So, with respect to a common source amplifier what do you think is this configuration certainly gives you a better output impedance, but is there a downside? So, what I am essentially asking is, is this configuration better than this configuration in some way or is it only worse? So, let us think about from the perspective of the swing limits ok. So, let us assume I mean what is the absolute low voltage that you can bias you can bias the transistor M1 in a common source amplifier at V0 can be as low as dgq minus 1 social voltage right. So, V0 min can be equal to d over drive of M1 right.

What do you think will be the V0 min in the cascoded configuration? So, clearly this guy minimum voltage here right. So, this minimum voltage will be so let us mark this node let me call this Vs1, Vs1 min is equal to V over drive 1. Similarly, so what will be the gate of M2? So, Vgq2 min will be how much? This will be Vs1 min that is equal to V over drive of M1 plus 1 Vgs of M2 right. So, Vgs2 right. So, what will be V0 min then V0 min will be V over drive of 1 plus Vgs2 minus threshold voltage of M2 and if we assume the threshold voltage is identical then this effectively becomes V over drive of 1 plus V over drive of.



So, you see that in the circuit on the left the minimum output voltage is 1 over drive voltage of M1 in the circuit on the right the minimum over drive minimum output voltage is the

sum of 2 over drive voltage right which clearly means that at the output you cannot swing as much now as you could have had if you had used a common source amplifier. So, the cascoded stage the extra current buffer needs some headroom in order to bias itself and because it needs some headroom to bias itself you need you need to budget for that and what is that cost? The cost is the over drive voltage of the transistor ok. So, this is the cost that you pay fine. Now the question is how do I bias I mean ok this is all good that we understand this over drive I mean this is the minimum voltage of V over drive that will require but now the question is what should we do how should we bias go about biasing the transistors M1 and M2 because we have seen earlier that a constant voltage bias has issues right it is not a very robust way of biasing a transistor under the condition that the ambient voltages temperatures and everything can change essentially if threshold voltage changes then what happens? So, what is the equivalent threshold voltage independent biasing scheme that is what we are asking ok. So, let us draw the parallel with common source amplifier again.

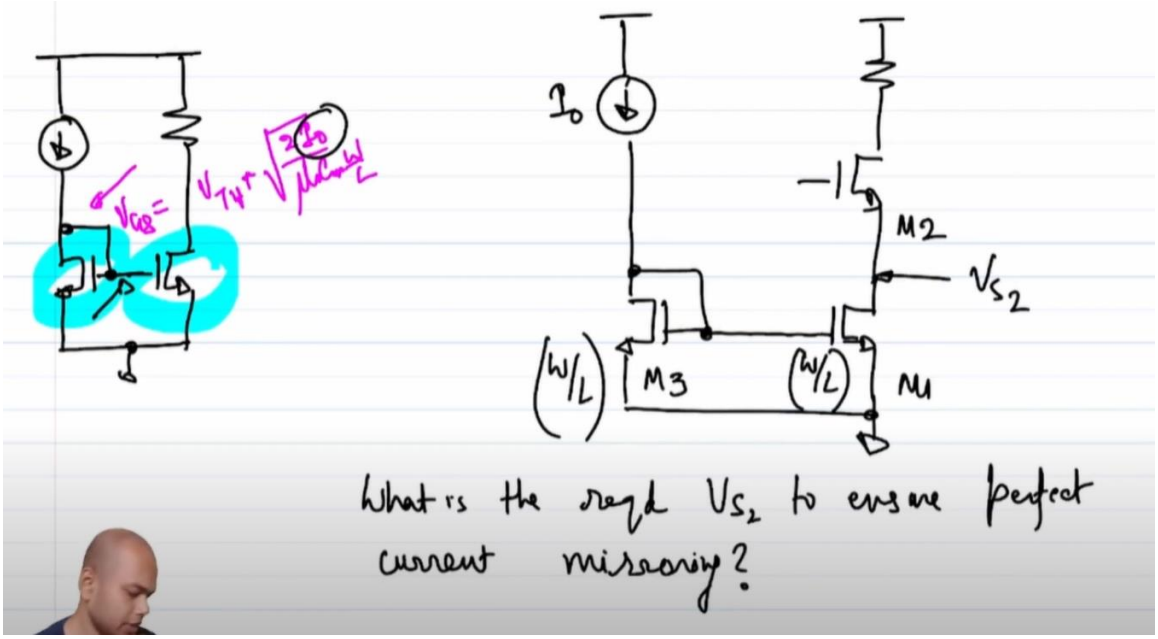
What was the biasing scheme for our common source amplifier? The current biasing the constant one of the constant current biasing schemes was using a current mirror right. If you recall in one of the earlier lectures where we covered current mirror or where we introduced current mirror this is what we had what we had seen. Why again why was it necessary? This was necessary because note that this voltage here right. So, this is Vgs, Vgs is equal to what? Vgs equal to one threshold voltage plus under root 2 I0 by mu n Cox W over L if I0 is fixed if I0 is fixed right then what is happening? The voltage of the Vgq the gate voltage is adapting itself to the change in threshold voltage. If for example, the threshold voltage decreases then Vgq decreases in order to keep I0 fixed if the threshold voltage increases right it keeps it increases Vgsq in order to keep the I0 fixed right in order to give the overdrive fixed ok.

So, in essence this whatever be the whatever be the ambient conditions the currents the quiescent current on the both the arms will be always be identical as long as these two transistors these two mirroring transistors right as long as these two mirroring transistors are identical. So, hence this is called a current mirror circuit right. So, can we use principles of this current mirror circuit to bias or cascode configuration? Actually we can and that is what we will do. So, let us start off with let us start off with how do I bias M1? Assume that we have a current source of I0 available to us. We can do the same thing we can borrow the same playbook from the circuit on the left.

So, let us do that let us say that I have a this is given. So, I generate a Vgs appropriate Vgs through this diode connected configuration right and feed that Vgs to M1 right. So, let us make we call this M3 ok right. Let us further assume that what is the underlying assumption? The underlying assumption is that both the W by L's are identical right. If

both the W by L's are not identical clearly the circuit.

So, when you have same Vgs same overdrive, but different W by L you will have different current right. So, here we are talking about a mirroring ratio of 1 hence we can we can get by taking a W by L of 1 fine. So, how do we bias M2? How do we bias M2? So, what is the minimum voltage that is required or rather what is the voltage that we require at the drain of M1 not the minimum voltage, but what is that voltage that we require the drain of M1 in order to ensure that there is perfect balance of current on both sides right. So, in the so let me repeat what I said what I am asking is Vs2 right. So, what is the is required Ts2 to ensure perfect current mirroring? So, let us think about it right.

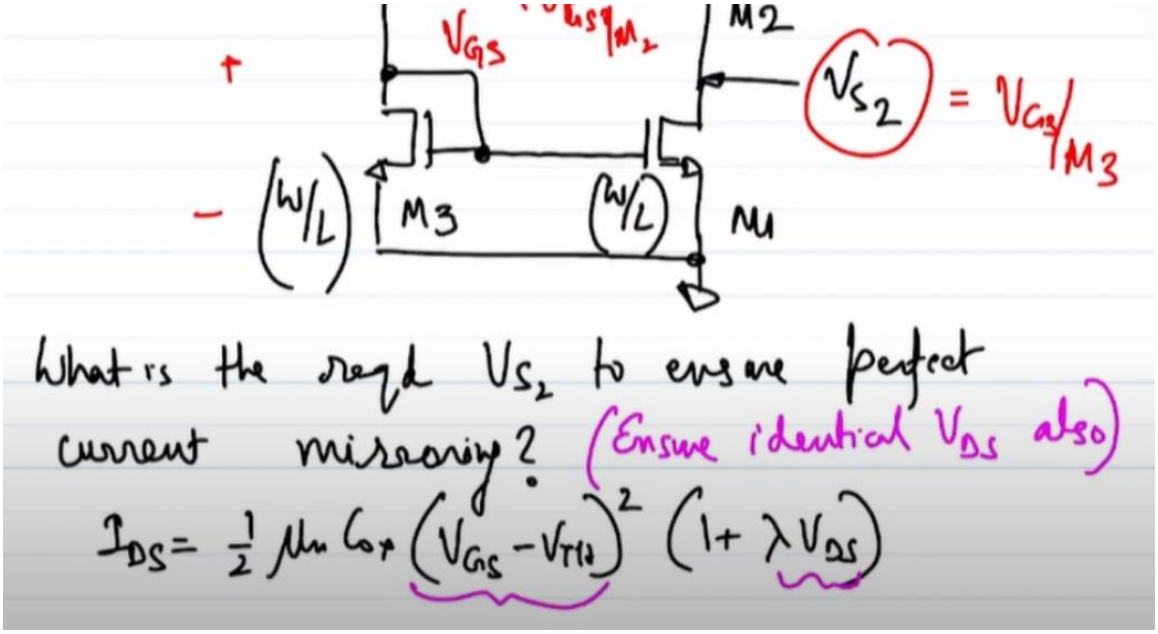


So, what is our current voltage equation for our transistor? The current voltage equation for the transistor in presence of channel and modulation is mu n C of Vgs minus threshold voltage whole square times 1 plus lambda Vds right. So, if two transistors need to have identical currents right and they have same Vgs same overdrive what needs to be also identical. So, this is identical between M1 and M3 because they share the same gates, they share the same source. However, this is not given right Vds we do not know whether they are identical or not. So, in order to ensure that the currents in the two branches are identical right not they are identical to a larger extent than in the configuration on the left what we need to ensure? We need to ensure that the drain to source voltage of M1 and M3 are also identical right.

So, we need to ensure identical Vds also right. If we ensures identical Vgs if we ensure identical Vds then regardless of what you do the currents in two branches will be identical even if even if temperature changes humidity changes right special voltage changes right as long as the characteristics of the two transistors are identical as a circuit designer if you

ensure that the Vgs and Vds are identical the currents will be will be identical correct. But now we have a problem right who is setting the Vds, who is setting the drain to source voltage in M3? Clearly the drain to source voltage of M3 is equal to the gate to source voltage of M3 because drain and source drain and gate are connected. So, this is Vgs correct.

So, this voltage is Vgs. So, how do I ensure what is the what how do I ensure Vs2 becomes Vgs? How do I ensure this? So, if I take you back to the previous lecture what you might have noticed is who is setting that voltage Vgs who is sorry who is setting that voltage Vs2? Clearly the bias the gate voltage of M2 was setting the voltage at Vs2. Why do I say so? Because this current is supposed to be largely constant this current is expected to be I0 regardless of whatever gate voltage you have. So, which gate voltage at M2 that you have which means the Vgs of M2 is constant since the Vgs of M2 is constant if you change the gate voltage of M2 the source voltage of M2 will also follow along in the same direction right. So, if we want the source voltage to be equal to Vgs of M3 right. So, let us say we want this source voltage to be Vgs of M3 what will be the expected gate voltage at the gate of M2 expected voltage at the gate of M2 this will be Vgs of M3 plus Vgs of M2 for a current of I0.

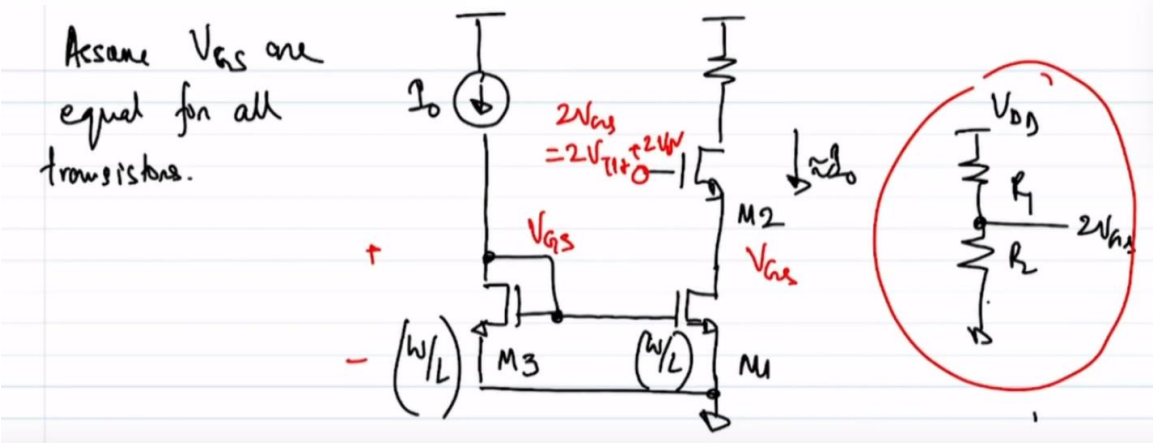


Of course, we are assuming all the currents are I0 and we for to start off we are assuming all the all W by L are also equal right. So, that is I mean when you start out you make some assumptions we are making that assumptions fine. So, essentially where are we at? So, let me copy this. So, ok. So, if we assume for simplicity it is not necessary, but let us assume this assume Vgs are equal for all transistors right.

This is just to make our explanation convenient it can it did not be identical right. So, let us assume they are identical for the time being. So, which means so that I do not have to

write a subscript all the time. So, this we expect to be Vgs if this is supposed to be Vgs right or this is supposed to be yeah this is supposed to be Vgs what is this node voltage supposed to be this is supposed to be 2 Vgs obviously for a current of I0 ok. So, I need to generate a voltage of 2 Vgs now right.

How do I generate 2 Vgs? Can I generate a voltage of 2 Vgs by let us say putting a register divider and let us say I have figured out that 2 Vgs is supposed to be 1.2 volt. So, I put a register divider of let us say one point I mean let us say I put a register divider this is Vdd this is R2 this is R1 and I size R1 and R2 such that this is 1.2 volt or this is exactly equal to 2 Vgs. Will this work? It might work for one particular very sweet case but it will not work across the variations of threshold voltages right because why? Because note that Vgs is equal to what threshold voltage plus overdrive voltage right.

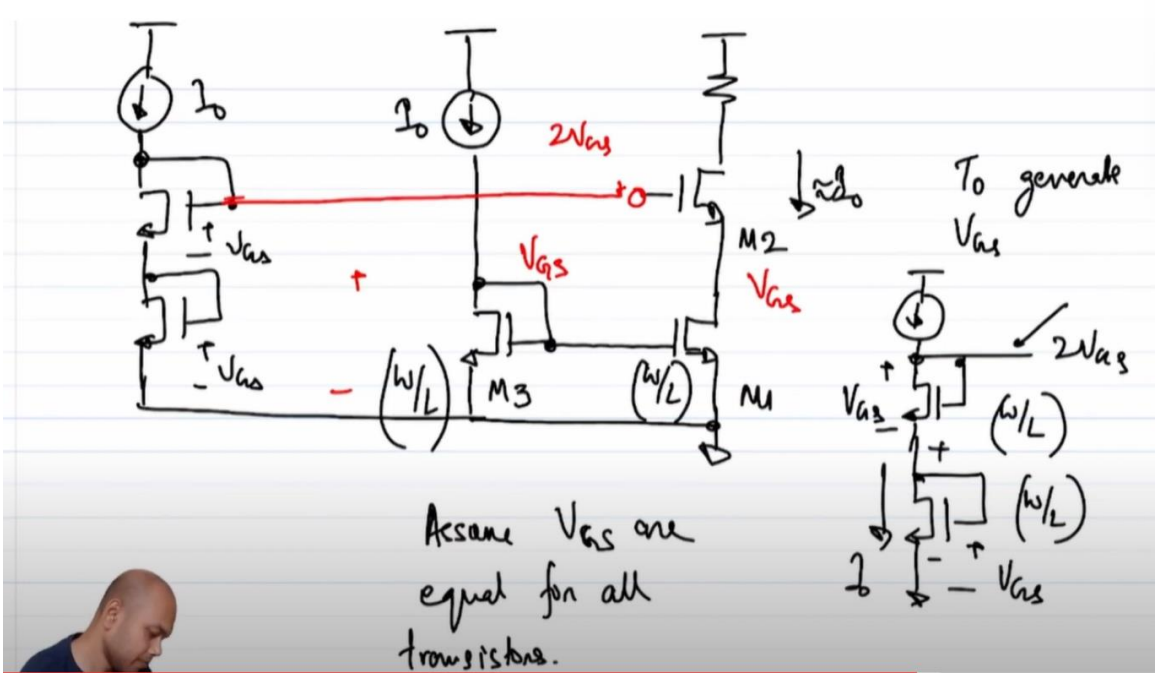


So, if threshold voltage changes 2 Vgs is essentially equal to 2 Vgs is equal to 2 Vgs this is equal to 2 threshold voltage plus 2 overdrive voltage right. So, if threshold voltage changes the requirement of that node voltage also changes. Now if I am making this with a bug if I am recreating that node voltage with a with a register divider as shown here then we will land into trouble right. So, what is the other option? So, let us take a step back again and then see what is the other possible option. So, how did we generate the voltage Vgs? How did we generate the voltage Vgs that was required to bias M1? We generated the voltage Vgs by biasing by pushing a required current I0 into M3 which was diode connected right.

So, you have to generate 1 Vgs right to generate 1 Vgs Vgs the modus operand device push the required current into the transistor and have a feedback by connecting the drain and the gate right. So, this is an automatic generation of the required Vgs. So, how do I generate 2 Vgs? So, this is 1 Vgs I need to put something I need to put something so I need to put something here to get another Vgs right. If I put something here to get another Vgs this voltage will be equal to 2 Vgs. So, what should I put there? So, if we see that this two terminal device right if this two terminal device is getting me 2 Vgs getting me Vgs if I put the same thing on top what would I get? So, if I put the same thing here what will I get?

What will be the output? Note that the what is the current now the current through this transistor is I0 hence the difference in voltages between the drain and the source is Vgs.

Again the same current I0 flows to the top transistor assuming both are W by L, W by L identical transistor same threshold voltage. What is the voltage drop? Between the drain and the source this will again be Vgs which means what will be the voltage at this node? This will be 2 Vgs and do you think this biasing scheme is will get affected by this generation of biasing scheme is better than the resistor divider? Of course it is because our transistor M2 in the original network wants a biasing voltage which changes with the threshold voltage variation in order to adapt itself and this clearly will serve the purpose right. So, since this clearly serves the purpose what we can simply do is copy this guy here. So, this gives me one Vgs this gives me another Vgs right and what we simply need to do is to connect these two nodes right. So, this is one Vgs this is one Vgs let me use a different color just so that we are not confused.



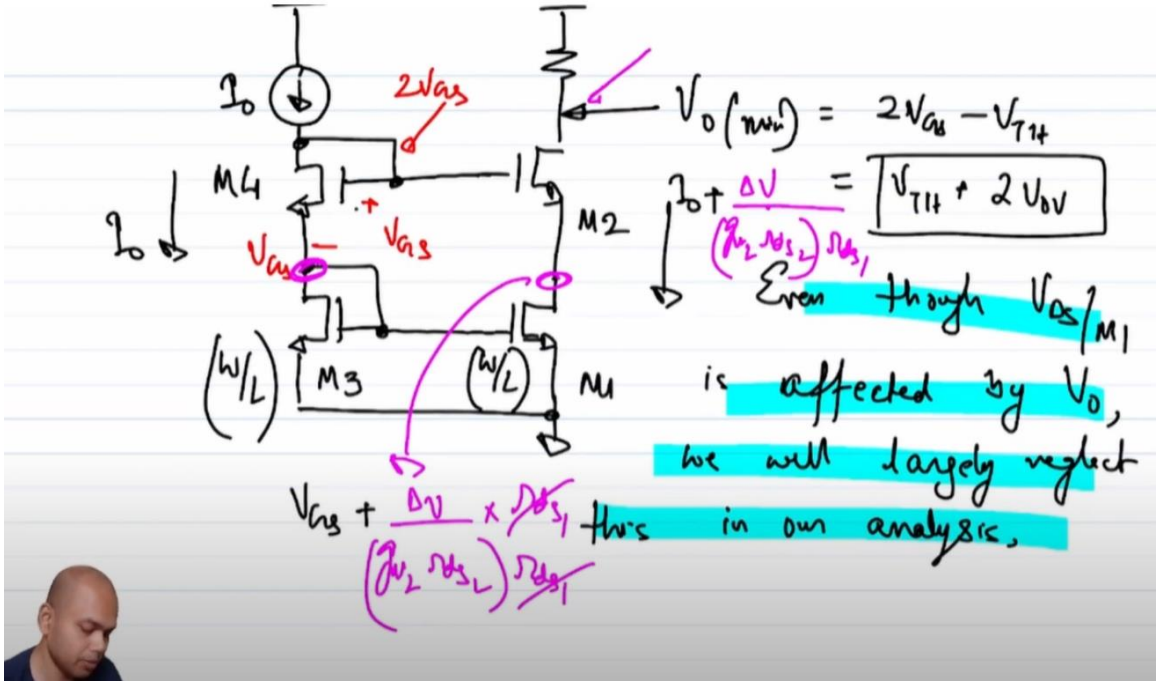
If we connect these two nodes this is one Vgs and this is one Vgs. So, this is one Vgs and this is one Vgs. So, this is one Vgs and this is one Vgs. So, let me use a different color just so that we are not confused. If we connect these two nodes we are good right.

So, this is 2 Vgs always an M2 gets 2 Vgs which is what it always wanted ok fine, but let us see can we do one step better? What is the current requirement in this branch? This current requirement is I0 right. Can we generate 2 Vgs from the current requirement of this branch? Because see note that we are already generating one Vgs. So, this guy is generating one Vgs this guy is also generating one Vgs and we are providing the same amount of

current in both the branches and just that we have put one more diode connected transistor on top to generate the second Vgs. So, instead of using a separate branch what happens if I put this guy put the diode connected transistor on the left leftmost stack we put this guy over here. So, instead of confusing you let me sketch what I am trying to say again because a picture is worth more than a 1000 words.

So, what I am essentially saying is forget about having a separate branch ok. But if we simply do this what will be this voltage? So, we know that this voltage is Vgs right and this voltage will also be Vgs which means this voltage will be twice Vgs and we no longer require the help of this additional branch right. So, we save some current because now we do not have to use a separate current source we can get by using one single one single current source right. Ok, so now what do you think ok fine. So, now the current on the left branch and the current on the right branch will be almost identical.

Why do I say almost identical? It will be almost identical because not exactly identical to the nth decimal place because note that this voltage is V0 need not be equal to 2 Vgs correct. So, this voltage can go how low can V0 go? How low can V0 go? Clearly V0 min now is equal to 2 Vgs minus 1 threshold voltage right which is essentially if I replace the Vgs with threshold voltage plus V over drive. So, this becomes 1 threshold voltage plus 2 V over drive correct. So, this is V0 min and this clearly is I mean this clearly can be lower than and this clearly is lower than 2 Vgs. So, V0 can need not be same as the drain to the drain voltage of M2 need not be same as the drain voltage of M4.



Since the drain voltage of M2 is not the same as drain voltage of M4 the incremental current right. So, that the current in both the branches will also not be identical to the nth

decimal place. So, if the current here let us say is this current in this branch is I0 what will be the current in this branch. When will these two currents be identical? These two currents will be identical only when the drain voltages of M1 is equal to the drain voltage of M3 and also the drain voltage of I mean so the current so the current will be identical only when they drain voltage of M1 is equal to the drain voltage of M3 right. So, essentially when this voltage and these voltage are identical then the currents in both the branches will also be identical.

However, the drain voltage of M1 is also affected by a second order, is also affected by to some extent by the drain voltage of M2 right. So, to the first order it's not we have been ignoring this effect up until now but because we still have that lambda Vds term for M2 right. So, the drain voltage of M1 will get affected by the drain voltage of M2 but note that but not by a significant amount had it been a common source amplifier without the cascode state right. So, the output voltage variation would have been di could have directly affected that would have directly affected the drain voltage of M1 but in this case it will not affect it as much right. So, even though we in this case so even though Vds of M1 is affected by V0 we will large we will largely neglect this in our analyzer.

So, this is something that we should keep in mind because it will help our analysis otherwise what will make what will end up happening is that when you do when you solve problems of current mirror based circuits you will end up with messy equations with third order terms and all and that will give you that will make the algebra unnecessarily complicated without giving us too much of insight. So, what we will do is we will assume that we will assume that the drain voltage of M1 is not affected by the drain voltage of M2 to the first order right. But if we had to calculate we can still do that because we know the incremental current right. So, what will be the incremental current? The incremental current here will be I0 plus whatever delta I have at the output delta V right let me use a different color. So, it is whatever delta V I have divided by the incremental output resistance looking into the drain of M2 what is that? That is clearly gm2 rds2 times rds1 right.

So, if this is the incremental current what will be the incremental voltage here? What will be the change in voltage? The change in voltage will be it will go from Vgs to Vgs plus this incremental current delta V over gm2 times rds2 times rds1 times rds1 because M1 has a output impedance of rds1. So, these two cancel. So, essentially the voltage at the drain of M2 will be the voltage at the drain the voltage at the drain of M1 will be the delta the change in voltage in the drain at in the drain voltage at M2 divided by the intrinsic gain of the cascode transistor divided by the intrinsic gain of M2 right. So, this is I understand this is slightly involved I covered I assume many things in these explanations right. But the key thing that you should keep in mind is this statement.

The key thing that you should keep in mind while solving your problem is this statement right. So, the drain voltage of M1 in the presence of a cascode transistor M2 is largely unaffected by is largely unaffected by the by the swing at the cascode node swing at the drain of the cascode transistor M2 ok. .