Course name- Analog VLSI Design (108104193)
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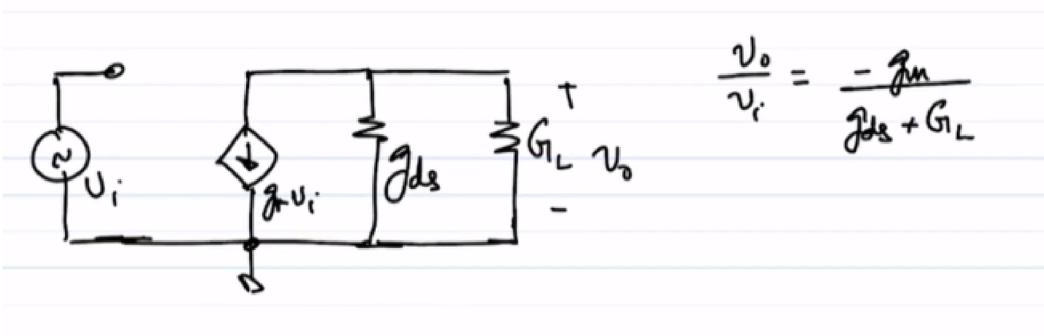
Week- 8
Lecture- 23

Now, welcome back, this is lecture 23. So, we were discussing in the previous lecture, the effects of effects of Y22 or GDS to our common source amplifier and we saw that, we saw that if we incorporate the effect of non-infinite output impedance or non-zero output conductance, right. So, if this is GDS grounded in our common source amplifier, this was the, this becomes the model and if I have an output load marked as GL and we are taking the output across the output load, what do we observe? We observed that V0 over Vi became minus GM over GDS plus GL and naturally this is a lower value of gain than that we have gotten in the absence of GDS.



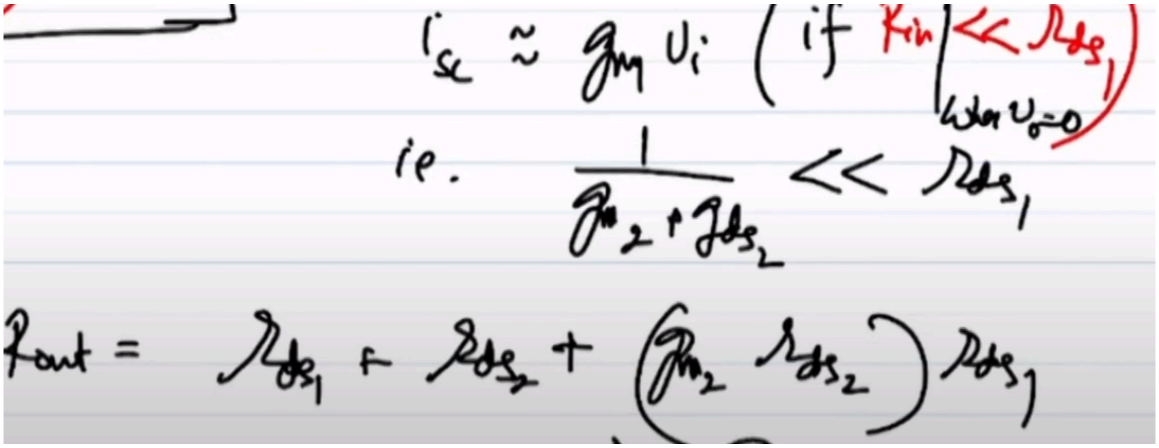
So, what was the solution? The solution that we came up with was use a current buffer, right. So, what is the current buffer? Again, a current buffer is a contraption that helps in pushing the current from a non-ideal current source to a load without the effect of loading, right. So in our case, our ideally, in our case, so this non-ideal current source was this section of GM, Vi and GDS, right.

This was a non-ideal current source, we have a load RL or GL, let me call this as RDS, RDS1, let me call this GM1 just to ensure that we are using the right consistent notations from previous lecture, right. So what do we need to do? We needed to, we needed to put a current buffer in between. So we needed to put a current buffer in between so that once we connect these, the amount of current that flows in, so this is GM times Vi or in this case the amount of current that flows in should be minus GM times Vi, right. So, the approximately minus GM times Vi and that was possible only if the looking in impedance, right.

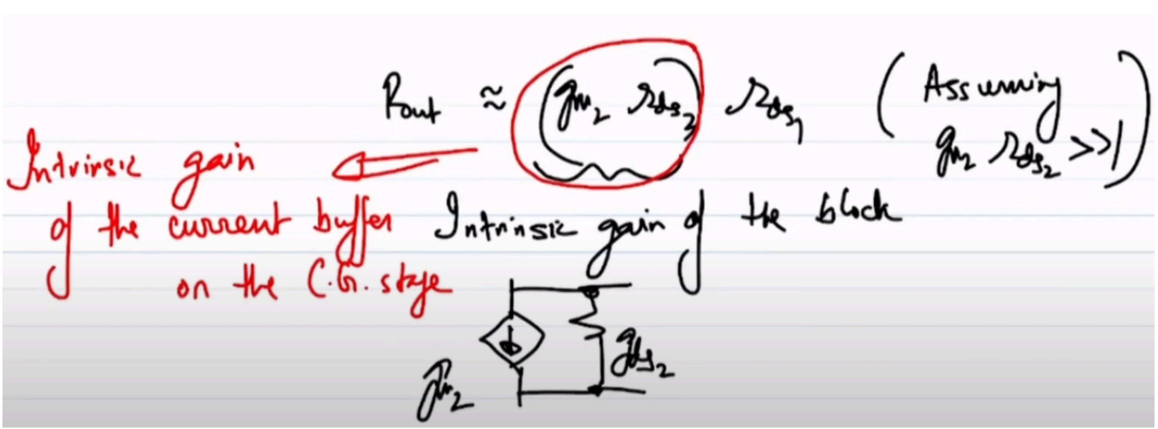
So, R in would have been approximately 0 or in other words R in is much much less than RDS1, right. So this was the one of the bare minimum requirements of a current buffer. What was the other requirement? The other requirement for a current buffer obviously is the fact that the output impedance R out, right, has to be much much greater than RL because a current buffer is nothing but a current controlled current source, ok. So and how did we do this? We had already seen that what is a current buffer? A common gate amplifier is a, can act like a current buffer and we and then we said that is, so now what we need to do is to replace this block, right, replace this block with a common gate, correct. So again what is the incremental model of our common gate amplifier? So now what we can do? We can put, this becomes GM1 Vi, this is GDR, let me call this RDS1, RDS1 we have the load RL and we had to put a common gate amplifier and we had used a common gate amplifier before and what is it? It is nothing but a, nothing but a contraption who is using a MOSFET whose incremental gate is grounded, right, whose gate is incrementally grounded and if we call this node as Vs, this current becomes GM times minus Vs because gate is grounded and just like any MOSFET we cannot neglect the output resistance, right, anymore because we now know that the output resistance is a reality, right and we connect this here and this becomes our Enaught, ok.

And then we further saw that, then what did we further see? We further saw that the short circuit current, the equivalent, not an equivalent model for this, so this is RL, we call this Isc and this R, this R out, so not an equivalent model for this was Isc was almost equal to GM1 times Vi under the condition that, under what was the condition? If the looking in impedance, right, looking up impedance into the source of the common gate amplifier would have been much, much lesser than RDS1, right. So if, whatever this R in was, if R in is much, much less than RDS1, so in other words this translates to i.e., if GM1 i.e.,

what was the looking in impedance? Looking in impedance was 1 over GM1 plus GDS, sorry, GM2 plus GDS2. This is the looking in impedance when the output was short circuited, right, so because we are trying to figure out what Isc was, so that is an important thing that you should keep in mind. So when this looking up impedance, this is R in was much, much lesser than RDS1, right, so this was the requirement, right. So this is R in when V0 is 0, so that is an important consideration because otherwise the R in will be different, ok. And what was R out? And we also saw that R out was the summation of these two resistances, summation of RDS1 and RDS2 which naturally should appear but we had one additional term and the additional term was, the additional term was GM2 times RDS2 times RDS2, correct.



And then we further saw that, we further argued that it is expected that in saturation this term will be much, much greater than 1, GM2 times RDS2 because ultimately in saturation we want an amplifier to behave like, a transistor to behave like a, like almost like a current controlled, voltage controlled current source which means its output impedance should be closer to infinity. So, uncertainty is not possible but which means the output impedance should be very high and also we are expecting GM to be very high, so we are expecting GM times R to be very high, so it is expected that GM times R should be much greater than 1. If that is the case, in saturation your R out almost becomes equal to GM2 RDS2 times RDS1, right, right, ok. So, this is assuming GM2 RDS2 is much, much greater than 1, ok. So, now couple of jargons, so in a common source, in an amplifier, right, in an amplifier if I go back to this, so the common source amplifier model, right, so in the absence of, right, so in a, when GL is equal to 0, right, when GL is equal to 0, i.e. RL is equal to infinity,



what is V0 over Vi? V0 over Vi will be minus GM1 times minus GM1 by GDS1, correct, right. So what does this, what does this mean? It essentially means that even if your load is infinite, you are not getting infinite gain, right. In an ideal common source amplifier, if it were an ideal voltage control current source, then if we had an infinite load, if RL would have been infinity, the voltage across that infinite load should also have been infinity. But in this case clearly that is not possible because the transistor does not have an infinite output impedance, right. So even in the absence of RL, you are going to get a finite gain.

And this gain which is limited by the characteristics of the transistor itself is an intrinsic property of the transistor and we call this the intrinsic gain, right. So essentially we call GM1 over GDS1 to be intrinsic gain of a transistor, okay. So what is the intrinsic gain of this guy? What is the intrinsic gain of this guy? The intrinsic gain of that guy is basically the GM associated with that block times the impedance associated or the resistance associated with that block, right. So what is that intrinsic gain? So this essentially becomes intrinsic gain of block GM2, essentially this becomes the intrinsic gain of this contraption. So why am I saying all these things? I am saying all these things because it seems like the output impedance, right, output impedance of this contraption, so this output impedance or in other words the output impedance looking here, right, in the absence of the current buffer would have been RDS1.

In the presence of current buffer, so in the absence of current buffer the output impedance would only have been RDS1. In the presence of current buffer it seems like the output impedance has gotten amplified by the intrinsic gain of the current buffer, right. So this is the intrinsic gain of, this is the intrinsic gain of the current buffer or the common gate stage, correct. So this is a very important property, this is a very important property that you will often see in many places that in order to increase the output impedance of an amplifier often we put, we pass the current that is coming out of a common source stage to a common gate stage, right, so that the output impedance increases and this contraption is also called a gas code block, right. So this is also called, let me use a different page to talk about this.

So this the current buffer, the combination of a common source and a common gate stage to increase the output impedance is also called a gas code configuration, gas code. Please note the spelling is C-A-S-C-O-D-E not cascade, the gas code configuration, ok. So many times we will hear people saying why do not you use gas code, moment you say that you have a low output impedance you might hear people say why do not you use gas code. So gas code by that essentially what one means is why do not you pass the current from the common source stage to a common gate stage, right, ok. So now that we know what this is at least what the incremental circuit looks like we need to then take the next step and see what will be the circuit look like when we replace the incremental equivalence with the MOSFET, right.

Ultimately we have to put the circuit together with the MOSFET, so let us do that, right. So let me quickly sketch the incremental equivalent once again. So this is V i, right. So this is the gate of the first MOSFET, so this is V m 1 times V i and you have this output impedance G d s 1, then the gate of the second MOSFET is grounded, right. So this is V g 2 is grounded, so this is G m 2 V g 2 minus V s, V s and we have V d s 2 and this output is obviously connected to a R L, ok.

So now let us replace this stuff with the, so let me put the R L on top so that I can save some space here, right. Let me put the R L here, ok. So now what is the basic thing we need to do? So basically wherever you see this contraption you replace that with the MOSFET. So here comes one MOSFET, right. So let us call this M 1.

Again what do you have on top of this M 1? You have another MOSFET, let us call this M 2, correct and on top of that what do you have? You have a resistance R L, right and now we need to bias, right. So how do you bias? M 1 is a common source stage. So how do you bias a common source stage? We know it by now, we have done it multiple times. So this becomes the common source bias, right. So let us call this V g u 1, ok.

How would you bias the transistor M 2? So clearly you cannot leave it floating. Can you keep it grounded? I cannot keep it grounded because of what? Because ultimately I need to bias the transistor in such a way that some current flows, right. We need some current, let us say some current I naught to flow in this stack, right. So by the way before we proceed, can you tell me who is setting the current in this stack? Clearly the current in this stack will be set by M 1. So what do I mean when I say who is setting the current in this stack? What I am essentially saying is which one is, on what factors does I naught depend on? What are the primary factors on which I naught depend on? So what does I naught depend on in a transistor? It depends on, primarily it depends on the V g s provided the transistor is in saturation.

Now as a designer we have to ensure that the transistor actually remains in saturation, right. So we can walk backwards and we can assume to start off that the transistor is in saturation and since I naught depends on V g s, so we can identify which is the transistor that is setting the V g s, right. So in this case M 1, the gate of M 1 is V g q, what is the source of M 1? The source of M 1 is grounded. So the V g s of M 1 is V g q which we are setting separately, right. So since we are setting separately the V g s of M 1, the current I naught will be determined by the V g s of M 1.

Now one might argue that what about the V g s of M 2, right. What about the V g s of M 2? Is M 2 V g s setting the current? I would argue no because, so let me take you back couple of lectures where we were discussing this. Let us assume that we need to bias this transistor M 2 with a constant current source of value I naught. How do you go about biasing this? How do you go about biasing this? Basically this will auto bias as long as we ensure that the gate of M 2 is of certain value, correct. So we need to ensure that gate of M 2 is of some V g q 2, some value V g q 2, right.

And what will that value be? So for this we need to ensure that there is at least some voltage across I naught, right. There should be some voltage across this current source I naught otherwise the I naught might start off and whatever that some voltage might be is a specification for the I naught. And let us assume that specification is V I naught min, right. If this is V I naught min, what will be the voltage required at V g q 2? So clearly your V g q 2 minus V I naught min will be what? Will be the threshold voltage for M 2 plus the overdrive for M 2 which means V g q 2 has to be what? It has to be at least V threshold voltage 2 plus V overdrive 2 plus V I naught min, correct. Okay, so this we already had decided and what did we decide on the on how to bias R L? I mean this is the simpler part, we can simply say that this is connected to V DD and as long as V DD is high enough we need to ensure that we can ensure that M 2 remains in saturation, right.

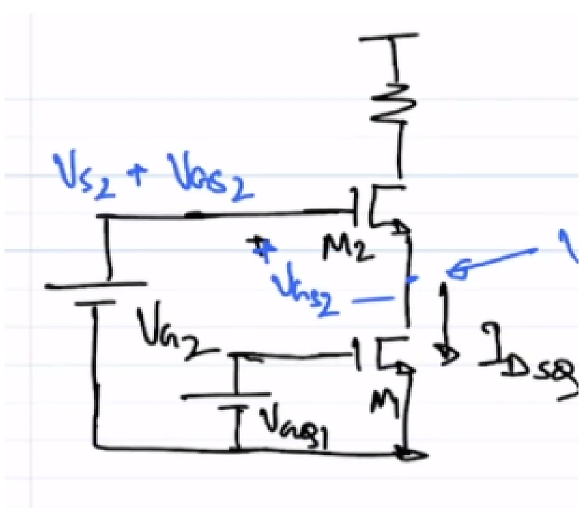
So that is the easier part because here the voltage is I naught V DD minus I naught times R L. Okay, as long as we ensure that V DD minus I naught times R L is greater than V g q 2 minus 1 threshold voltage we are good, right. So fine, so now why did I come back to this? This we had already discussed but the reason I came back to this is what is our cascode stage now? What is this I naught now? This I naught is now instead of I naught we have a transistor and what is that transistor? We have the transistor M 1, right. So let me draw that. So instead of I naught we have the transistor M 1 which is probably biased with the some voltage V g q 1.

If this transistor is in saturation what will be this current? This current will be some I naught or some I d s, I d s q, right, corresponding to I naught, corresponding to M 1, right. Okay, so then so now can you tell me what is the minimum voltage that is required to keep M 1 in saturation at this node? What is the minimum voltage? So this node let me call it V s, right, or let me call this V s 2, right, because it is the source of M 2. So let me call this V s 2. What is V s 2 min? V s 2 min will be V g q minus threshold voltage of the first transistor, right. This has to be V g q minus threshold voltage of the first transistor.

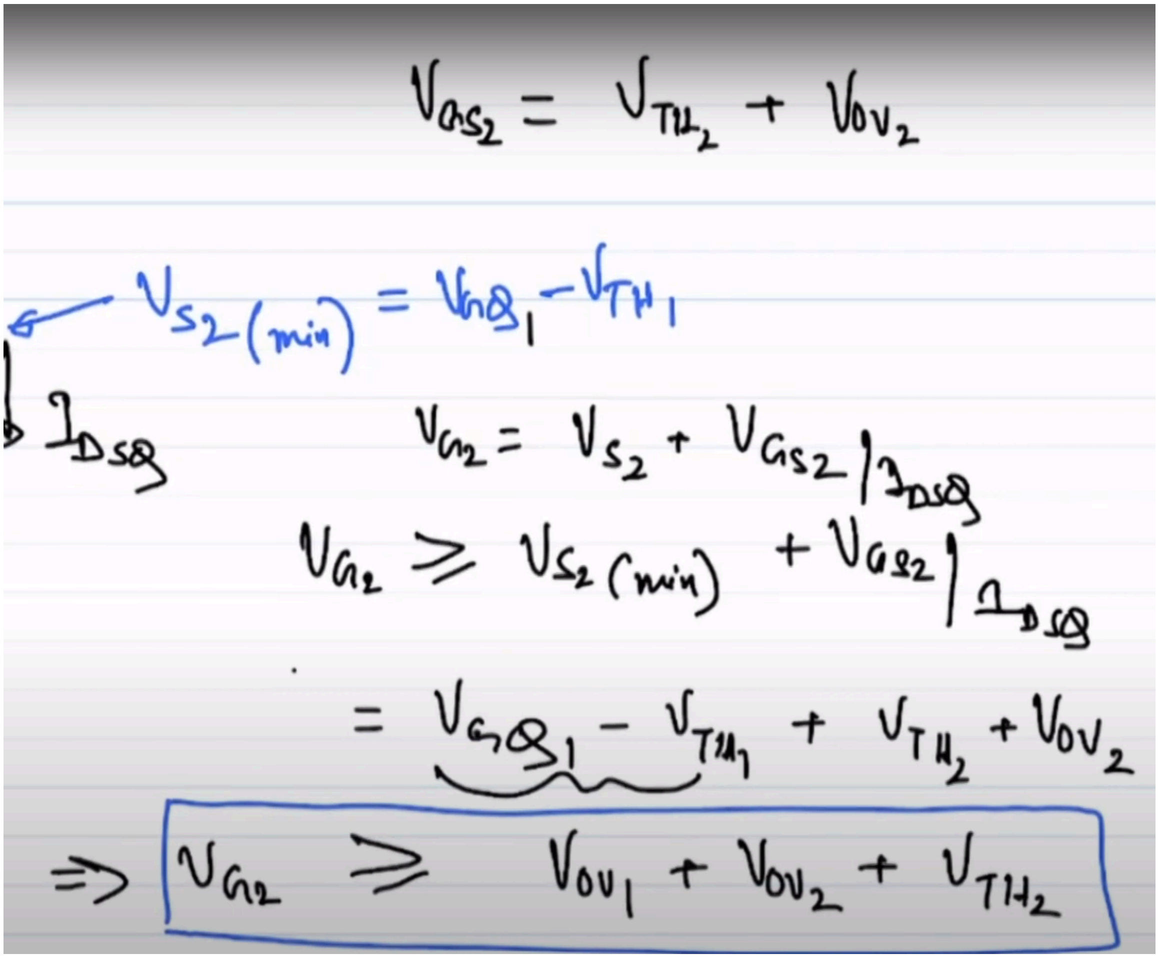
Anything above this is fine but you cannot go below this, right. Fine. So if this is the requirement, this is the requirement of V s 2, what has to be the requirement of this guy? What has to be the requirement of V g 2? V g 2 has to be 1 V g s above V s 2, right. So this, note that this voltage drop is V g s 2. So this voltage V g 2 has to be V s 2 plus V g s 2.

What is V g s 2? What is V g s 2? V g s 2 has to be equal to, this is we saw it here, right. So V g s 2 has to be equal to V threshold voltage of the second transistor plus V over drive of the second transistor. So what does V g 2 need to be? Therefore V g 2 needs to be V s 2 plus this, right. So what is V g 2? V g 2, let me write it in a different line so that it makes sense. So your V g 2 has to be, since V g 2 is V s 2 plus V g s 2, this has to be V s 2 min is V g.

So this is, so V g 2 has to be this which in other words V g 2 has to be at least greater than V g 2 has to be greater than equal to V s 2 min plus V g s 2 for a current of I d s cube, right, for a current of I d s cube, right. So this is equal to V, I just plug in the values so this becomes V g q 1 minus V threshold voltage 1 plus V g s 2 which is V threshold voltage 2 plus V over drive, correct. In other words this is equal to what? V over drive of the first transistor of M 1, right. So V over drive of the first transistor plus V over drive of the second transistor M 2 plus the threshold voltage of the second transistor, right. So means that V g 2 has to be greater than equal to this.



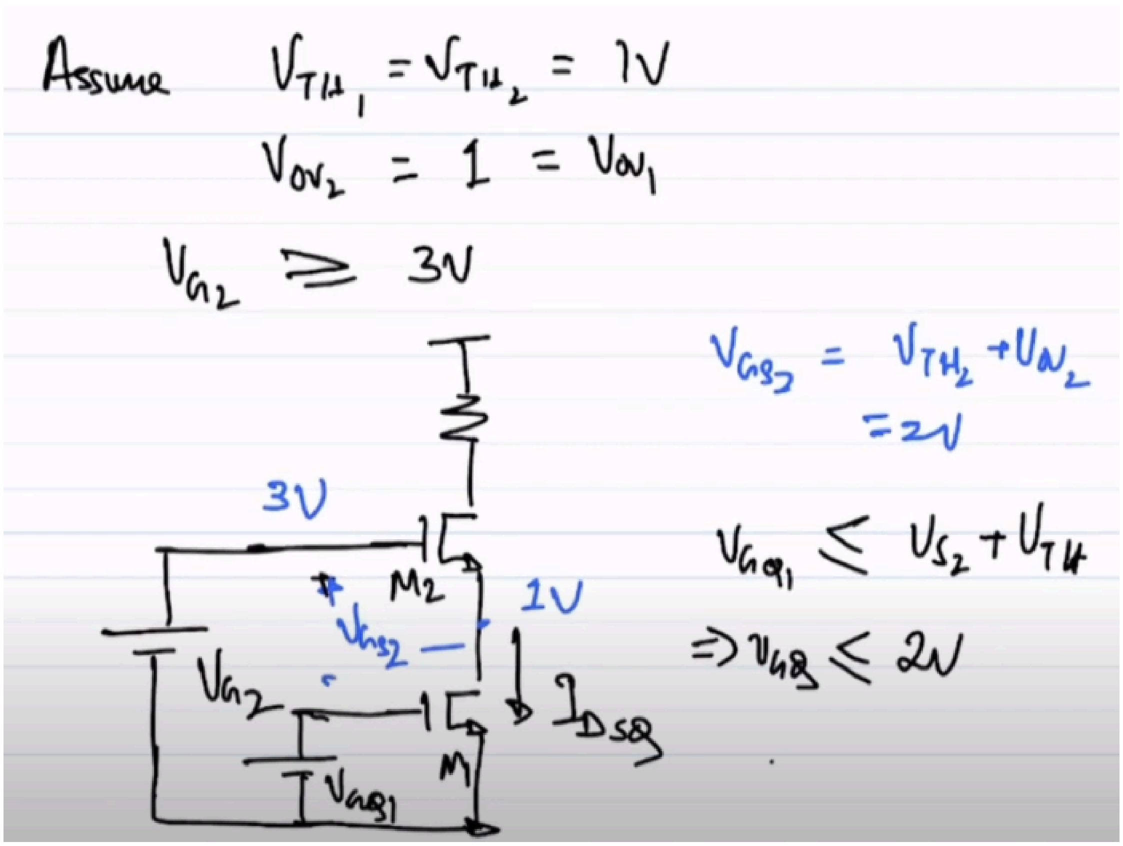
As long as we can ensure that V g 2 is greater than equal to this under quiescent state, under quiescent state at least we can ensure that the transistor M 1 is in saturation. Why do I say M 1? The reason I say M 1 is let us assume that V g 2 is lower than this value, ok. So let us assume V g 2 is lower, right. So let us assume after doing all the maths we found out that, let us assume, we found that assume threshold voltage of 1 and threshold voltage of the second transistor are 1 volt. Let us assume the over drive voltage is also 1 volt for both the transistors.



Did not be the case because note that over drive is a function of the size of the transistor But to make our life simple let us assume that the over drive of both the transistors are also equal to 1 volt, right. So if that is the case, what do you need to ensure V g 2 to be? So V g 2 should be at least greater than T o V 1, 1 volt, V o V 2, 2 volt and V th 2 is 2 volt, 1 volt which means this should be at least greater than 3 volt, correct. So what happens if let us say this is not 3 volt, so let me put the values together once more. So let us assume that, what did we assume? Let us say this is equal to 3 volt, so this is 3 volt, I could use a different color maybe, ok. If this is 3 volt, what is V g s 2? V g s 2 is 1 over drive, V g s 2 is threshold voltage of 2 plus over drive voltage of 2 which is 2 volt.

If the gate is of 3 volt, threshold voltage V g s 2 is 2 volt, what is the source of M 2? This is 1 volt. So in order to keep let us say M 1 in saturation, right, in order to keep M 1 in saturation what we need? This is something that we have discussed earlier but not in this context. So what we need? What we need V g q 1 to be? So V g q 1 has to be less than V s 2 plus 1 threshold voltage, correct? So which means this has to be implies V g q 1 has to be less than 2 volt, right? So let us assume, let us pick a number, let us put it at 2 volt. Why would pick a number? Let us put it at 2 volt.

So let us say this is 2 volt, ok. So let us remove this, ok. So now tell me, ok tell me one more thing before we proceed. What do you think has to be the value at the drain of M 2? At least it has to be greater than the drain voltage of M 2 minus 1 threshold voltage of M 2, right? So which means that this has to be at least 2 volt or higher. Let us pick a different number, let us not keep it right at the edge.



Let us say this is 2.5 volt or let us say this is 3 volt, ok. What is the drop across R L? The drop across R L is I d s q times R L, right? So that might be some value and let us assume that we have chosen V d d to have an appropriate value to keep M 2 in saturation, ok. So now let me, now tell me what is going to happen if I reduce the voltage, gate voltage of M 2 from 3 volt to let us say 2.5 volt. Ok even before that tell me what is going to happen if I increase the gate voltage of M 2 by let us say plus 100 millivolt, 0.

14 volt. What is going to happen to the circuit? Will the current in the network change? To the first order will the current in the network change? So here in you have to

understand who is setting the current in the network. So who, if the transistor, if both the transistors M 1 and M 2 are in saturation, right, if both the transistors are in saturation is I d s q likely to change? Clearly not. I mean you can neglect the effect of, you can neglect the effect of channel length modulation for the purpose of this analysis, right? So if we neglect the channel length modulation and if M 1 and M 2 are in saturation, right, so I d s q will depend on, depends solely on the T g s 1, correct? So neglecting, if we neglect channel length modulation, if C L M is neglected, right? So the current in I d s q, the current I d s q solely depends on the V g s of M 1. Why? Because the source of M 1 is grounded, you cannot change the source voltage, but the gate of the M 1 is dependent on you, you are driving the gate, right? So essentially I d s q is dependent on, is only dependent on the V g s of M 1, which means for M 2, M 1 behaves like an ideal current source. So if M 1 acts like an ideal current source for M 2, changing the gate voltage of M 2 should not change the current in that stack, correct? If changing gate voltage of M 2 does not change the current, what is the only likely scenario? The only likely scenario is the V g s of M 2 will not change, right? So essentially what I am trying to say is, if M 1 is, if M 1 and M 2 are in saturation, I d s q depends only on M 1 and not on M 2, right? Since it only depends on M 1 and not on M 2, what is the implication? The implication is, this implies V g s of M 2, that is V g s 2 is constant.

V g s 2 does not change, even if you change the gate voltage of M 2, right? So if V g s 2 does not change, what does that mean? It means essentially that if V g 2 is increased, then V g s 2 will also increase. By how much? By exactly the same amount, because if it does not increase by the same amount, right? What is going to happen? You will not have V g s 2 to be constant, right? So this since V g s 2 has to be constant due to constant current bias for M 2, right? So what is going to happen here? So now coming back to the point, if the gate of M 2 goes up by 100 millivolt, the source of M 2 also has to go up by 100 millivolt. So this will also go up by 100 millivolt. If this goes up by 100 millivolt, will the current through M 1 change, neglecting channel length modulation? If you neglect channel length modulation, if you increase the drain, if you change the drain to source voltage of a transistor, should the current change? No. One might argue that it should change now because we have been including channel length, we have been including GDS, but again, you should understand that when to neglect something and when not to.

In this case, there will be some change, but that change will be miniscule with respect to the quiescent. Since the change will be miniscule with respect to quiescent, we can neglect the miniscule change. When you are doing incremental, you cannot neglect GDS because you cannot neglect anything with respect to 0. So again, coming back to the same point, if I circle back to wherever we started, what who is setting that source voltage of M 2? Clearly, the gate voltage of M 2 is setting the source voltage of M 2.

The source voltage of M 2 is not constant. If I change, if I increase gate voltage of M 2, the source voltage of M 2 will also increase. Ok, great. So, this is all good, but what happens if I reduce the source voltage, if I go by minus 0.1 volt? By the same logic, what will happen? What will happen to the source of M 2? This will go by, this will also reduce by minus 1.

1 volt in order to keep the VGS to same. But now let us turn our attention to M 1. What do you think is a biasing condition of, what do you think is the operating condition of M 1 now when the source or the drain of M 1 or the source of M 2 has reduced by 100 millivolt? Clearly, M 1 is not in saturation anymore, right? Because now the saturation condition of M 1 is getting violated, ok, right? So, what was the saturation condition of M 1? We had to ensure this condition and this condition is no longer valid if the source voltage falls from 1 volt to 0.9 volt. So, what is the solution? You cannot really, I mean, what is the reason of this problem? This problem arose because we were biasing the transistors right at the edge. We are biasing the transistors right at the edge of saturation.

For which transistor? For right at the edge for M 1, not for M 2, right? Because the way we took the values, note that the drain of M 2 is 3 volt. For M 2 to go out of saturation, we had to increase the gate voltage of M 2 to beyond 4 volts. Then only M 2 would have gone out of saturation. But in this case, if we bias that gate of M 2 to a lower voltage than 3 volt, it seems like M 1 will go out of saturation, right? So, since this is not a viable condition, so what we need to do? We need to ensure that we do not bias it right at the edge, we have to ensure that. We have to ensure that for a proper health of the transistor M 1, we have to ensure that the gate voltage of M 2 should be higher than 3 volts.

So, this is 2 volt, right? So, this has to be then greater than 3 volt. Let us pick another value, let us pick like 3.5 volt. Because if I and this was supposed to be 3 volt, right? So, this was 3 volt. By the way, who is setting the 3 volt? This 3 volt is set by because we expect a current of I D S Q, this is V D D, right? So, this voltage is V D D minus R L times I D S Q and let us assume that we have chosen V D D and I D S Q in such a way that this is 3 volt.

If this is 3 volt, I need to ensure that the gate of M 2 is not above 4 volt. So, we chose this to be about 3.5 volt, right? If this is 3.5 volt and under the conditions of P overdrive, whatever we chose, what will be this voltage? This will be approximately 1.

5 volt. If this is 1.5 volt, what do you think is the health of M 1? Even if this guy drops by, for some reason if the voltage at M 2 drops by 100 millivolt, this will drop by 100

millivolt and still we are good, right? Now, the reason why it should drop is, we will see later, right? You can have different temperature variations, you can have non-robust biasing, all those conditions because of which the voltage at the gate of, I mean voltages at various nodes can change, but we should always keep in mind that during design, we should not make a design which is just at the edge of working, right? We need to have some margin, we need to ensure that the transistors are not biased just at the edge of cut-off or just at the edge of saturation and hence we decided to, in this case we decided to increase that voltage, I mean bias the voltage of M 2 in such a way that both M 2 and M 1 are comfortably in saturation even if things change slightly, ok? Ok. Thank you.