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So, let us now take a look into the effect of this non-zero Y2O or the non-zero PDS. Let us take the example of our good old common source amplifier. So, let us see what is going to happen. Let us say this is our common source amplifier and let us assume that it has been biased properly and all right. So, we know that floating battery is not realizable, but now we know that how to realize this floating battery using capacitors and voltage dividers right. So, let us not bother with that.

Let us say this is Vi, Vgq, Vdd, let us say this is Rd ok. So, you have some Poisson current Ids, Idsq flowing through going through the transistor ok. So, what will be the incremental model of power of this stuff? The incremental model will be input is Vi that goes to the gate Vg, the transistor is replaced with the current source of value gm times Vi right, Vm times Vgs, but in this case source is grounded. So, gm times Vi on top you have Rd, Rd is grounded, but is that it? No right now because we have a Y2 2 correct, we have a Y2 2 the new transistor model.

So, if I go back one more step, what was the old transistor model? The old transistor incremental equivalent model was this is Vg, this is Vs, this is gm times Vgs right. So, this was the incremental model for our transistor. So, this was the port 1 and this was port 2, but now the new incremental model is, so this is the old model. What is the new model? Getting channel length modulation into account with clm is input side remains as is, the output side we have gm times Vgs and we have a Y2 2 or we call this gds right. So, this becomes a new incremental model.

So, we have to use a new model here right. So, this is a gds, this is the gds and this is Rd right. So, what do you think will be the output? What do you think will be V0 over Vi? Clearly Rd and gds are in this case I should say 1 over gds because we are talking about a resistance here. So, Rd and 1 over gds come in parallel. So, essentially your V0 becomes minus gm times Vi times 1 over gds parallel Rd correct, which is which can be also be represented as minus gm times Vi by gds plus gd ok.

So, what do you think this expression is telling us? Clearly this expression is telling us that in the absence of channel length modulation if we did not consider channel length modulation, the effect would have been would have been that the gain would have been minus gm times Rd, but in this case the gain is dropping because the internal Y2 2 of the transistor right, the gds of the transistor is coming parallel to the output resistance. So, in other words the current that was coming from the gm, the current from the source is now getting divided between its own impedance and the resistance on output right. So what is the effect of channel length modulation? The effect of channel length modulation is the current gm Vi is getting let me write it fully the incremental current gm times Vi is getting divided between gds and gd this is leading to drop in the gain right. So again, so what is the if I sketch let me call this Rd s instead of calling gds let me call this Rd s because we are talking about voltages we are talking about resistances this is Vi right. So again, what is the root what is the issue? The issue is the current that is flowing out right the current that is negative current that is flowing out is now getting divided between this and this earlier the entire current was flowing into Rd and we were getting a voltage of gm times Rd times Vi minus gm times Rd times Vi in this case we are getting a lower value of voltage right.

So what is the solution now? What do you think should be the solution? So in order to lead you to the solution let me sketch this entire thing in a slightly different way then you will see that solution will probably become obvious. So let us say that this stuff over here let me call it a current source an incremental current source I in right with the internal resistance Rd s and we understand that I in is equal to gm times Vi and the resistance Rs is equal to Rd s. What is the problem statement? The problem statement is I have this non-ideal current source and I want the entire current I in to flow into RL this terminal of the RL is accessible right. So I want the entire let me yeah so I want the entire of I in to flow into RL. What happens if I directly connect? There will be a current division between RL and Rs right.

In other words RL is RL is loading the current source correct. So or rather the internal resistance Rs is loading the current source and that is why we are having a problem. So that is why the entire of I in is not flowing into RL. Again what is the problem statement? The problem statement is I need to push in this current I in the total almost the entirety of I in into RL even though there is a internal resistance to this current source. So what I am asking is, is there a contraption that I can put in here that will do the job? Obviously we have seen in the last couple of lectures few contraptions which can do the job.

So what are we looking for? We are looking to transfer the current from one port to another without any division. Essentially what do you want? We want a current controlled current source right. We want a current controlled current source or a current buffer which are the same things. We have a current buffer right an ideal current buffer input impedance is 0 right. An ideal current buffer impedance looking in is 0 right which means entirety of I in can flow in right ok.

So what is the current buffer? We have we have spent a lot of time in the last few lectures talking about CCCS, VCCS and all all sorts of current control sources. A current buffer in this case is essentially a common gate amplifier right ok. So easy way to remember this is which port of the transistor gives you low impedance the source right. So looking into the source gives you the low impedance naturally the source of some transistor should be connected to the input of the CCCS right. So in other words what am I saying? All I am saying is if this is my incremental circuit all I am saying is what to do? You have to put a current buffer.

What is a current buffer? A current buffer what is the incremental equivalent of a current buffer? Incremental equivalent of a current buffer is this where in the gate of the input gate of the current buffer is grounded and this is say this I call this S. So the current will be gm times 0 minus Vs right and obviously there will also be well I mean let us not include the gds for the time being and there will also be a resistance Rd connected to right. Now you might turn around and tell me that we know that this current buffer will be realized ultimately will be realized using a transistor. It is a common gate amplifier right it is a common gate stage. So if the transistor in the bottom does not have I mean does not have 0 gds right it has some source resistance it has some rds.

So we cannot also neglect the rds of the current buffer right. So there will be a there will be an internal resistance to this as well. So let us call this rds2 right and where will this rds2 be connected? The rds2 will be connected between the force of the transistor that is the drain of the current buffer and the source of the current buffer right. It is not that it is not between drain and ground it is between drain and source ok. So in other words what is this transistor? What is the let me draw it fresh so that we can do a proper analysis.

So what will it look like? So this should look like so you have Vi here for the original transistor. So let us call this gm1 times Vi there is an gds1 you have a current buffer on top the current buffer is the gate of the current buffer right is grounded. So this we call as Vs this will be gm2 times 0 minus Vs. Similarly you will have a gds2 and then you will have this Rd or gd connected between the top and the output side of the current buffer to the ground right and where is V0? This is the V0 that we have got. So if we do an analysis of this right so let us in order to do this analysis what is going to the V0 let us not analyze the circuit.

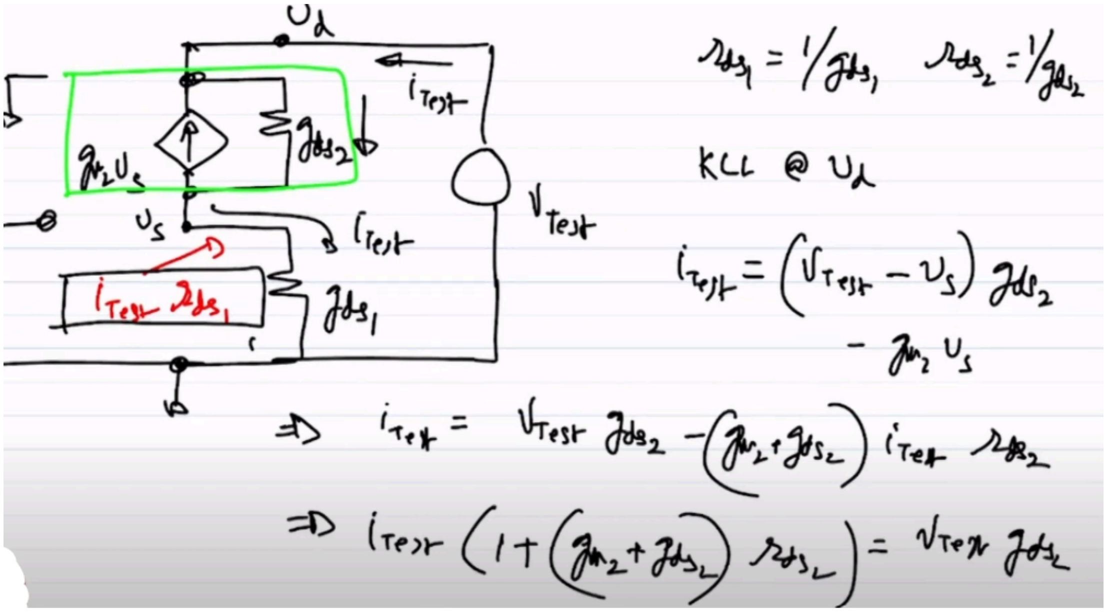
So what will be the Norton equivalent? The Norton equivalent will be output will be so

Norton so for Norton's equivalent we need to short the first in order to find out the Isc right. So what will be the Norton equivalent? We need to find out Isc let us say I need to find out Isc need to find out Rout if I find that out then I can put this Rd here and get it done right. So essentially what I am saying you have an Rd here we are trying to find out the Norton equivalent of we are trying to find out the Norton equivalent of the box looking to the looking to the left ok. So what is Isc? How will you go about figuring out Isc? Let us copy this. So what did you do to get Isc? You short output port and I will like to find out the short circuit current in which direction in the direction that in which I have marked Isc.

So in other words I am for Isc I am taking the current flowing out of Rd right from the top essentially this will be the Isc ok. Let us find out Isc. So let us do a KCL at this node. You can do a KCL at this node Vs definitely but you can do a KCL at this node Vs but a better way to approach this type of situations is to find out the impedance. So in order to do a KCL at any node you need to know what is the impedance attached to each to the node right.

So sometimes it is useful to pause before you write out the full blown equations to see is it can we ease our life by trying to figure out the impedance associated with the node first and then go ahead and apply a KCL. So what I am essentially asking is what is the impedance looking up right. In other words I am asking is what is the impedance of this guy. This is GDS2 this is gm times minus Vs where this is Vs and this is shorted. What I am saying is what is the impedance looking up.

What will you do the same old same old you apply a V test right and we find the I test and again this instead of putting minus Vs we can flip the direction of the current this becomes gmV test right. So what is the current through GDS2. This is GDS2V test. So what is I test? I test is gm plus gm2 this is gm2 plus GDS2 times V test correct. So what is the resistance looking up Rn is 1 by gm2 plus GDS2 correct.



So what is the resistance looking up here resistance looking up is 1 over gm2 plus GDS2. So in a sense I can then ease my work and say that I will replace this stuff with a resistor replace this entire contraption replace this entire contraption with this resistor right. So let us do that. So if we do that what we end up with see this becomes this remains gm times Vi gm1 times Vi this is GDS1 and we have a contraption here and the value of the resistance is or in terms of conductance if I write it is becomes gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 plus gm2 and we are trying to see what is the what is the current that is flowing into gm2 plus GDS2. Why are we interested because note that whatever current flows in whatever current flows in through into this contraption has to come out from the other side right.

So in other words what I am saying is if we know the current that is coming out of this node or going into the node I automatically know the current that is coming into that node because this stuff is a black box or red box the way I have sketched it right. So whatever current is because there is no other leakage path there is no other path in which the current can escape. So whatever current comes in from the top has to come out from the bottom or in other words whatever current is going in from the bottom has to come out from the top correct. So if that is the case right so this will be the this will be Isc correct. So what is the current that is what is Isc? So KCL at Vs and Vs will yield the current that is coming into that node Vs is gm times Vi right.

And what is current going how much of it is how so this is Isc right this is Isc. What will be Isc? Isc will be the original current gm times Vi gm1 times Vi whichever was coming into that node will be divided between two conductances the higher conductance will win in this case the ratio of the conductance will be gm2 plus gds2 by gm1 plus gds1 plus gm2 plus gds2 correct. So if we ensure gm2 plus gds2 is much much larger than gm1 plus gds1 then what happens Isc becomes approximately equal to gm1 times right. So this is the job of this is the job of a current buffer right this is the job of a current buffer where it will be able to isolate one part of the circuit from the other while transferring the current from one part of the circuit to the other right. So this becomes the Isc but what about the output resistance? So how do you how do you find out the output resistance? So for output resistance we do the same thing as we have been doing.

What will happen to the what will happen to the input? Input will be grounded right because in order to find output resistance we do not bother about we have to desensitize the input. What should we do at the output? We have to apply a test voltage and we need to find out the test current correct. So let us mark out the important aspects. So this is gm times Ti this is gds1 and since the other unit is also grounded I know this current is gm2 times ds where ds is this node and this is also gds2 correct. So let us try to figure out what will be the i test if I apply a v test right.

So if we know that what is Vi? Vi is? Vi is 0 right. Since Vi is 0 so this goes off we are only left with we are only left with this part of the circuit ok. If we further know that if since the current i test is flowing into this contraption since the current i test is flowing into this contraption whatever is coming out will also be i test. If this is i test what is Vs? What is the value of Vs? Value of Vs becomes i test times 1 over gds correct. So this becomes i test times 1 over gds or let me call it rds1 right.

So let me write it down also rds1 is 1 over gds1 similarly rds2 is 1 over gds2 ok. So Vs becomes equal to i test times rds1 correct. So now if we apply a KCL at this node right if I apply a KCL at the drain terminal right KCL at Ed what should it do? What should it imply? It should imply that the current that is flowing in i test is equal to the two other currents. What is this current? What is the current flowing through gds2? Current through gds2 is V test minus Vs times gds2 right and what is the current that is flowing up right that is gm2 times Vs. So this becomes minus gm2 times Vs correct.

But we know we already know what is Vs? Vs is equal to i test times rds1 so we can basically replace the same thing. So this becomes i test is equal to the test times gds2 minus if I take ds common this becomes gm2 plus gds2 times Vs where Vs is. Make some space here ds is i test times rds2 right. So now if I push everything alright on the other side it becomes i test 1 plus gm2 plus gm2 times rds2 is equal to V test times gds2 correct. So which essentially means t test over i test becomes 1 over gds2 times 1 plus gm2 plus gds2 times rds2.

So essentially your R out becomes 1 over gds2 is rds2 1 plus and I have made a mistake somewhere this is rds1 right this is rds i test times i ds1 rds1 correct. This is here it is gds2 no problem with that the rds1 rds1 ok. So this becomes rds2 1 plus gm2 rds1 plus gds2 times rds1 and if I remove the bracket we get rds2 plus rds1 plus gm2 rds2 times this becomes that ok. So let us sketch the network once again and have a brief look into what this actually means. So what is happening here we have rds1 here we have rds2 here and this is vs this is gm times minus vs and we are trying to find out what is the impedance looking from the top right.

So let us see whether this makes sense. So if I am trying to figure out what is the resistance from the top then it is quite natural to expect that the term of rds1 should appear that is here a term of rds2 should appear that is here right. But we are having an additional term of gm2 times rds2 times rds1. So which among these three terms do you think will dominate clearly the last term will dominate because when a transistor is biased in saturation right it is we expect the gm times the ideally see rds2 is supposed to be infinite right ideally rds2 is supposed to be infinite because the y22 is supposed to be 0 because of some non idealities because of your channel length modulation y22 will not be equal to 0 but it will be the small value right. So since we expect it to be a small y22 to be a small value we still expect rds to be a large value right. So in other words we still expect gm times rds to be much much greater than 1.

So if that is the case then we can say that this is the term that dominates right this is the term that dominates and in the absence of in the absence of the current buffer what would have been the output resistance in the absence of current buffer the output resistance only would have been rds1 but in the presence of current buffer the output impedance has increased from rds1 to this extra rds1 plus rds2 plus some additional additional resistive term which happens to be the dominant term right correct. So in essence what is the small signal equivalent or what is the Norton's equivalent of our buffer network or the current buffer network. So this is isc what was isc? isc was approximately equal to gm1 times Vi what is Rout? Rout so this I can say is approximately equal to gm2 times rds2 times rds1 right. If gm2 rds2 is much much greater than 1 that is a caveat if it's not then this is not true if this is back here then this will be true and since in the transistor bias in saturation we expect this to happen hence can say this Rout is approximately equal to gm2 times rds2 times rds1 and we have our Rd connected and we are taking the voltage across the Rd. So what is what is V0? V0 will be isc right minus isc times Rd parallel Rout which is minus gm times Vi Rd parallel this this guy rds1 times gm2 times rds2.

$$\Rightarrow \frac{V_{Test}}{i_{Test}} = \frac{1}{g_{ds_2}}\left(1 + \left(g_{m_2} + g_{ds_2}\right) r_{ds_1}\right)$$

$$\Rightarrow R_{out} = r_{ds_2}\left(1 + g_{m_2} r_{ds_1} + g_{ds_2} r_{ds_1}\right)$$

$$\Rightarrow \boxed{R_{out} = r_{ds_2} + r_{ds_1} + \left(g_{m_2} r_{ds_2}\right) r_{ds_1}}$$

Do you think the situation has improved with respect to a common source amplifier or the situation has worsened? Clearly the situation has improved because now the current division is happening between Rd and an Rout which is multiple times of rds1 in a common source amplifier right so in a CSM this would have been gm1 times Vi rds1 and then Rd. So instead of instead of rds1 now you are having an amplified version of rds1 right so this I can say this is almost equal to Rout almost I can say this is equal to some amplified version some A times rds1 note that this A is not the amplifying factor of the transistor right not the amplifier not the amplifying factor for the for the common source amplifier stage right this is some factor and that factor is let me call this A2 right so looks like instead of rds1 now you have now you have A2 times rds1 where A2 is gm2 times rds2 right since you have a higher resistance essentially this is a this contraption is a this contraption is a better current source than the contraption on the body. So in a nutshell what did we see in what did we see in today's lecture what we essentially saw was there is a non-ideality in a in a in our transistor which we have not been considering till now and the non-ideality is the output impedance of the transistor we have been considering that Y22 is 0 for our transistor but as it turns out that is not so there is a some finite non-zero Y22 which means the output impedance of the transistor is not infinite right till now we have been considering that the output impedance of the transistor is an is infinite it is an ideal voltage control current source as it turns out it is not because it has some finite output impedance. Now if you have a finite output impedance which is rds1 in this case and we want to use this contraption as a common source amplifier so naturally the entire current incremental current of gm1 times Vi will not flow into the output load that we purposefully have put but there will be a current division between between the internal impedance of the transistor that is rds1 and the output load that will drop the gain that will drop the gain of the transistor. So what is the solution the solution is to put a current buffer in between the current buffer to help the incremental current from the transistor to flow into the into the load R all right.

So if we put the current buffer in what we see we see that we are able to make the entire contraption look like a better current source because now the short circuit current remains almost the same under certain condition obviously and whereas keeping making the output output resistance output resistance higher right. So this becomes a this becomes a better current source right. So this readily gives you a first hand first hand example of the use of a current buffer in a practical circuit okay. So we will stop here in the next lecture we will see how do we actually bias this this this circuit ultimately now it has become a two transistor circuit. So we are graduated from a single transistor circuit to a two circuit two transistor circuit in order to in order to mitigate a non-ideality right.

So we will see how to bias this this network in the next lecture right okay. .