

Course name- Analog VLSI Design (108104193)
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Week- 5
Lecture- 21, module-02

Welcome back. So, up until now in the last few lectures, we have been concentrating on various topologies of a single transistor circuit with the aim of designing various control sources and we saw that our humble common source amplifier was a voltage control current source right. So, voltage control current source an example of voltage control current source was a common source amplifier right. So, let me write it write it out fully right. Then we saw a voltage-controlled voltage source with a gain of 1 right approximate gain of 1 which was common drain amplifier. Then we saw current controlled current source which had common gate amplifier right.

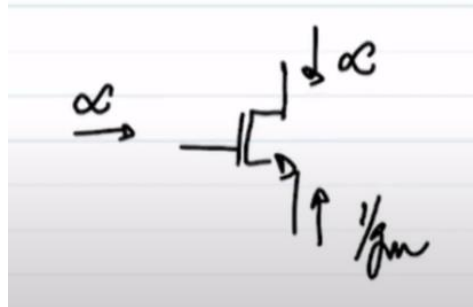
What was the what were the characteristics? Characteristics where the primary characteristics were in terms of the R_{in} and R_{out} R_{in} and R_{out} for a voltage control current source R_{in} should be high R_{out} should be low right. How high with respect to what? High with respect to R_{in} should be high with respect to the source resistance and R_{out} should be low with respect to the load resistance right. So, if I have to sketch if I have to write it appropriately I should say R_{in} should be much much greater than R_s and R_{out} should be much much less than or rather R_{in} this case is a current source right, R_{out} should be much much greater than R_L and a common source amplifier was satisfying that. What about a voltage control voltage source? In case of a voltage control voltage source, what was the requirement? The requirement was R_{in} should be much greater than R_s and however, in case since it is a voltage source which means its output resistance should be ideally 0, but 0 is not possible.

		R_{in}	R_{out}
VCCS	Common Source Amp.	$\gg R_s$	$\gg R_L$
VCVS	" Drain "	$\gg R_s$	$\ll R_L$
CCCS	" Gate "	$\ll R_s$	$\gg R_L$
CCVS	??	$\ll R_s$	$\ll R_L$

So, it should be much much lesser than R_L . In case of a current control current source I was we wanted the current input to go in without getting divided which means input resistance should have been much much lesser than R_s and it is a current source at the

output side. So, output resistance should be much much greater than R_L right. So, what other voltage sources what other control sources remain? Clearly you see that one is absent from this and that is a current controlled voltage source. What is the R_{in} and R_{out} requirement for that? It is a current control source which means R_{in} should be much lesser than R_s right ideally should be 0.

What is R_{out} ? R_{out} should be much lesser than R_L or ideally should be should be 0, but what is the topology? As it turns out if you just simply take a transistor if you just simply take a transistor and let us quickly run through why we could do the other three topologies by simply connecting the sources and the loads at certain terminals. We were able to do because the transistor has two high impedance nodes and one low impedance node right. So, a transistor biased in saturation has drain impedance to be infinity right at least that is what our model is predicting gate impedance is obviously infinity. However, the source impedance looking in is $1/g_m$ right. So, this the source is the low impedance and other two are the high impedance.



Now, when we wanted to when we wanted V_{ccs} or V_{cvs} we could as well connect in case of V_{ccs} we could we wanted two nodes of a transistor which were high impedances and that is available. In case of a V_{cvs} we wanted one node high impedance, input node high impedance, output node to be low impedance that was also possible because input node was the gate output node was the source. In case of current control voltage source we wanted the input node to be low impedance output node to be high impedance that is also possible because in input node was source and output node was drain. But now we want now you now you want a now you now you want two nodes which are of low impedance right that is the requirement of a current control voltage source and clearly we do a transistor in itself does not provide you two low impedance nodes. So, which means we have to we have to change course and we will have to think about this problem in a slightly different way.

So, that is what we will do in the rest of this lecture. So, let us see. So, before we proceed into getting into getting into how to design a current control voltage source let me take a slight amount of detool and talk about negative feedback. So, what is negative feedback? What do we understand by negative feedback? So, in a very layman term a negative feedback is a phenomena by which we observe certain output and take a corrective action

based on what the output actually is and how what the output actually should be right. Take for example, you are riding a bicycle when you are riding a bicycle you know that you have a path that you are that you are traveling right.

So, let us say you need to take a turn let us say you take need to take a turn in the road and the control knob is your handle right. So, when you are taking a turn you know the direction in which you want to go, but when you are driving the bicycle the bicycle might or might not go in the direction that you want. So, in your mind what are you doing? You are trying to figure out if there is a difference between the direction in which you want to go and the direction in which you are actually going. If there is a difference then you are taking corrective action by turning the handle right. You are taking a corrective action to turning by turning the handle and in your mind you are trying to figure out whether the difference between the actual wherever you want to go sorry wherever you want to go and the where you are going the difference between those two are getting minimized or not right.

So, in a very layman terms negative feedback means observing observe the output whatever the output might be and take corrective action based on whether the output is exp is deviating from the expected output right. So, there are three things here one you need to observe the actual output observe the actual output right you need to observe the actual output also you need an expected output because you need to know where you are going if you do not know where you are going then there is no point in taking any action. So, you need to know where you are going you need to observe where you are actually going and then based on that difference you need to take a corrective action correct. So, if we have to tabulate these if we have to tabulate this action or if you have to itemize this action what we need to what we are essentially saying we are saying that find the difference between the actual output and the expected output right. So, that is that is number 1, number 2 is use the difference information to drive the system in a direction that minimizes the difference or reduces the difference right instead of minimizes let me say reduces right.

Negative feedback.

Observe the ^{Actual} o/p and take Corrective action based on whether the o/p is deviating from the expected o/p.

- (1) Find the difference between the ACTUAL o/p and the EXPECTED o/p.
- (2) Use the difference information to drive the system in a direction that reduces the difference.

So, that is in essence how a any negative feedback system works now depending on whether it is a electrical system or mechanical system or electromechanical system or even a biological system you will have to you will have to put the system together in order to achieve this action right. So, let me show you with an example hopefully I will be able to convince you. So, let us say we want to design a current control voltage source right. So, in a current control voltage source what is the expected output firstly what is the input? Your input in a current control voltage source my input is I_{in} a current source right input is a current source I_{in} let me write input is a current source is a . In this case let me say it is a incremental current source because all these things are in incremental domain see this previous input is incremental current source I_{in} and output is expected output right this is expected output is input is I_{in} times output is a voltage right I_{in} times some constant and that constant let us say is R right.

So, it is a voltage source at the output input is that input is current output is voltage which means there has to be a change of there has to be a change there is a change in unit right. So, the proportionally constant if you have to go from current to voltage is a resistance. So, let us say this is value a resistance of value I_{in} times R right. So, we need to we need to figure this out right expected output is this is supposed to be V_{out} V_o expected ok. So, how should we arrange this? So, let us say we want to we have a voltage source rather Let us say we have a output V_o we want to ensure that is V_o effectively becomes equal to I_{in} times R and you have an R you have an I_{in} right let us say you have an I_{in} you have a current source I_{in} ok.

So, this is the expected output what is the real output real output it is obviously the output node that you are that you are observing right. So, this is the V_{out} is the actual output. So, you have to find you have to find a difference between the real output and the expected output. So, how do you find a difference R_{in} other words yeah. So, how do you find a difference we need to find a difference.

So, difference voltage is what? Difference voltage is equal to V_o minus V_o expected right which is V_o minus I_{in} times R . Let me call this V_{error} because this V_{error} it it by I mean instead of writing difference voltage all the time we let us call it something I call it error V_{error} why am I calling it V_{error} I am calling it V_{error} because ultimately what is the goal the goal is to make V_o is equal to I_{in} times R if we are achieve if we achieve the goal successfully then what will be this error voltage the error voltage will go to 0 and if it does not go to 0 what what what is it implying it is essentially implying that we have not been able to successfully make a current control voltage source which is supposed to give a output of I_{in} times R that is all it is saying right hence the nomenclature error. So, ideally we should we should arrange our circuit in such a way that the error voltage goes to 0 fine. So, first which means that we need to we need to so let me also write it down arrange a

circuit such that V_e tends to 0 ok. So, then I mean if we have to arrange something to make V_e tends to 0 then obviously we will have to ensure that we will have to ensure that we first generate V_e .

So, how do you generate V_e if you have V_o you have I_{in} you want V_e V_e is V_o minus I_{in} times R it is pretty simple what you do you you drag out a current of I_{in} from V_o through a current through a resistance R right. So, if I simply do this what will be this voltage this voltage will be V_o minus I_{in} times R which is V_e ok. So, what do we need to do again let me remind you of the other fact that a current control voltage source or rather when we have this I_{in} right when we have this I_{in} this I_{in} might have an R_s if we have a proper current control voltage source this relation should hold even if you have an R_s that is the whole purpose of putting a current control voltage source right. If we just simply pull I_{in} push I_{in} into R I will always get an output voltage which is equal to I_{in} times R , but that is not the goal because if we have if we do that then I am then the output voltage is susceptible to the source resistance R_s and precisely we do not want that that is why the input resistance has to be much less than R_s right. So, anyhow so let us we will come back to this discussion point in shortly, but for the time being let us try to design a circuit in which we can arrange a circuit in such a way once we have a V_e we need to drive the output in such a way V_e tends to 0 ok.

So, what should we do let us think about it. So, let us assume that V_e is not 0 right let us say V_e is positive right if V_e is positive ok. Let me say if V_e is increasing right if V_e is increasing what is it telling us if V_e is increasing what is it telling us it is essentially telling us that the current that I am drawing out right the current that I am drawing out from V_o is not sufficient right that is what I am being told if V_e is increasing which means which means the current that I am drawing out of V_o is not sufficient I have to increase the current that I am drawing out of V_o right if I increase the current that I am drawing out of V_o then I will be it is likely that I will be reducing the voltage at V_o right if I pull current out of a node the node the node voltage reduces ok. So, now, one might say that I already have a current source I_{in} . So, should I increase I_{in} I cannot do that because I_{in} is not in our control right I_{in} is a source that has been given to you by it is an independent source you cannot go and control it. So, what we need here we need a dependent source because we are taking we should be taking a directive action based on the information of V_e not if V_e is increasing then draw current out of V_o right if V_e is increasing draw current out of V_o right.

Similarly, if V_e is decreasing what should we do we should push current into V_o right. So, let us let us let us stick to the V_e is increasing case. So, if V_e is increasing we need to draw current out of V_o . So, so what is the action attempts that I am interested in input what to whatever stuff that I put here I have to put something here. So, that if V_e increases I draw current out right if V_e increases I draw current out of V_o correct.

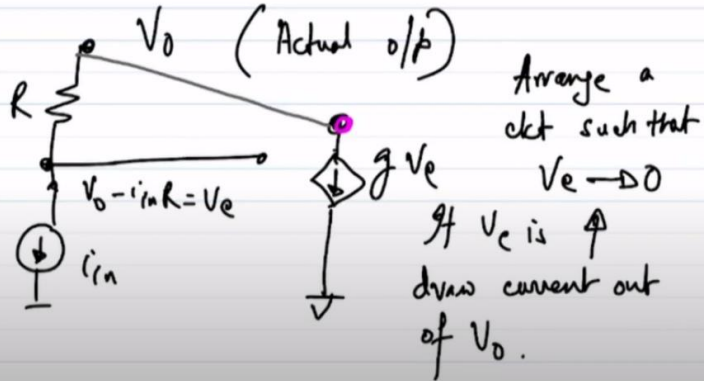
In a CCVS i/p is incremental current source, i_{in}

$$\text{Expected o/p} = \boxed{i_{in} R = V_{o \text{ expected}}}$$

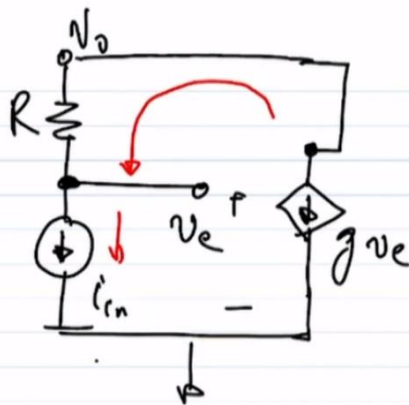
Difference voltage

$$= V_o - V_{o \text{ expected}}$$

$$= \boxed{V_o - i_{in} R = V_e}$$



So, essentially we want an incremental voltage control current source right we need a incremental voltage control current source right. So, so let us put that let us put an arbitrary voltage control current source then we will see whether it is realizable or not right. So, let us see let us say we put a voltage control current source right and let us say this voltage control current source has a proportionally constant let us say some g like some g times V_e . So, if V_e is increasing in the that and the way I have drawn I am drawing current out of I am drawing current out of this node what is the requirement if V increasing V increases I should draw current out of V_o what should I do I can simply connect these two these two terminals right let me draw it in a next page in a cleaner manner. So, what I am essentially saying is this.



$$gV_e = i_{in} \Rightarrow V_e = i_{in}/g$$

KCL @ v_e

$$i_{in} = \frac{V_o - V_e}{R}$$

$$\Rightarrow V_o = i_{in} R + V_e$$

$$\Rightarrow \boxed{V_o = i_{in} \left(R + \frac{1}{g} \right)}$$

$$\text{If } \frac{1}{g} \ll R \text{ i.e. } g \gg \frac{1}{R}$$

$$\text{then } \boxed{V_o \approx i_{in} R}$$

So, this is i_{in} . So, this is g times V_e this is V_e and I need to connect V_o to the top terminal

of the voltage control current source right ok. So, so this seems to be this seems to be the logic right. So, let us run through the logic once again what is this telling you this is telling us that if V_e increases I am pulling current out of V_o and if V_e decreases I am pushing current into V_o right this is all incremental. So, I should actually use a small notation right. So, that was a mistake let me use a small notation here g times V_e ok.

So, let us see let us see if this satisfies our case of firstly what is the thing that we need to see we need to see whether what is the input and output relation that is the first thing what is the second thing you need to see we need to check whether we are able to satisfy the input output resistance criteria as well right. So, what is V_o ? So, let us let us write KCL let us write KCL at which node would you like to write KCL at. So, let us let us write KCL at V_e . So, what is I_{in} what is the direction of I_{in} I_{in} is this this is I_{in} where is I_{in} flowing out from there is only one loop.

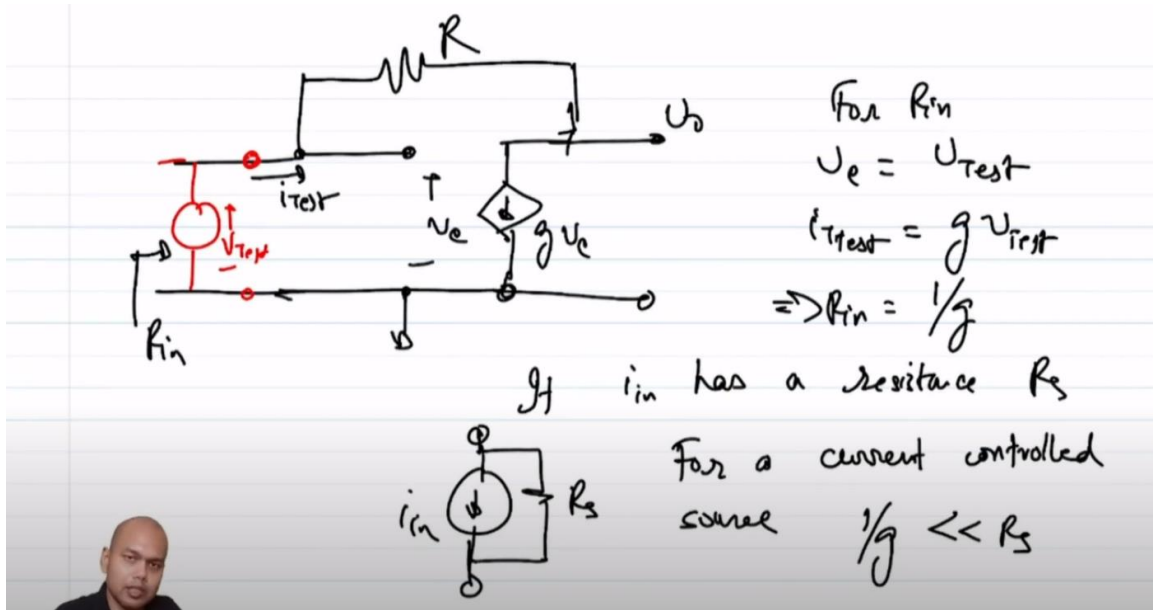
So, I_{in} is flowing this loop. So, what is g times V_e . So, g times V_e is equal to I_{in} which means V_e is equal to I_{in} over g right right. So, KCL at V_e what does it give what do we get we get I_{in} is equal to V_o minus V_e over R right which means V_o will be equal to I_{in} times R plus V_e which means this is equal to I_{in} times R plus 1 over g . So, this becomes V_o what did we want we wanted V_o to be equal to I_{in} times R , but we have a extra factor. So, but note that this g is in our control because we have put it right it is not it does not come with the with the with the source or the load information right.

So, if g is much much greater than R sorry if 1 over g g if g is much much greater than or rather Let me in this write in this way if 1 over g is much much less than R I e g is much much greater than 1 over 1 over R then V_o seems to be equal to I_{in} times R this is approximately equal to I_{in} times R then it looks like this can mimic our voltage control current source, but hold on we have not yet established whether the input output resistance criteria are satisfied right. So, let us do that next R this is I_{in} this is R this is I_{in} this is g times V_e where this is V_e right. So, this is this is my V_o . So, let us say I put the I_{in} here. So, that I can understand where the ports are right let us let me use a different color for the input I_{in} .

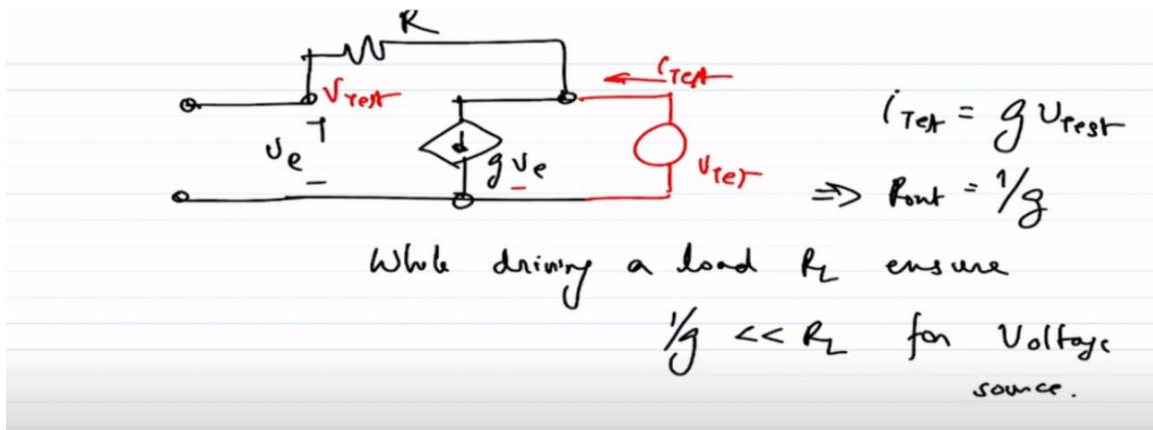
So, this is the port input port and this is the output port this is this is the R correct ok. So, what is the input impedance what we need to do in order to find out input impedance. So, for R_{in} we have to find impedance firstly we have to desensitize all the sources right. If you have to de energize I_{in} which means you set I_{in} to be 0 if I_{in} to be 0 then the current source goes off current source going off means it is an open circuit.

So, this is what your network is. Now, you have to find out the input and the output impedance what do you think is the input impedance what is R_{in} how will you find R_{in}

for R_{in} again you do the same old same old we apply a test voltage right you apply a test voltage and then you go around and find out what the test current is what is the what is the test current in this case you have again you have a single loop in this case V_e becomes equal to V_{test} right for R_{in} V_e is equal to V_{test} which means this current right which means I_{test} whatever is the I_{test} will be equal to G times V_{test} which means R_{in} will be equal to 1 over G ok.

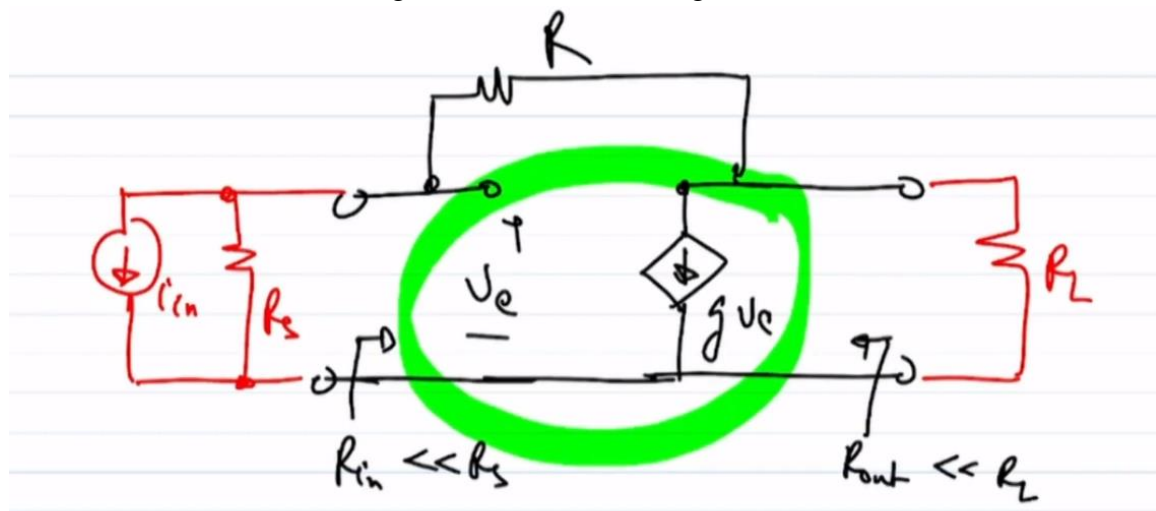


So, if the volt if the current source has a resistance R_s right if the current source has a if i_{in} has a resistance R_s that is if i_{in} comes with a resistance R_s for a for a current control source we need to ensure 1 by G is much much less than R_s right again note that this is in our control because this contraption is something that we have put in. So, what about the output impedance what will you do to find out the output impedance same old same old. So, again the source does not play a part because i_{in} goes to 0 this is what we are left with this is $V_e G$ times V_e we apply a test voltage at the output terminal we find out what is I_{test} right. So, clearly that no current flows here because other side is ground open.



So, this terminal becomes V_{test} which means G times V_e becomes I_{test} I mean this is the entire I_{test} . So, which essentially means I_{test} is equal to G G times V_{test} which means R_{out} also is equal to 1 over G which essentially means that if we have an R_L while driving a load R_L ensure 1 over G is much much less than R_L for voltage source correct. So, what does our final incremental model look like in the presence of sources and loads this is what it looks like. So, let me draw the contraption first. So, this is V_e this is G times V_e this is R these to go out this is the input I_{in} with a source resistance R_S and this is R_L right.

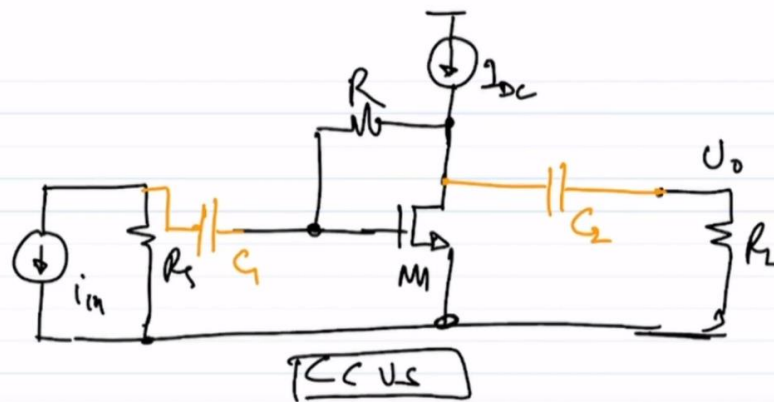
So, this will behave like a voltage control sorry this will behave like a current control voltage source right. If we honor two conditions one is in this particular case in this particular contraption what do we need to honor we need to honor R_{in} should be much less than R_S and R_{out} should be much less than R_L . Now, note that if we do the full blown analysis in the presence of both R_S and R_L in the presence of both R_S and R_L the conditions that you will get will not be exactly equal to this right. So, this is these conditions of R_{out} and R_{in} that I have derived is under the condition that only either R_S or R_L is present. So, if you do the calculations in this case in the presence of R_S and R_L you will get a slightly different result, but nevertheless it is still in your control to ensure that this circuit can behave like a voltage current control voltage source.



So, now, we I mean now you should readily recognize what is this contraption what is this contraption G times V_e this clearly is a MOSFET right what is that G that G_m is the transconductance of the MOSFET. So, now, let us replace the incremental model with its with this full blown equivalent. So, this becomes again this is I_{in} this is R_S right and we have R_L and instead of G times V_e we have to put a MOSFET, but this ground this is source source is grounded right. So, it is rounded we have a resistance between the drain right. So, this let me mark the terminals here this should be the drain this should be the source this should be the gate correct.

So, we have a resistance between drain and the gate correct. So, we have a resistance

between the drain and the gate and then we will have to ensure that the inputs are also connected right. So, how do you want to connect the input I mean we would like to connect the input I mean the same way as we have been doing we would like to connect the input through AC coupling capacitor. So, let us say we put a coupling capacitor here right let us say C_1 it is a coupling capacitor here let us say C_2 right this is R , but I mean you might be now screaming at me saying that how have I biased the transistor M_1 this is clearly not biased because what is its gate to source voltage what is the current flowing through it clearly nothing right the gate to source voltage is not applied it is 0 in this case right. So, what should I do I can simply put a current source right we can put a current source bias where do we want to put in this case it seems like since I already have a connection between the drain and the gate right the connection between drain and the gate is already established the easiest thing to do will probably be to mimic that condition in which we observe the drain and feedback at the gate right.



Find the constraints on the sizes of C_1 and C_2 and also the swing limits of the i_{in} if $i_{in} = I_p \sin(\omega t)$

So, this can be the IDC bias ok. So, this will be you know V_o ok. So, what I would request you to do this because so this essentially becomes my full blown current control voltage source with biasing in picture what I will request you to do is find the constraints on the sizes of C_1 and C_2 and also the swing limits of i_{in} if i_{in} is equal to $I_p \sin \omega t$ ok. So, I mean this will be your assignment for the week this will be one of the assignments for the week it might be instructive to go through it on your own right ok. I will see you in the next class. .