Course name- Analog VLSI Design (108104193)
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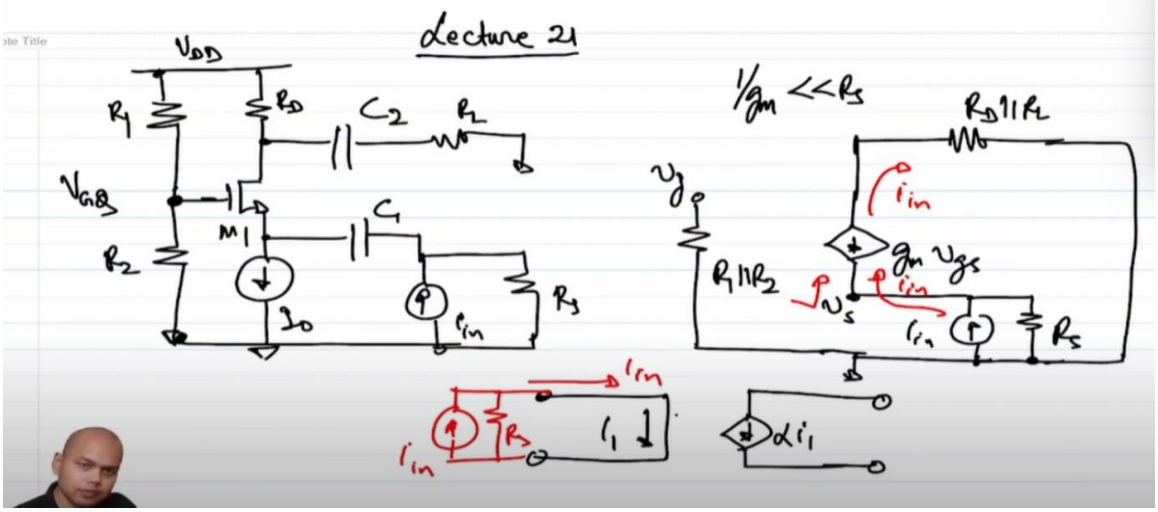
Week- 5
Lecture- 21, module-01

Welcome back, this is lecture 21. So, in the previous lecture we were doing we were looking into when we ended the previous lecture we were looking into a topology of common gate amplifier or in other words we are looking into a topology where we could get a current input and we were able to get a current output by that what we essentially meant was that we wanted a current control current source right. So, what was the topology that we ended up with? So, the transistor is biased with a constant current source, the gate is biased with some R1 R2 where the input DC voltage at the gate the DC voltage at the gate is Vgq. We have a sinusoidal voltage. So, the current source with some source resistance Rs and I would like to we would like to ensure that what would you like to ensure? We would like to ensure that all of this Rin, Iin flows out of the transistor and flows into the load right. So, what was the load? The load is as usual connected with a capacitor which is C2.

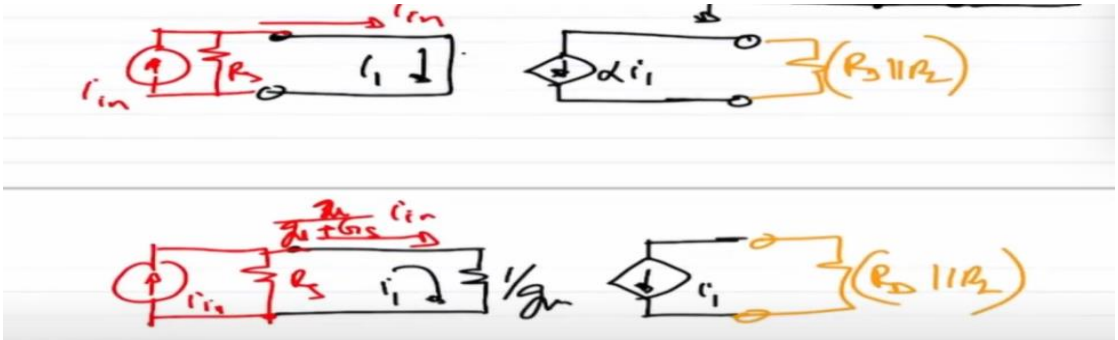
So, this is Rd this is Rl and the input was as usual connected through a capacitor C1 right and what did we these are connected obviously and what did we conclude? We concluded that in order to ensure that all of Iin we can as well reverse the polarity of Iin because this is incremental reversing the polarity will help with the analysis to some extent. What we need to ensure? We were trying to ensure that all of this Iin flows into M1 right flows into the source of M1 because Iin has two places to go, Iin can go here or Iin can go into M1 right. Mind you when I am saying that Iin can go to the right or the left I am I am citing the incremental picture of the topology. So, incrementally what we have? We have we have the MOSFET whose gate is connected to ground right through resistance of R1 parallel R 2 this is Vg this current source Io is open circuited in the in the incremental sense assuming C1 has been sized to be short circuited at the signal frequencies.

So, we essentially have this and this is gm times Vgs where Vs is the source voltage and on top we have a combination of Rd parallel Rl and this obviously is grounded. So, we wanted all of Iin to flow into flow into the gm for that we saw that we are needed to ensure that 1 over gm has to be much lesser than Rs because the resistance looking up the resistance looking up into the source is 1 over gm. So, as long as we ensure that 1 over gm is much lesser than Rs all of Iin would like to flow into the low impedance path that is into the 1 over gm. Now, if Iin flows into the low impedance path then obviously the only way it can come out is through the top of the transistor and it will flow into Rd parallel Rd right.

So, if 1 over if this condition is satisfied then the current that will go in will be Iin and the current that will come out from the other side will also be Iin.



So, hence we were able to isolate the load resistance Rd from Rs and we are able to buffer we were able to buffer the current between the load and the source right. So, in a in the classic topology so, let me write this condition here right. So, a ideal current control current a current buffer has a as this as its input has this as its incremental model that is if the input if this current is I1 the current at the other port will be some alpha times I1 right, but in our so that so that even if you have a even if you have a non ideal current source of Iin and Rs all the current will flow into Iin right this is ideally. However, in our case in our case what we have in our case obviously, here we also have Rd parallel Rl in our case what we have in our case we do not have the input to be short circuited in our case input is input impedance is 1 over gm. Now, in the presence of Iin and Rs what amount of current will flow into 1 over gm the amount of current that will flow in will be will be gm by gm plus gs times Iin where gs is 1 over Rs and this current is getting buffered and this buffering factor is 1.



So, if this is I1 this is I1 and the output is flowing into Rd parallel Rl right. So, this essentially is what is happening in the incremental feature in the circuit on the top. So, now, we while we ended the previous lecture I had requested you to find out if Iin is a sinusoidal waveform right if Iin is equal to Ip sin omega naught t. So, let us see say if Iin is equal to Ip sin omega naught t what will be the what will be the constraint on Ip correct. So, what I

am essentially saying is this Iin is a sinusoid.

So, let me draw it somewhere else. So, say this Iin is a sinusoid while going while going up it goes up to Ip while going down it goes down to minus Ip ok. So, let us do the going up first. So, what is happening when the current through Iin is increasing? So, what should we do we should we should first try to try to intuitively see what is happening if Iin is increasing because the transistor M1 we have to ensure that the transistor M1 stays in saturation and away from cut off. So, now, what do you think if Iin is increasing in the direction shown what is going to happen? If Iin is increasing you are pushing in you are pushing in current into the node into the source.

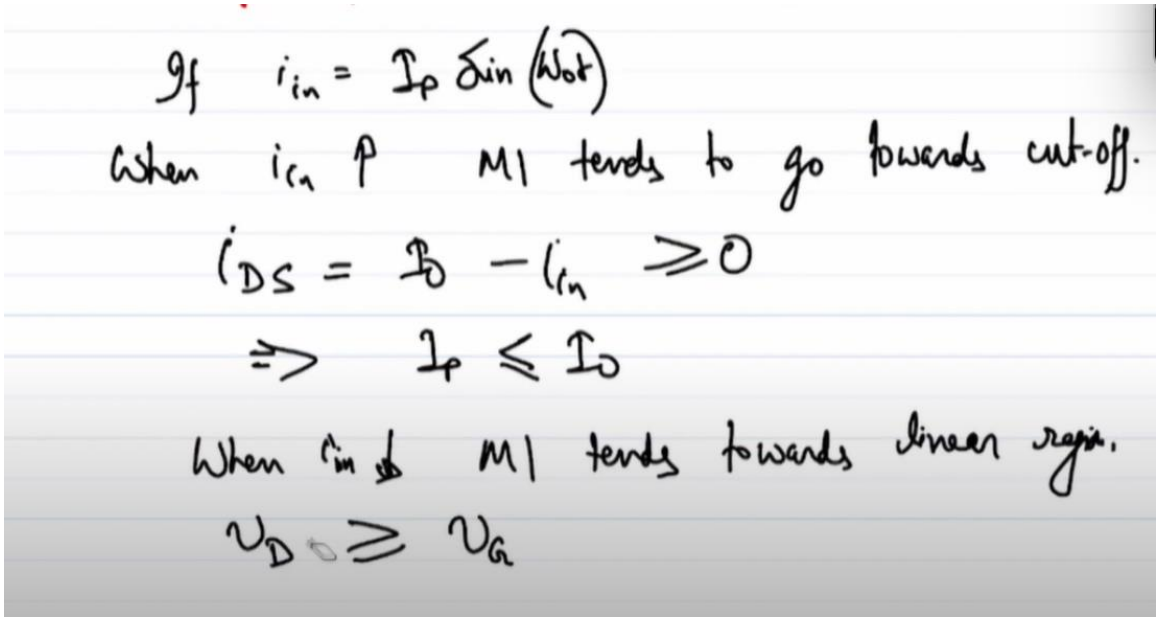
So, what happens if you push in current into the source? The source voltage is bound to rise right if the source voltage rises what is going to happen what do you think is the transistor going into going into going out of saturation or into cut off? Clearly if the source voltage is increasing then the gate to source voltage is decreasing if the gate to source voltage is decreasing which means the transistor is going towards cut off. Now, you might also want to check what is happening at the drain. So, the so if Iin is increasing the increased current the increased current where is it flowing that increased current is flowing into the drain right the increased current is flowing into the drain and it is also increasing the voltage at the drain. So, the voltage at the drain increases then clearly the transistor is going is comfortably in saturation. So, we do not have to worry about the saturation condition, but we have to worry about the cut off condition.

So, what is the criteria for cut off condition we need to satisfy? We need to ensure that the total Ids is always greater than 0. So, what is total Ids for cut off? So, let me say when Iincreases M1 tends to go towards cut off fine. So, in this case what we need to see we need to see what is Ids. What is Ids? Ids is a quiescent current plus the incremental current. What is quiescent current? Quiescent current is Io correct right and what is the incremental current? The incremental current from where am I getting the incremental current I am getting from this picture right on the picture on the right.

So, incremental current is clearly Iin under the assumption that 1 over gm is much less than Rs right. So, but incremental current is Iin in which direction is it positive or negative? It is obviously, going in right. So, with respect to the direction of Io it will be negative. So, which means Ids will be Io minus Iin correct. So, this has to be greater than equal to 0 which means that worst case condition is Ip has to be less than equal to Io right.

So, this is the cut off condition for Ip right. So, if you want if you are trying to design a circuit for which you would want to ensure that a lot of Iin has a very high large amplitude without pushing the transistor into saturation then what you need to do? You need to ensure

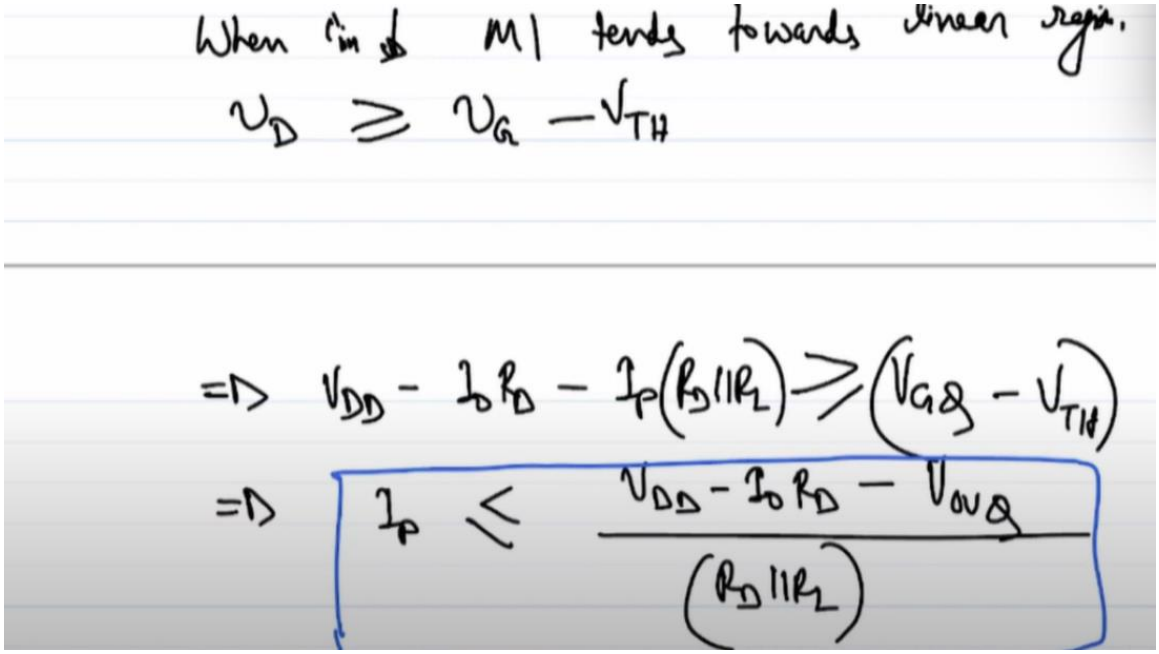
that the transistor is biased with a larger current right ok. So, if now let us say the other way other condition when Iin is decreasing what is happening? So, let us look at the transistor once again if Iin is decreasing that is Iin going negative if Iin is going negative what is happening? So, let us if Iin is going negative which means I am drawing current out right. So, I am drawing current out of the source if I am drawing current out of the source what is happening to the source voltage? Source voltage is decreasing this current is also being drawn out from the drain since the current I am drawing out from I am drawing the current out from drain what is going to happen to the drain voltage? Really the drain voltage is dropping which means the transistor is going towards linear region right. So, we see this we find out the same constant we find out the constant for the linear region case.



So, when I when Iin is droppingm1 tends towards linear region ok. So, what is the condition then? The condition is total Vds has to be greater than equal to total I do not have to bother about source the total Vds should be greater than total gate minus 1 threshold voltage total voltage at the gate minus a threshold voltage. So, what is the total voltage at the drain? Total voltage at the drain was the quiescent voltage plus incremental what was quiescent? Quiescent was Vdd minus Io times Rd right. So, let us check whether that is indeed correct right yeah. So, the voltage here was Vdd minus Io times Rd because Io was flowing through through Rd ok.

What about the incremental what is the incremental part for the drain voltage? So, clearly if Iin is if 1 over gm is much lesser than Rs again all of Iin is flowing out of that node right. Since all of Iin is flowing out of that node what is the incremental voltage at this node? The incremental voltage at this node will be minus Iin times Rd parallel Rl right when Iin is flowing out. So, I should also make a note here assuming 1 over gm is much much lesser than Rs. Similarly, if we make the same assumption then the voltage at the drain will be Vd quiescent voltage minus Iin or let me simply write Ip because this will be worst case in

case of when Ip when the Iin is at it is at its negative half cycle peak of the negative half cycle. So, Vdd minus Id Io Rd minus Ip times Rd parallel Rl should be greater than equal to total Vg.



What is total Vg? Total Vg is the quiescent Vg, quiescent Vg is Vgq right. So, this is Vg q. What is the incremental Vg? Clearly incremental Vg is 0 because no excitation has been applied at the gate right minus 1 threshold voltage which means what? Which means Ip has to be less than equal to Vdd minus Io Rd right minus V overdrive quiescent because this stuff was V overdrive quiescent divided by divided by Rd parallel R l right. So, which essentially means that you have 2 constraints you have I mean like before you have 1 constraint here and you have 1 constraint here. If Ip is supposed to be a if I n is supposed to be a sinusoidal current source then the worst of these 2 constraints right will determine the amplitude because you would neither want the transistor to go out of linear region or into cut off right.

Whichever is minimum of these 2 will determine whether the transistor actually is in proper operating condition or not right. .