Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 7
Lecture- 20 Module-02

Welcome back. So, till now we have seen two contraptions, one is a common source amplifier, one is a common drain amplifier. Another way of explaining those two contraptions or another way of going about is going about relating these contraptions with the control sources that we already know as the following that a common source amplifier has let us say I talk about input impedance and output impedance. Say common source amplifier, what is the input impedance that you see in a common source amplifier without taking the source and the load into account, then input impedance is infinite or rather I can say it tends to infinite. What is the output resistance of the common source amplifier? So, let me write it out as common source. What is output resistance? Output resistance without excluding the load RL that is looking into the drain of the transistor the output resistance is also tends to infinite or in this case is infinite.

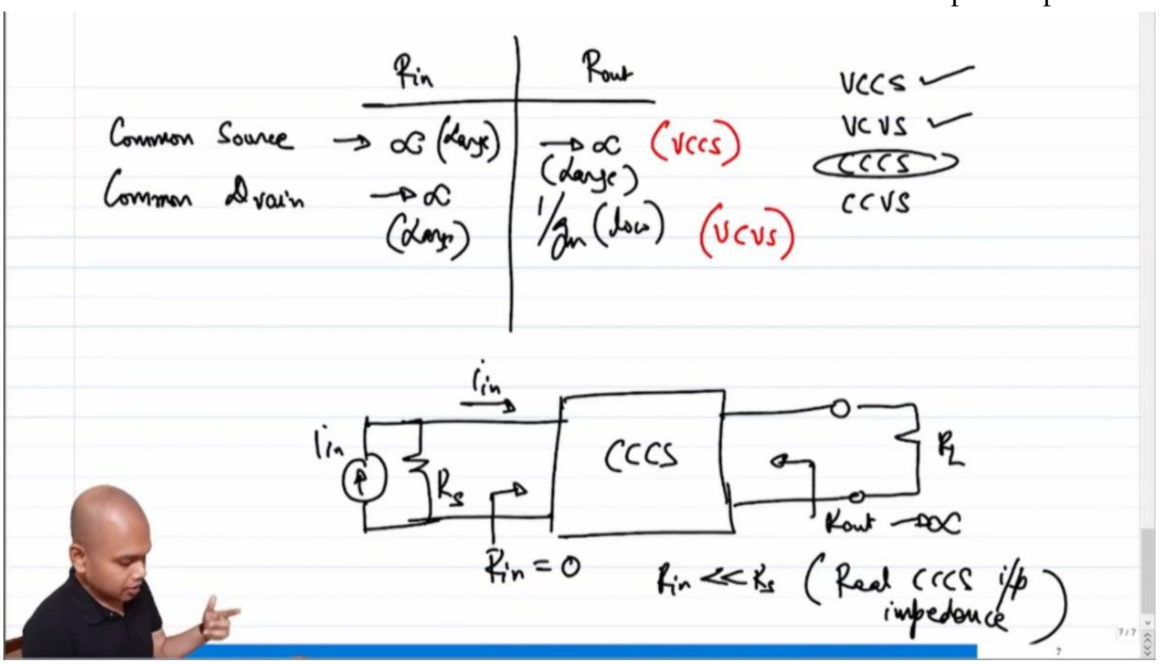
So, among the control sources that you are aware of, what are the control sources that you are aware of? We are aware of voltage control current source, voltage control voltage source, current control current source and current control voltage source. Which of these four do you think a common source amplifier classifies into? Clearly, it is a voltage control current source right. This voltage control means input port is infinite impedance, its current source means output port is of infinite impedance. So, this all some of the category of VCCS.

What is our common drain amplifier? Which category does it fall into? What is Rin? Rin again tends to infinity right, because we are looking into the gate of the transistor one might say it is R1 parallel R2, but I mean that is also in our control. We can say Rin tends to infinity or if you are not comfortable infinity we can say that Rin is high right. In this case also RHout was high or large. Again mind you large, small, high, low these are all relative quantities with respect to what? With respect to the load that is attached. So, what about the output impedance in a common drain amplifier? Output impedance is 1 over gm which is low right with respect to the load is low.

So, input impedance is large output impedance is small. What do you think this configuration classifies into? I mean we have talked about this, this clearly is a voltage control voltage source with a maximum gain of unity right ok. But now let us so this is ticked off, this is ticked off. Let us try to see if we can attack this, if we can attack current control current source. So, in a current control current source what do you think the input impedance has to be? In a current control when you say current control source which means the input should be able to take in any current right which means that assumption is that if you have a CCCS assumption is that if I have a current source let us say I have a non-ideal current source.

By non-ideal current source I mean there is an internal resistance. So, if I connect this current source to the CCCS block all of this current Iin let us say in this case Iin should flow into CCCS right. It is only when the Iin flows it becomes a controlling variable it is a current is a controlling variable. If nothing flows in then I mean there is no point in calling a block current control block because it has to be able to accept current in at its input port right. So, if it accepts the current in the input port in the presence of a non-ideal resistance R s what can you comment on the input resistance? Rin has to be close to 0 in this case Iin has to be 0.

It is only when Rin is equal to 0 all of Iin will flow into the current control current source input port and no current will flow into Rs. If Iin is not 0 right then some current division will happen some portion of the current will flow into the input port and some portion will go into Rs. So, in a real current control current source what do we need to have? We need to have Rin to be much much less than Rs. This is real CCCS input impedance.



Ok. What about the output side? It is a current source at the output side it is a current source which means output impedance has to be large right should be infinite right. So, in a current control current source the input side has to be of low impedance output side has to be of high impedance. So, if that is the scenario and we would like to make a current control current source using a MOS transistor right. So, what do you think will be our architecture from the perspective of looking into the impedances right. So, a MOS transistor has as we know it has 3 terminals right.

We have gate, drain and source. Among these 3 terminals only 2 terminals can take in a current input. The current cannot go into the gate. So, there is no point in considering that as one of the input terminals for a current control current source right. So, which terminal can be used? So, I can say I have a non-ideal.

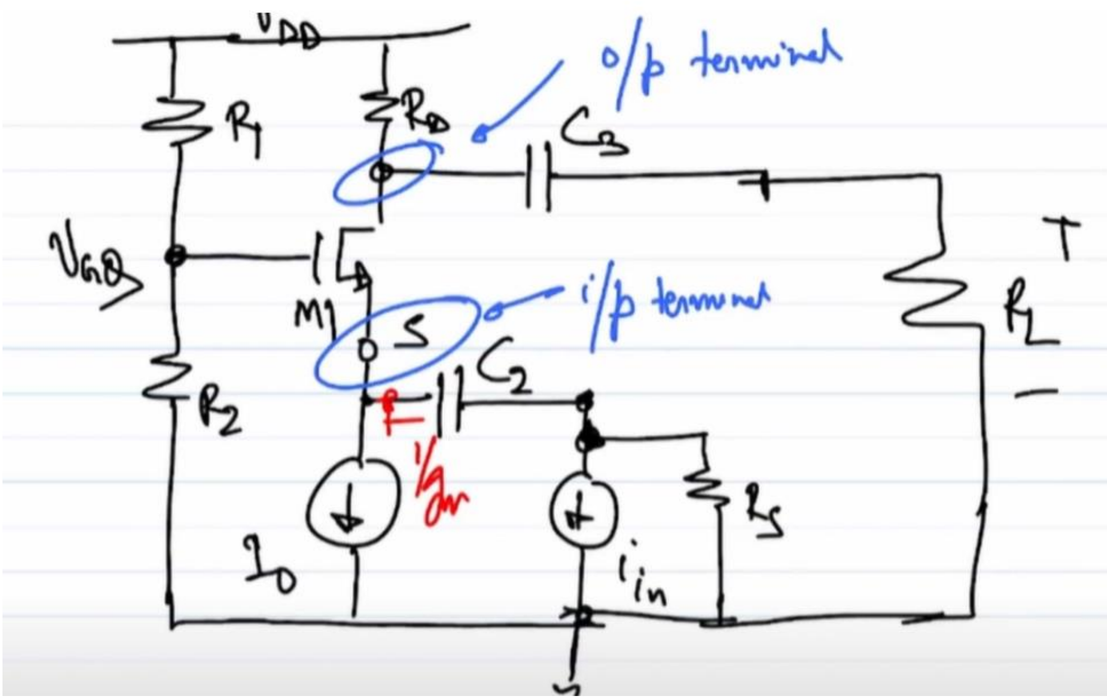
Let us say I have a non-ideal current source, incremental current source. Let us say Iin with a resistance internal resistance Rs and these are the 2 ports coming out of the current source. Where do you think should I connect this current source? Should I connect it to the drain? What is the impedance looking in? What I am essentially asking in this CCCS topology the looking in terminal can this be a drain terminal or can this be a source terminal? So, what is the looking in impedance into the drain if the transistor is biased in saturation looking in impedance is infinity right. Because it is Y22 at the drain terminal is 0. What is the looking in impedance into the source? What we saw looking in impedance into the source was 1 over gm 1 over the transconductance of the transistor and by definition we would like 1 the transconductance of the transistors to be as large as possible which means we would like to which means naturally the impedance looking into the source becomes smaller right.

So, if that is the case where do you think we should connect we should connect our control source we should definitely then connect this control not the control source where should we connect this non-ideal current source we should connect it to the should connect it to the source of the of the transistor m1 ok. We should connect it to the source of the transistor source of m1 but again you should at this point turn around and tell me that this you told me this is an incremental current source how can I just take in an incremental current source and you would be absolutely right. First we have to establish the transistor is biased in saturation right. Without the transistor being biased in saturation nothing can be done correct. So, let us bias the transistor first right.

So, let us bias the transistor first and then we will then we will see what can be done. So, let us put it inside for the time being. So, how do I bias a transistor? So, let us take our one of our favorite ways of biasing put a current source at the drain or a put a current source at the source. In this case since I would like to connect the increment current source to the source the source cannot be bounded which means I would like to have I would like to use the biasing current at the source of the transistor. So, this let us say is I0 right.

What about the gate how do how do we plan to bias the gate same old same old gate we are not doing anything because you already have established that the input is going to the source. So, the gate we can simply bias and leave it right. So, let us say this is Vgq ok. So, what do how do I now what how do you propose I connect the input how do I propose I connect the input to the source and I can I connect like can I simply connect the incremental input to the to the source. I cannot because now the incremental input has a resistance Rs and that will load the DC picture and all those same story will happen.

So, what is the best way to go about doing it? The best way is basically put a coupling capacitor Let us call this C2 ok. What about now the drain terminal. So, clearly the drain terminal impedance incrementally is infinite Y22 is equal to 0 or gds is equal to 0 which means I can take the output from the drain terminal. In other words the load has to be connected to the drain terminal and how do I connect the load I mean I can directly connect the load to VDD or if you are not satisfied by now we already know what to do we can connect this to Rd and then AC couple let us call this C3. So, that is what we were calling it earlier connect the load at the AC couple the load like this and we can take the output across R ok.

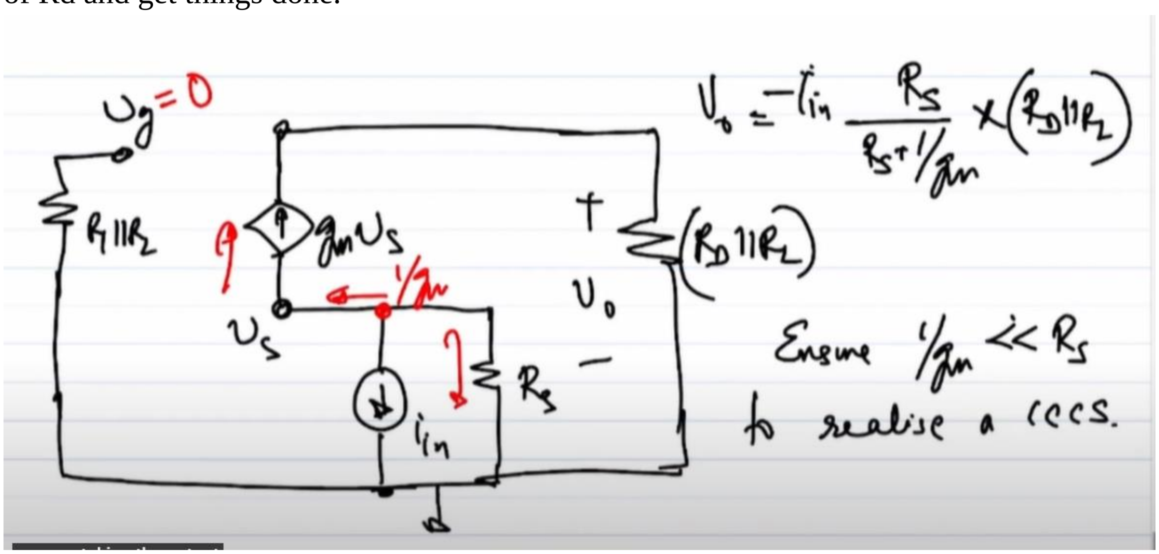


So, now what do you think will be what do you think is the input resistance? What will be the input resistance in the incremental model? What do you think will be the input resistance? What is the input terminal? So, this clearly the input terminal. So, this is the input terminal. What is the output terminal? So, clearly this is the output terminal right. So, what is the input impedance? What is meant by input impedance? Input impedance is meant by the impedance looking into the input terminal incremental impedance looking into the input terminal is what? Again we have done this multiple times this is 1 over gm correct. So, how much current will flow into the source? Note that in the incremental model.

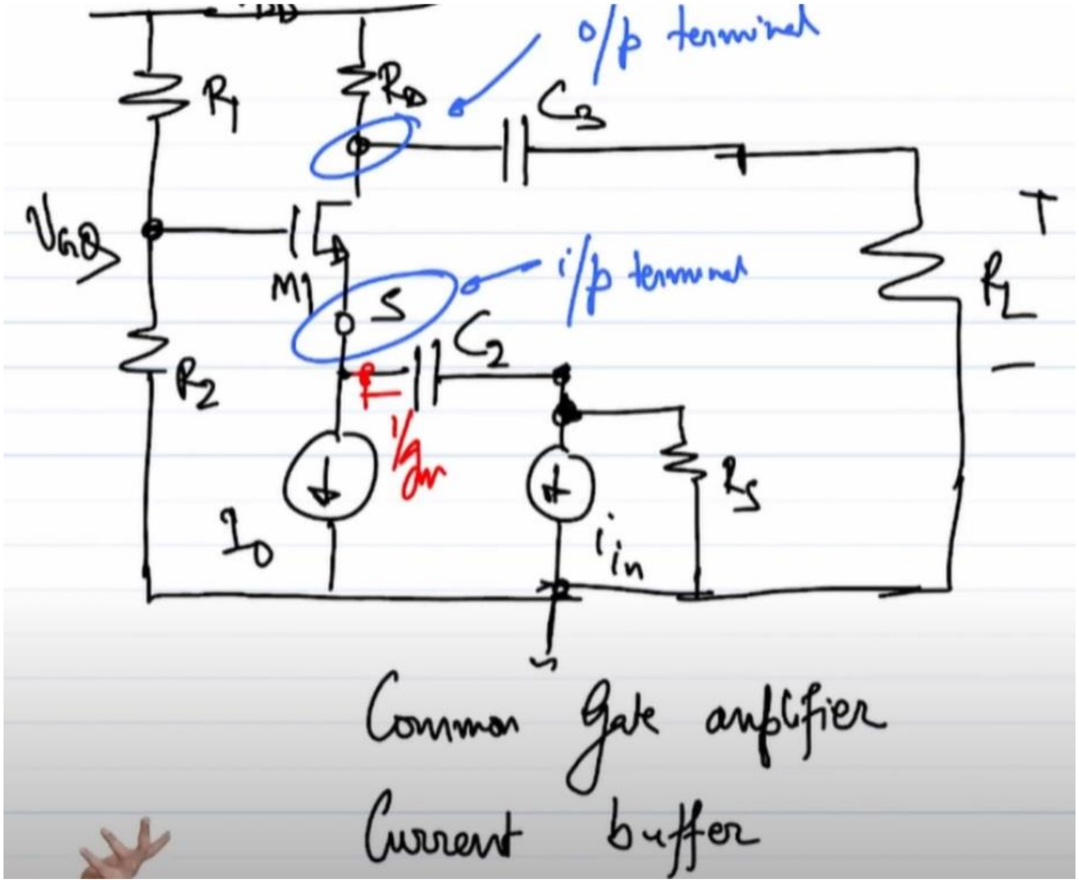
So, if you are not if we have to go if you have to sketch out the incremental model this is what we will see. So, in the incremental model the gate is connected via R1 parallel R2 to ground this is Vg. I have an input which is In connected to the source of the transistor Vs, the In has the internal resistance Rs and the output is essentially Rd parallel Rl and we are taking the output across this terminals right. And this current is gm times Vgs correct. What is Vg? Vg is 0 because it is the floating node one side is connected to R1 parallel R2.

So, Vg is 0. So, this becomes gm minus Vs pointing downwards. So, this essentially becomes gm Vs pointing upwards right. So, what is the impedance looking up looking into the source impedance looking in is 1 over gm. So, how much current is flowing into the source? In is appearing at this junction and it has to decide how much should it go this way and how much should it go how much portion of it will go into this internally impedance. So, how much will go upstairs? So, clearly the voltage division of it.

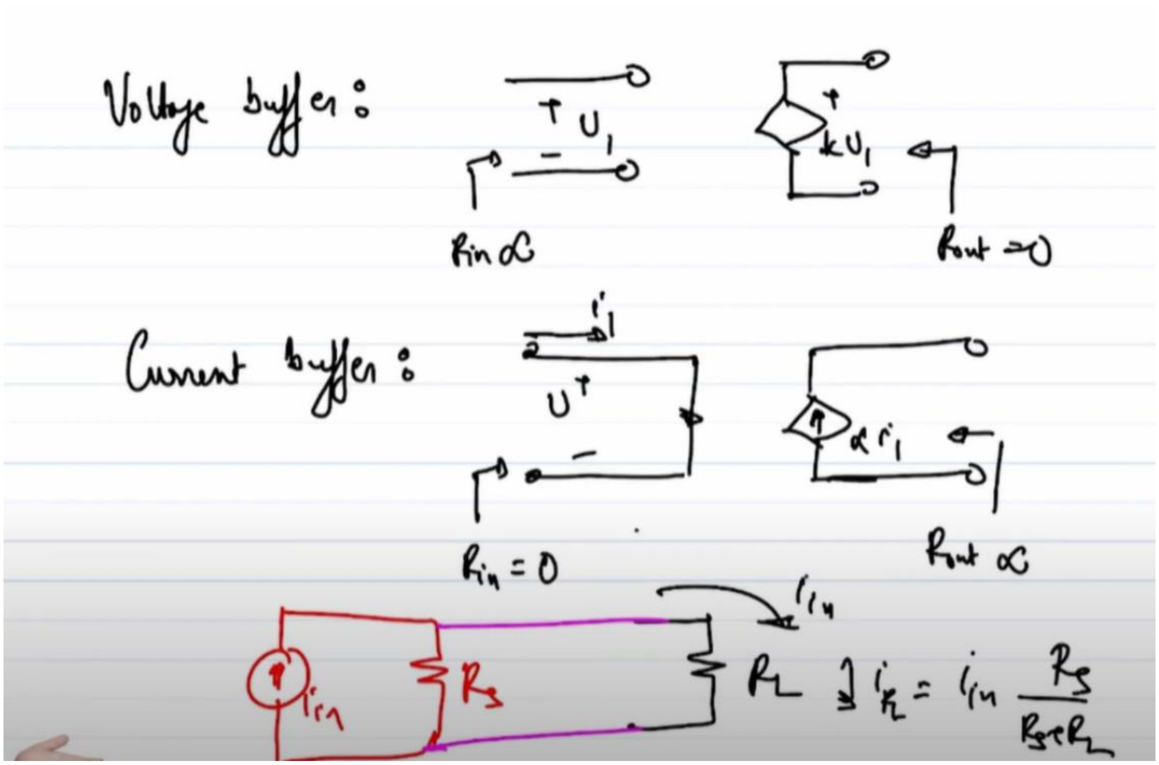
So, how much? So, this will be Rs by Rs plus 1 over gm will be the current that is flowing through the gm Vgs current source and this current will flow into the parallel combination of Rd parallel Rl and it will create a voltage of. So, I have to the current division so this is minus Iin times current that is flowing in and this current is creating a voltage of RT parallel Rl and this will be the V0. So, in order to ensure that this behaves like a voltage the current control source current control input source what we need to ensure? We need to ensure that ensure 1 over gm is much much less than Rs to realize a CCCs. Why are we not bothered about the output side? We are not bothered at the output side because we know the output impedance is anyways infinite looking into the drain. I mean one might argue that the presence of RT has reduced the output impedance sure, but I can always increase the value of Rd and get things done.



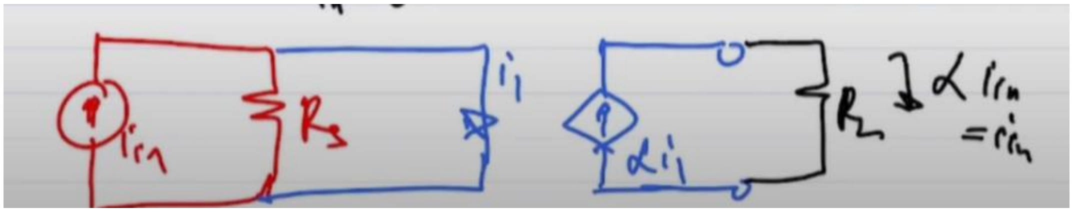
So, now here comes a set of terminology again. So, incrementally what do you think is happening to the gate? Incrementally the gate is rounded right input is applied to the source you are taking the output from the output side right. So, this often is called a common gate amplifier right. So, again please recall when I say common gate what I essentially mean is grounded gate right. So, in this case the gate is grounded it is called a common gate amplifier this is also called a current buffer.



Why is this called a current buffer? So, in order to appreciate the terminology so what is a current buffer? So, before going into current buffer what is a voltage buffer? What is a voltage buffer? A voltage buffer is a contraption that takes in a voltage V1 and produces an output which is proportional to the voltage V1 and is able to drive any load right which means its output impedance is Rout is 0 right and Rin is infinite. So, what should be a current buffer? What should be a current buffer? A current buffeRin plain English should be a contraption that takes in a current at its input side right it takes in current at its input side. So, let us say this is the port V1 this is the current I1 it takes in a current at the input side and produces a current at the output side which is proportional to the current that it is that it is taking in right. So, let us call this alpha times I1 and is able to drive any load which means what? Its output impedance has to be infinity and its input impedance has to be 0. This is an ideal current buffer and why do we call it a buffer? We call it a buffer because so let us say I have an ideal non-ideal current source let us say I have a non-ideal current source Iin it has some resistance Rs and I would like to pass I would like to pass it pass this entire Rin to another resistance Rn.



What is the problem statement? The problem statement is I have this non-ideal current source Iin which has internal resistance Rs and I would like to build I have to build something here so that the current Iin flows into RL the entirety of Iin or maybe a significant fraction of Iin flows into RL. So, if I simply connect these two if I simply connect these two what happens there is a current division that happens and the current that will flow that is IRL will be Iin times Rs by Rs plus RL. So, now if RL is comparable to Rs then clearly you see a significant portion of the Iin will be lost and if RL is less than Rs I am sorry if RL is more than Rs then almost nothing of Iin will go into RL. So, then we have to put some buffer so what buffer do we put? We put a current buffer. What is the current buffer again? A current buffer is a contraption that is a short circuit at the input port and creates a current which is some alpha times I1 at the output port and if the RL is connected here if alpha is equal to 1 for example clearly the amount of current that will flow here is alpha times Iin which is equal to Iin if alpha equal to 1.



So, the current that flows into RL is independent it is not dependent on the effect of loading of the RL on the non-ideal current source Iin. So, hence this is a this is the job of a current buffer to translate the current at one port into the other port without causing any loading.

So, looks like the buffer that we have I mean the common gate amplifier that we have is doing just that because the amount of current that is flowing in so what is the current that is flowing in? The amount of current that is flowing in is almost equal to Iin if gm times Rs is much greater than 1. Now Rs might not be in your control but gm is in your control you can design your circuit in such a way that gm times Rs is much greater than 1. If that is true then almost entire Iin flows in regardless of whatever is connected at the output port.

Since the entire Iin flows in regardless of whatever is connected to the output port this essentially becomes a current buffer because it is conveying the input current information from a non-ideal source efficiently to the output and isolating the loading effect of the output RL on the non-ideal input source. So, this essentially becomes a current buffer as well. So, what I would next request you to do is to find out what is the swing limits of Iin. So, what I would request you to do is find assume Iin is equal to some Ip sin omega 0 t find the swing limits of Ip right or Let me say find Ip max for which M1 is in saturation and away from cut off right. So, I hope you will be you will do it before the next lecture and we will discuss this in the we discuss the answer in the in the next lecture. Thank you. .