Course name- Analog VLSI Design (108104193)
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Week- 7
Lecture- 20, Module-1

Welcome back, this is lecture 20. So, in the previous lecture we saw that when we bias our transistor with a constant current source when the source when the current source was connected to the source of the transistor, we could use this configuration to our advantage in order to realize multiple topologies. One topology was obviously the common source amplifier and the other topology was to design a common drain amplifier where the resistance with the load resistance R L is connected to the source and the drain is incrementally grounded, right. Okay, so this is R S, this is V i, C 1, this is C 2. Then we also saw what are the constraint on C 2, we also saw what are the constraint on C 2 in order to ensure that this behaves like a common drain amplifier. We also discovered one interesting property of the MOSFET and the interesting property that we discovered was the fact that the resistance looking into the source of the MOSFET is equal to 1 over g m, right.

So, in case of an ideal MOSFET biased in saturation, right, so biased in saturation, right. So, it means gate is with some voltage, drain is with some voltage, source is with some voltage, the incremental resistance looking in, right, the R T H looking in is equal to 1 over g m of the transistor and we also knew that the R T H looking into the drain of the transistor, right, when the transistor is biased in saturation R T H is equal to infinity because its Y 2 2 was 0 or its g d s was 0. So, hence we were able to use common source amplifier to get our, to drive all the current that was coming from the MOSFET into the load resistance and we got some voltage gain, in the process we also got some power gain. However, in this architecture we saw that since the resistance looking in into the source of a transistor, the incremental resistance looking into the source of the transistor is not infinity, in fact it is 1 over g m which can be small with respect to the resistance R L, right.

So, in that case it seems like we have a contraption whose output resistance is lower than the load that it is driving. If the output resistance is lower, so if R T H or R out is much much smaller than R L, then we could, we can use the block as a voltage source, right, as a voltage source. And using this property we try to see if we connect R L to the source of M 1, obviously through AC coupling capacitor C 2, then whether this can behave like a voltage source and we saw that, right. We saw that as long as g m of M 1 times R L is much much greater than unity, which is another way of saying 1 over g m is much much smaller than R L, then we saw that R L was not loading, R L was not loading the transistor, which essentially means that the transistor is now acting as a voltage source while driving R L, right. So, this is where we stopped.

So, we would like to explore this architecture a bit more and we would also like to see what are the swing limits of this architecture. If you recall we saw the swing limits of a common source amplifier, few lectures back. We would like, we would also like to see what is the maximum swing that you can apply, maximum input voltage that you can apply to this transistor in order to establish its limits, right. So, if we, obviously I cannot apply infinite amplitude sine wave at the input. So, what we would like to see what are the, what are the swing limits for this architecture, right.

So, let us go about analyzing the same. Ok, so what should we do to establish swing limits? What is the first thing that we need to do? We need to first find out the quiescent drain and quiescent voltages and currents. So, what is the quiescent voltage? So, we establish that I have some current I naught and we have some voltage VgQ, right. So, let me use a different color. So, we have a voltage VgQ, this current is I naught, ok.

So, what is this voltage at the source? This voltage at the source is VgQ minus Vgs for a current of I naught. So, let me call this V sQ, ok. What is the, what is the current, quiescent current through RL which is clearly 0, right. What is the quiescent current through the source, right, through the input Vi which is also clearly 0. Let us assume Vi is equal to Vp sine omega naught t, ok.

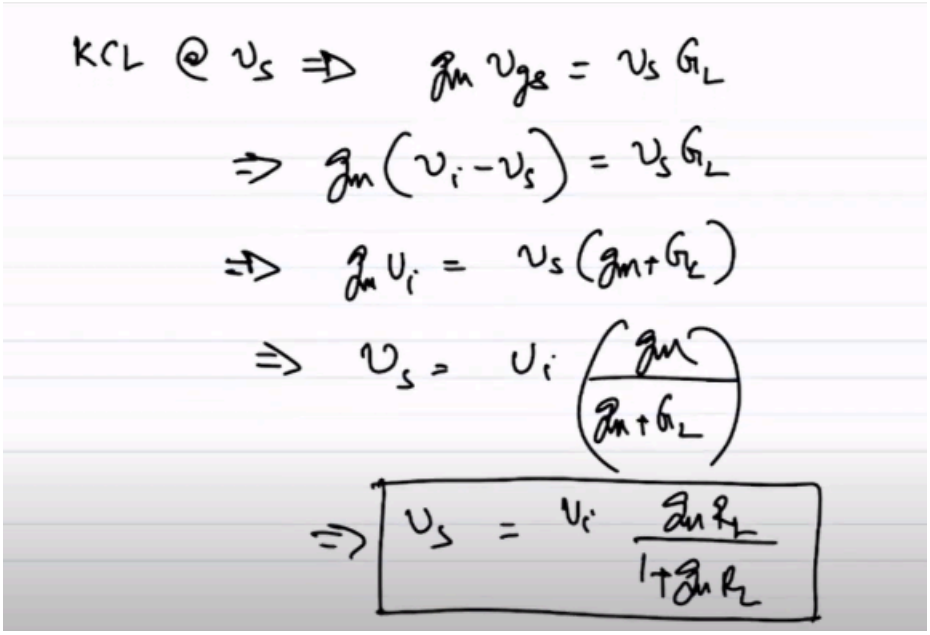
Further we can assume that in this particular instance we can, let us assume that C1 and C2 are large enough to be treated as short circuits, ok, at frequency of omega naught. And now if that is the case, so what is the next step to do? Since the quiescent point is established we would also like to see what is the incremental currents and voltages at the different terminals of the transistor and also through the transistor, the currents through the transistor. So, the next step will be to figure out what will be the incremental equivalent of this. So, let us do that what is the incremental equivalent of this? So, Vi Rs capacitor shorts, right, because we assume they are to be large enough for to be treated as a infinite valued. This is R1 parallel R2, ok.

So, this is the gate voltage Vg, this is our transistor, right. This is the source, this is Vs, ok. What is connected at the source? At the source clearly I have a infinite value capacitance C2 and then a resistance RL to ground and what happens to the current source I naught that opens up, right. So, this I have RL to ground. So, just to ensure that I am drawing symmetrically I will just connect all the grounds together.

That is always a good practice to avoid mistakes, right. Now, this value is gm times Vgs, the drain is clearly a short circuit. This goes here and this is my incremental Vnaught, ok. So, what is Vg? Vg is equal to Vi times R1 parallel R2 by Rs plus R1 parallel R2, right. So, which is approximately equal to Vi if we size R1 parallel R2 to be much much greater than Rs and since R1 parallel R2 is in our control we can decide to do that.

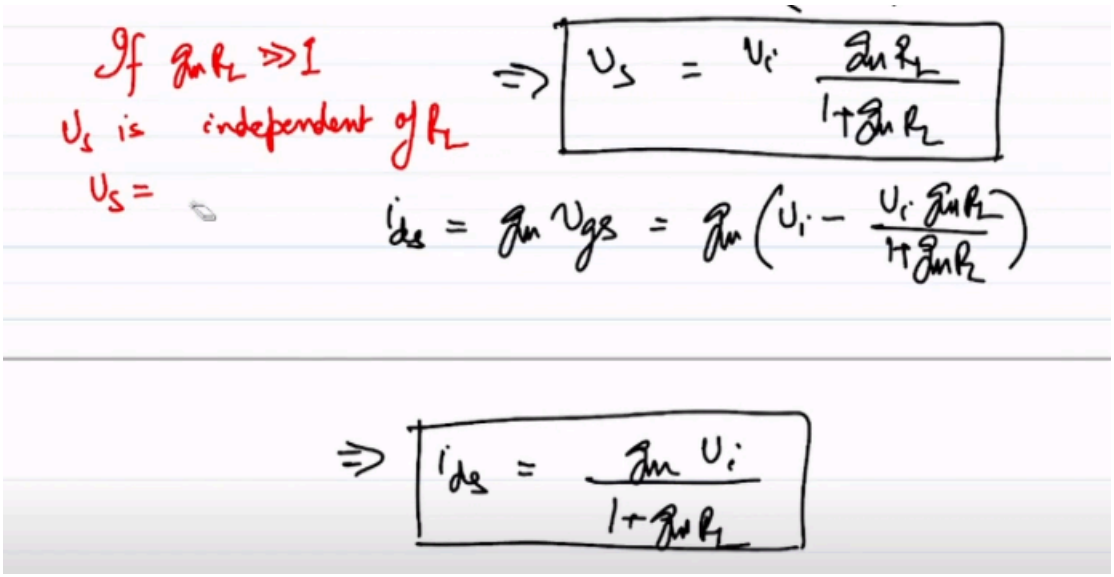
So, let us assume that we have done that, ok. So, Vg is established. What about Vs? What

about Vs? So, in order to figure out Vs what we need to do? We need to solve the KCL at the node Vs, right. KCL at Vs will lead to gm times Vgs will be Vs times gl, but gl is of course 1 over RL, ok, which is gm times Vg minus Vs which is Vi minus Vs which is equal to Vs times gl. Again, even though it is obvious it is instructive to note that this is gm times Vgs, this is not gm times Vg because your source is not grounded, ok.



So, now if I rearrange the terms what do we get? We get gm times Vi is equal to Vs gm plus gl and hence Vi Vs over Vi or simply Vs is equal to Vi gm by gm plus gl and if you are comfortable now writing in terms of RL we can write it as Vi times gm RL by 1 plus gm RL. So, this is Vs and this is exactly what we had got in the previous lecture, ok. So, we got the gate voltage, we got the source voltage, what is the other thing that we need? We need the incremental current, right. So, Ids incremental is gm times Vgs which is gm times Vg minus Vs which is Vi minus Vi times gm RL by 1 plus gm RL which means Ids is equal to gm times Vi by 1 plus gm RL, ok. So, before we proceed let me draw your attention to one more level of detail.

So, in the previous lecture we saw that if gm RL is much much greater than 1, right then Vs is independent of RL and hence this was a voltage source, right or in other words in this case and Vs in this case was is equal to Vi. So, this was acting as a voltage buffer, right. So, if we use the same constraint, if we use the same constraint here what we get? If gm RL is much much greater than 1, what we get Ids becomes gm Vi by gm RL which is Vi over RL, right. So, this seems to be a very simplistic result, right. It seems like I mean after doing all these things and the current the incremental current through the transistor is essentially the input voltage divided by RL, right.



So, is this only mathematics or is there a reason behind it? I would like to draw your attention to the fact that there is in fact a reason behind it and the reason is as follows. So, if we honor the condition of gm RL to be much much greater than 1, what do you think the value of Vs or V0 would have been? Vs or V0 would have been equal to Vi, right. So, V0, this voltage would have been equal to Vi if gm RL was much much greater than 1, right. If this voltage, if the incremental voltage at the output V0 would have been equal to Vi, what do you think the incremental current through RL would have been? So, in this case, I RL would have been Vi over RL and since this would have been Vi over RL that current has nowhere to flow but through the transistor. Hence, the incremental current through the transistor would also have been Vi over RL.

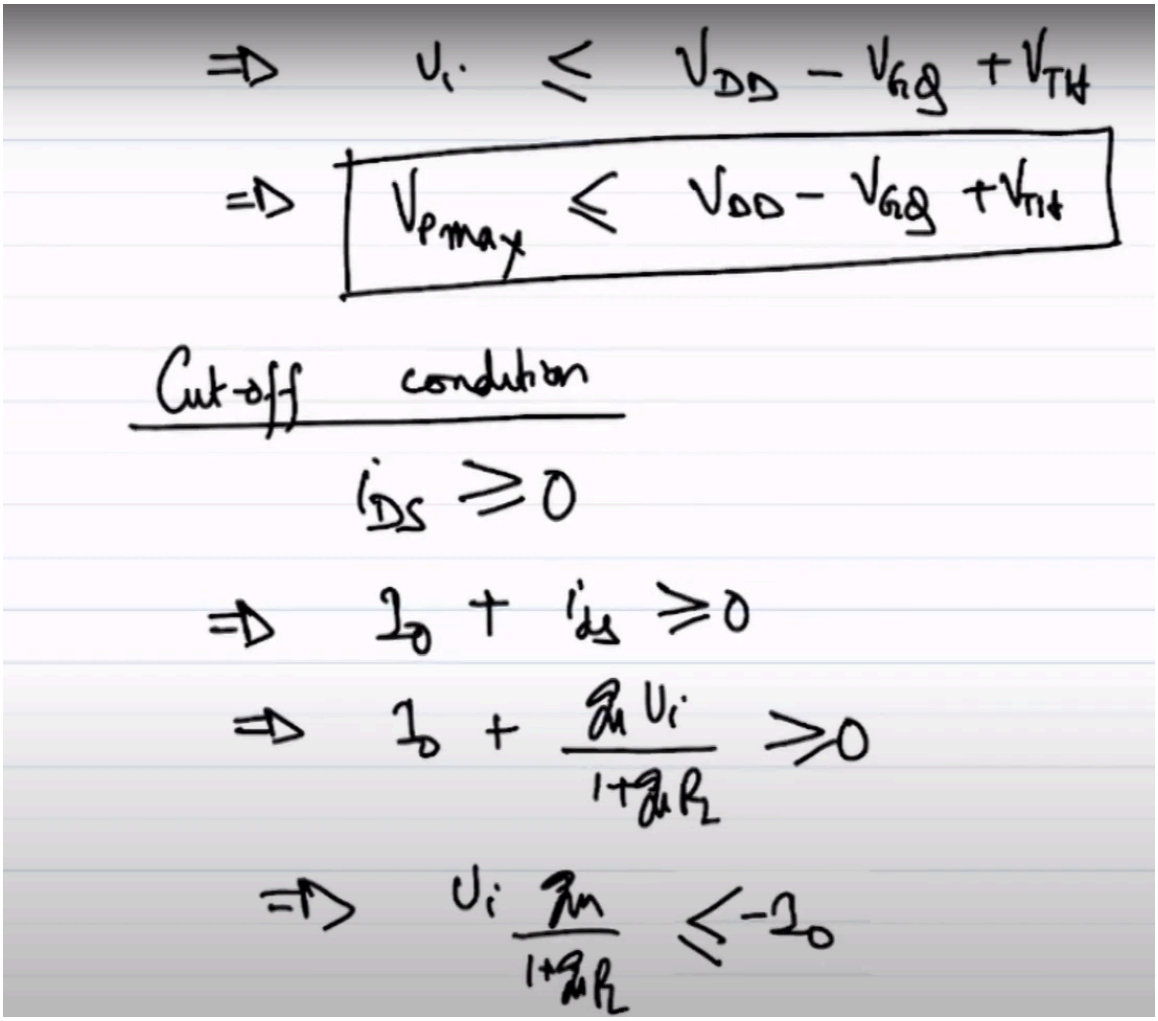
Very often you will see that in case of a voltage buffer we often make the approximation that the incremental current through the transistor is Vi over RL without getting into all the details of whether gm RL, whether the details of output is gm times Vi by 1 plus gm RL, you will get some amount of details through that but very quickly in order to develop intuition you can assume that under the condition that gm RL is much greater than 1, the incremental current through this source follower is Vi over RL and this is the genesis of that argument. Okay, so let us not get sidetracked, let us come back to the requirement of swing limits, right. So, let us sketch the circuit once more. Okay, so what is the total current or rather let us do the easy one first, let us do the voltage, right. Let us do the condition for linearity of M1, right.

So, for M1 to go, M1 to be away from linear region. What is the condition? The condition is that total train voltage has to be greater than equal to total gate voltage minus threshold voltage, correct. What is the total drain voltage? Total drain voltage is VDD because nothing is connected, I mean the drain is already connected to VDD. So, condition is VDD should be greater than equal to, what is the total gate voltage? Total gate voltage is a quiescent voltage,

right, quiescent voltage VgQ plus the incremental voltage at Vg, correct, minus the threshold voltage. So, in other words, VDD should be greater than VgQ.

What is the incremental voltage at Vg? We saw that the incremental voltage at Vg under the condition that R1 parallel R2 is much greater than Rs is equal to Vi minus threshold voltage which essentially means that the condition that we end up with is Vi should be less than equal to VDD minus Vgq plus threshold voltage or since Vi is a sinusoid, we end up with Vp max should be less than VDD minus VgQ plus threshold voltage, ok. So, this is as far as the linearity condition, this is as far as keeping the transistor in saturation condition is concerned. What about the cut-off condition? Again, I would like to remind you the fact that we are not talking about absolute cut-off here, we are talking about the case in which the quiescent current plus the small signal incremental current goes to 0 and we saw that that is a far more prudent condition to use. You would anyway not want to drive your transistor to 0 current because your signals will be far more distorted and also we saw that the condition for small signal approximations to hold is that your the incremental Vgs has to be much lesser than the overdrive of the transistor, right. So, since that has to hold we cannot anyway shut the overdrive to 0, right.

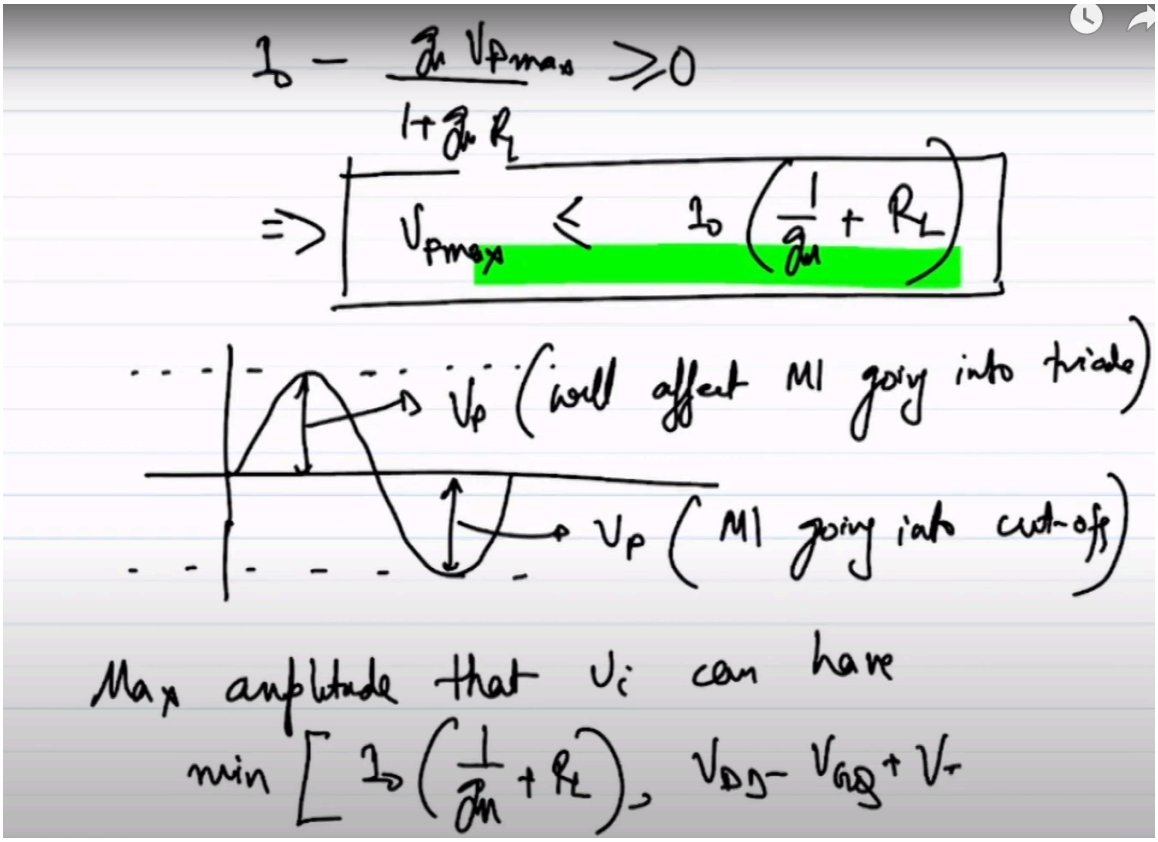
So, we will use the, throughout the course we will use the condition of quiescent plus incremental, right. So, what is what was the quiescent current? So, what is the condition? The condition is id, as it has to remain greater than 0. So, what is the quiescent current? Quiescent current through the transistor in this case ids, right. Quiescent current through the transistor was I0. What was the incremental current? Incremental current is ids, right.



ids has to be greater than equal to 0. What was ids? ids was gm Vi by 1 plus gm RL this has to be greater than 0. In other words, in this case Vi gm by 1 plus gm RL has to be less than equal to minus I0. If we directly replace Vi is equal to minus Vp. So, this condition is likely to occur when Vi is equal to minus Vp, right.

Goes at the lower end of the cycle. So, this becomes I0 minus gm times Vp by 1 plus gm RL or Vp max in this case, right. gm RL should be less than equal to 0, sorry, greater than equal to 0. In other words, Vp max has to be less than equal to I0 1 by gm plus RL, ok.

Ok. So, this is essentially the constraint that you will have to honor while trying to figure out what is the max, what is the Vp max when the sinusoid goes in the negative direction, right. So, essentially what we are saying is if I have, if this is, if this is my sinusoid, right. This is Vp, this will be Vp, this will also be Vp, but this Vp will affect M1 going into triode. The lower Vp will affect M1 going into cut-off. Now, if you want to ensure that it neither goes into triode nor into cut-off, then you will have to choose your Vp in such a way that it honors both the condition of this and this.



So, whichever is the smaller value, right, whichever is the smaller value will ultimately end up being the, will end up being the maximum amplitude of the sinusoid that you can apply. So, in other words, so Vp max amplitude that Vi can have will be minimum of this condition that is I0 1 over gm plus RL and this condition, right, Vdd minus VgQ plus threshold voltage, Vdd minus VgQ plus the threshold voltage, ok. Thank you.