Course name- Analog VLSI Design (108104193)
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Week- 7
Lecture- 19, Module-1

Now, we will come back, this is lecture 19. So in the previous lecture, we saw another way of designing a common source amplifier where the MOSFET was biased using a constant current source. However, the current source was attached to the source right instead of the train right. So if I have to sketch the same circuit again, this is what we saw. We saw couple of things, number 1, this way of biasing does not need anything in the sense that you stick in the current source at the source and given that you have some appropriate bias voltage at the gate, the transistor biases itself right. And then we had to apply an input, we had to AC couple the input, that is what we did.

And however, we saw that in this case, we had to ensure that in a common source amplifier the source has to be incrementally grounded. The way we could do that was by connecting the capacitor right, connecting a capacitor C2 and we assume that C2 is the infinite value. And how was the load connected? The load was again connected through another capacitor C3 and this is what our network was okay. So this is where we stopped, we did the analysis of the small signal model and we stopped here.

But like before we like to know what is this infinite capacitor right, what is the value of this infinite capacitor because ultimately at the end of the day nothing is infinity. We need to understand what is the minimum value of capacitance that we can get away with okay. So what is the principle of finding out the minimum value of the capacitance? So principle is for a first order circuit, for finding mean C so that it acts as a short circuit at a frequency omega naught radian per second and we need to find the time constant right if the network is first order. So this is important. So the network has to be first order.

If the network is not of first order, the time constant is of no use because you cannot define a time constant if the circuit is, if the network is not of first order right okay. So which means that I need to figure out what the time constant associated with C2 is right. So in order to figure out the

KCL @ v_s

$$-g_m v_s = j\omega_0 C_2 v_s$$

$$\Rightarrow v_s (g_m + j\omega_0 C_2) = 0$$

$$\Rightarrow v_s = 0$$

$$R_{Th} = R_S + R_L$$

$$\tau_2 = C_2 (R_S + R_L) \gg \frac{1}{\omega}$$

time constant, what is the time constant that is associated with C2, what should we do? Let me mark the transistor M1. So obviously we have to first linearize the circuit right, replace the MOSFET with this small signal equivalent and then do the analysis right. So let us do that.

So what should we do? So we notice what should I replace the MOSFET with? The MOSFET goes, MOSFET is replaced with a small signal equivalent right. So this is gm Vgs okay. What is source? What is the source of the MOSFET? Note that the current source I0 goes to infinity in the incremental model. So I am left with only C2 right. So I am not replacing C2 with a short circuit because we are trying to figure out the time constant associated with C2.

So I am keeping the C2 as is right. So I am keeping C2 okay. So this is Vs, this is Vg. What is associated with Vg? With Vg I have a parallel combination of R1, R2 to ground right. So parallel combination of R1, R2 to ground.

What else do we have? We have C1 right. We have C1. What else we have? We have Rs and then we have Vi right. We have Rs and we have Vi but in order to figure out time constant we do not need the input. We can de-energize the input.

Setting Vi to 0 is equivalent to shorting this terminal okay. So far so good. What is happening at the drain side? At the drain side I have a resistance to Vdd which means incrementally resistance to ground and I have a C3 and RL also connected right in parallel to it. So what do we have here? We have R3. This is also to ground.

So I have C3 and RL which is also to ground. So what I will do? I will just make all the grounds same so that there is no confusion. So these are all the grounds are tied together right. So all the grounds are tied together. So that there is no confusion and what we need? We are trying to figure out what is the time constant associated with C2 okay.

So you might say that this is not a first order circuit. You would be right. This is not a first order circuit because you have three capacitors C1, C2, C3 but let us see whether this is something can be and we get more intuition because of the circuit is of a certain type right. So what do you think will be this voltage Vg? So note that this loop is a self-contained loop and it does not have any source associated with it right. So no current will flow into the loop right.

Since no current will flow into the loop what do you think will be and this given that this is 0 volt what do you think the voltage at Vg will be incremental voltage.

Incremental voltage at Vg is 0 right. So Vg goes to 0 okay. So what is now if Vg grows to 0 what is gm times Vgs? gm times Vgs becomes gm times Vg minus Vs which is gm times minus Vs right. So I can replace this with gm times minus Vs okay great.

So if we have to figure out the time constant associated with the capacitor C2 right then what should we do? We should we need to find out the Thevenin equivalent resistance looking from the two terminals of the capacitor right. Basically we need to find out the Thevenin equivalent resistance looking into this right. We can remove C2 and find out the Thevenin equivalent right. So let us do that. So in this case now I can basically remove the loop at the input end because that is 0 that is of no use.

So let us remove that. So what am I left with the circuit becomes significantly simpler. So the input side Vg becomes grounded okay. So this becomes Vs. Let me draw it in a different page so that would be clearer.

So Vg is grounded. This is gm times minus Vs and I have the capacitor here. So I am trying to find out the impedance looking into the network from the two ends of the capacitor. So I do not need the capacitor I can put a test voltage right. So I can put a test voltage Vtest and I want to figure out what the Itest is right okay. What is connected at the other end of the drain? At the other end of the drain I have a resistance connected to ground and I have a combination of capacitance and resistance connected to ground okay fine okay.

So far so good. So now you notice that here we have a current source gm times minus Vs pointing downwards. Negative is something that is we are not particularly good at handling at least for the intuition purposes what I will do is I will make it gm times Vs and I will flip the direction of the current okay. So let us do that. So I will flip the direction of the current and I will make this. So if we flip the direction of the current source I make this gm times Vs okay.

This is Vs okay. So what is Vs in this? Vs is equal to Vtest right because simply because I have connected Vtest between Vs and ground right. So what is gm times Vs? So gm times Vs becomes gm times Vtest okay and this happens to be the current Itest right. So what is Vtest over Itest then? Let me write it here. So then Vtest over Itest times 1 over gm that I am just writing 1 right and this becomes equal to the Thevenin resistance associated with the capacitor. Note that 1 over gm is purely resistive right.

It does not have any imaginary term, any S term which means which essentially means that now if I have to draw the equivalent circuit from the capacitor C2 from the perspective of the capacitor C2 what do I see? I see capacitor C2 and what do I see on this side? What I am essentially asking is what am I seeing this side? I am seeing Rth. What is Rth? Rth is 1 over gm. So what do I see here? I see 1 over right. So now if this is what type of circuit, what is the order of this circuit? Obviously this order of the circuit is a first order so we can associate a time constant. What is the time constant associated with the capacitor C2? Let us call it tau 2 that is 1 over gm times C2 and in order for the capacitor to behave in like a short circuit what needs to happen? This has to be much much greater than 1 over the frequency of interest at radian per second, right.

So, radian per second which means that C2 has to be much much greater than gm over m over omega right. So, if you can ensure this, if you can ensure this right then C2 will behave like a short circuit at right. What about then let us turn our focus to the capacitor C3 right. So, again for C3 the input side of the network the input loop does not matter because while we are calculating time constant the input side is essentially not there right because I do not have any input and there is also no connection between the input and the output right I mean directly. So, I can essentially remove this ok.

What about what should I do now? So, like before I have to find out the time constant associated with C3 which effectively means that I have to find out the Thevenin equivalent impedance looking from these terminals right. What should I do? I will, I should put again a test voltage source Vtest I need to find out what it is right ok. So, what do you think in this case what will be the effect of this gm times vs right. So, essentially what I am asking is how much of the it is do you think will flow into R3 and how much of it will flow into the network in the bottom right. So, what do you think will happen? So, let us assume let us assume that some part flows and it generates a voltage vs right ok.

So, what happens then? So, if some part flows down right if some part flows down and it generates a voltage vs. So, if I find out the KCL at that node vs what do I get? I get the amount of current flowing down. So, KCL at vs leads to minus gm times vs which is the current flowing down it should be equal to it should be equal to the current flowing down from the capacitor through the capacitor. And what is the current flowing down through the capacitor? SC2 times vs right this should be SC2 times vs right. If you are not comfortable with SC2 let us call it j omega naught C2 times vs because we are talking about some frequency omega naught right we are trying to figure out.

So, which means it becomes vs gm plus j omega naught C2 is equal to 0 right which means what the only possible solution which is which is general which can be generalized is vs has to be equal to 0 vs is equal to 0 what does it imply? It implies that there is no current flowing downwards right. So, there is no current flowing downwards then what does it imply? It implies that the loop the only loop that is in existence is the loop on top and what is the equivalent resistance? What is the equivalent hevelin resistance look when the loop on the top? It is R3 plus RL. So, that is right so Rth in this case is R3 plus RL which essentially means that the tau associated the time constant associated with the capacitor at C3 or the capacitor C3 is C3 times R3 plus RL and this has to be much much greater than 1 over omega naught which means C3 has to be much much greater than R3 plus RL times omega naught right. Note that this has not changed and this constraint has not changed from the original common source amplifier that we initially researched. However, the important addition here is that we have a additional constraint because we have an additional capacitor C2 ok. Thank you. .