Course name- Analog VLSI Design (108104193)
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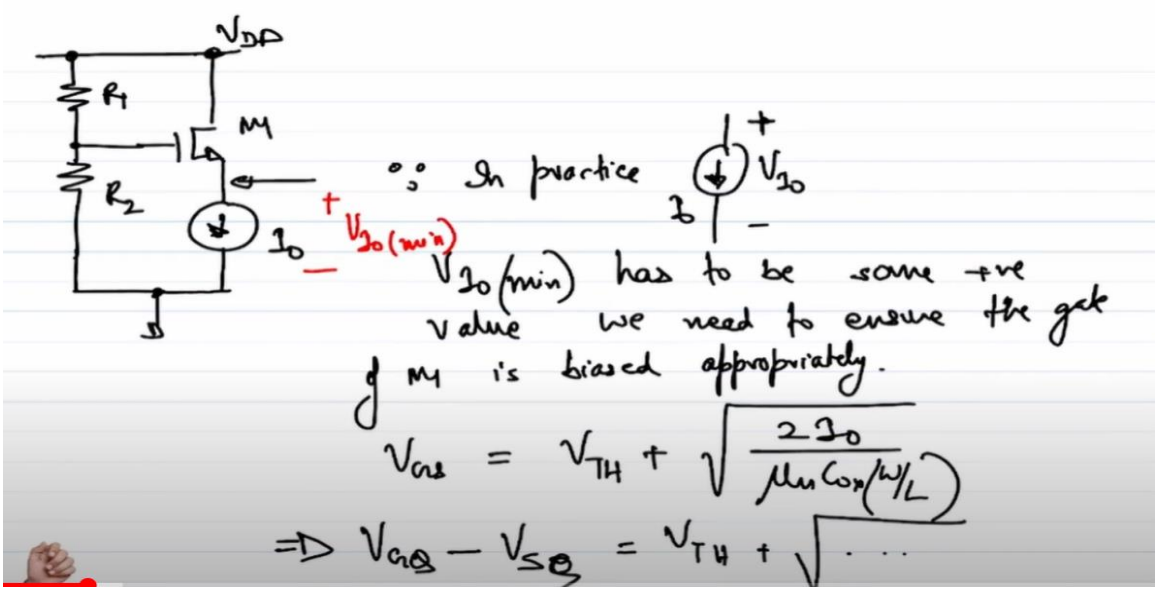
Lecture- 18, module-02

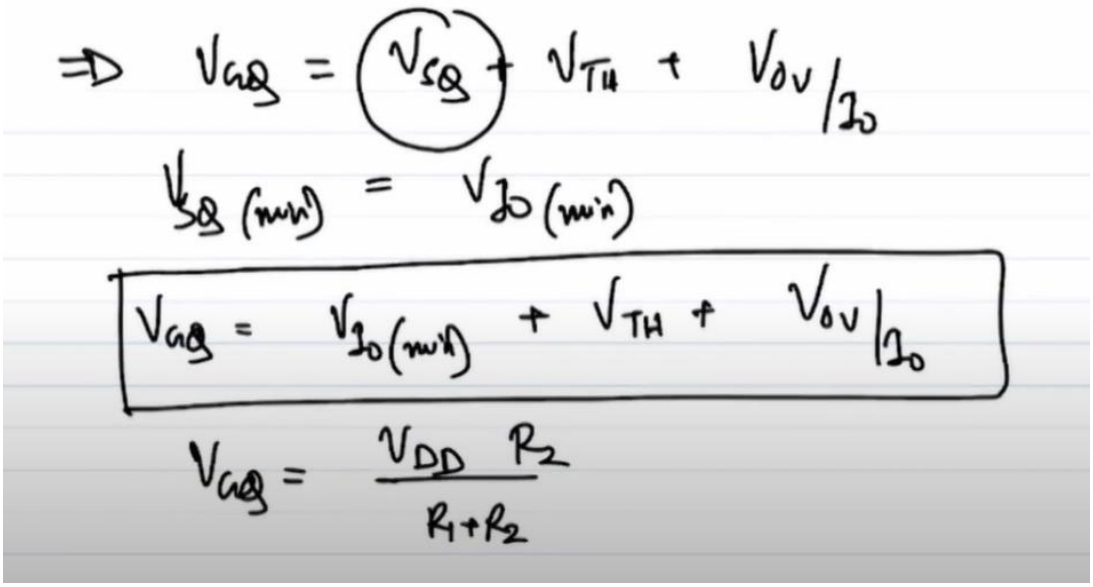
Welcome back. So, we are now at this stage where our biasing of the transistor using a constant current source where the constant current source has been connected at the source of the transistor, it seems like we do not have to do anything and the transistor is getting biased automatically, right ok. So far so good, I mean looks like best of all worlds, but yet we have not yet figured out, we have not yet figured out what the gate voltage Vgq needs to be because ultimately it is when you have an ideal current source one might say that ok I mean the voltage at the source voltage at this node can be anything and the current source will not get affected, but ultimately everything is a real element the current source is also a real element which essentially means that this voltage, voltage at the source cannot go below ground right. So, since in practice this I0, if this is I0 and this is the voltage across I0, let us just say that Vi0, since in practice Vi0 minimum has to be positive some positive value, we need to ensure the gate of M1 is biased appropriately. Why did I make that statement? I made this statement because if let us say Vgq for some reason is if let us say R2 is much much less than R1 right, if R2 is much much less than R1 Vgq will be very close to ground right. If Vgq let us say is almost close to ground right and you want I0 to flow through M1 what do you expect this voltage to be? You would expect some finite overdrive voltage and you would expect that overdrive voltage to be on top of special voltage you expect a positive Vgs right.



If we expect a positive Vgs and the gate is grounded what will be the source voltage? The source voltage will be negative. If the source voltage is negative do you think a real current source a practical current source will work? It will not work because for a practical current source to work you need to have a positive voltage in the direction shown right. This I mean in an ideal world where the current source can have any voltage across it while still operating like a current source then it is not a problem, but we do not live in an ideal world and as it turns out current sources are also made out of transistors right. So, which essence means that we need to put a minimum voltage Vi0 across the across the current source right.

So, if that is the case if that is the case we cannot have any arbitrary value of Vgq. So, then the question begs what value of Vgq we need and the answer to that will start from the analysis to that will start from where this analysis to that will start from what is the minimum voltage that the current source needs right. So, essentially I would need to know what is Vi0 min. Let us assume Vi0 min is known right. If Vi0 min is known then Vgq min or rather if Vi0 min is known then I know that the Vgs of the transistor Vgs of M1 is threshold voltage plus under root 2 Io by mu n Cox W by L of the transistor right.

Now what is Vgs? Vgs is Vgq minus the source voltage right Vsq which is equal to threshold voltage plus under root blah blah blah ok which means what? Which means Vgq is the source voltage plus threshold voltage plus this additional stuff whatever this additional stuff this is. What is this? This is essentially the overdrive of the transistor right. So, I will just simply write it as the overdrive of the transistor I am sorry. So, this is the V overdrive of M1 for a current of Io right. Moment you say overdrive overdrive can change with respect to current.



So, we need to also be cautious and ensure that we specify the current right. Now what is

Vsq? What is the minimum Vsq that we need? The minimum Vsq is Di naught min right. So, this is the necessity I mean Di naught min can be 100 millivolt can be 200 millivolt depending upon how the current source has been made. If that is the case what will be Vgq? Vgq will be Pi naught min plus the threshold voltage plus the V overdrive for the transistor right. And we know that Vgq is Vdd times R2 by R1 plus R2 and then you decide the ratio of R1 and R2 based on whatever Vgq ok.

So, that is as far as biasing the transistor is concerned right. So, let us now assume that this transistor has been biased properly. Let us assume the transistor has been biased properly and I want to use this like an amplifier right. Ultimately we want to use this as an amplifier I mean that is what we have been doing all along we want to use this like a common source amplifier because we can get a gain gain of gm times some resistance right. So, if we have to use this as a common source amplifier what do I need to do? So, firstly we have a input and we have a output or rather input source and output load they need to be connected right ok.

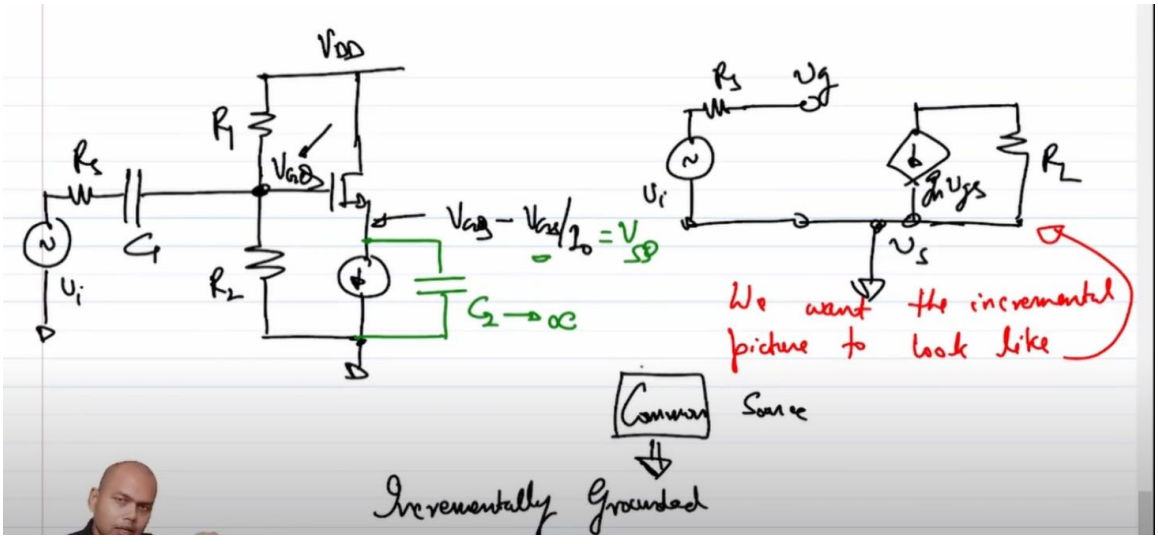
We can take one at a time. However, what is the common source amplifier incremental model of a common source amplifier? The incremental model ideal incremental model for a common source amplifier is this is Vi this is Rs this has to be open circuited this is V1 right or V1 instead of V1 I should say that this is Vg this is Vs, Vs is grounded incrementally grounded and this output goes into RL right. So, this is gm Vgs. This is the incremental model of a common source amplifier right. So, we want the incremental model or incremental picture to look like this to look like this, but the biasing picture should be should be the one in the left right.

So, I hope the problem statement is clear we want we want to modify the biasing picture on the left in such a way that it is the incremental picture looks like the one on the right ok. So, let us do the easy thing first in a common source amplifier where is the input connected input is connected directly to the to the gate right. So, here we also need to connect the input to the gate how can I connect I mean we have done that before in case of a voltage biased common source amplifier we will do the same thing what should we do we will put a we will put a capacitor will AC couple the input right we put C1 and we will assume C1 tends to infinity or C1 is infinitely large. Now, we know that infinitely large means it is infinitely large with respect to I mean we can we can figure out the time constant of the network and then find out the maximum value or the constant on C1 that is necessary for this capacitor C1 to act as a short circuit at the frequency of interest we know that I mean this is this is the done deal we have done that before, but what about the output side? So, in a common source amplifier what does this common source mean we can say that this common source is terminology common essentially means grounded right. So, common means grounded and note that this grounded does not mean absolutely grounded this

grounded means incrementally grounded.

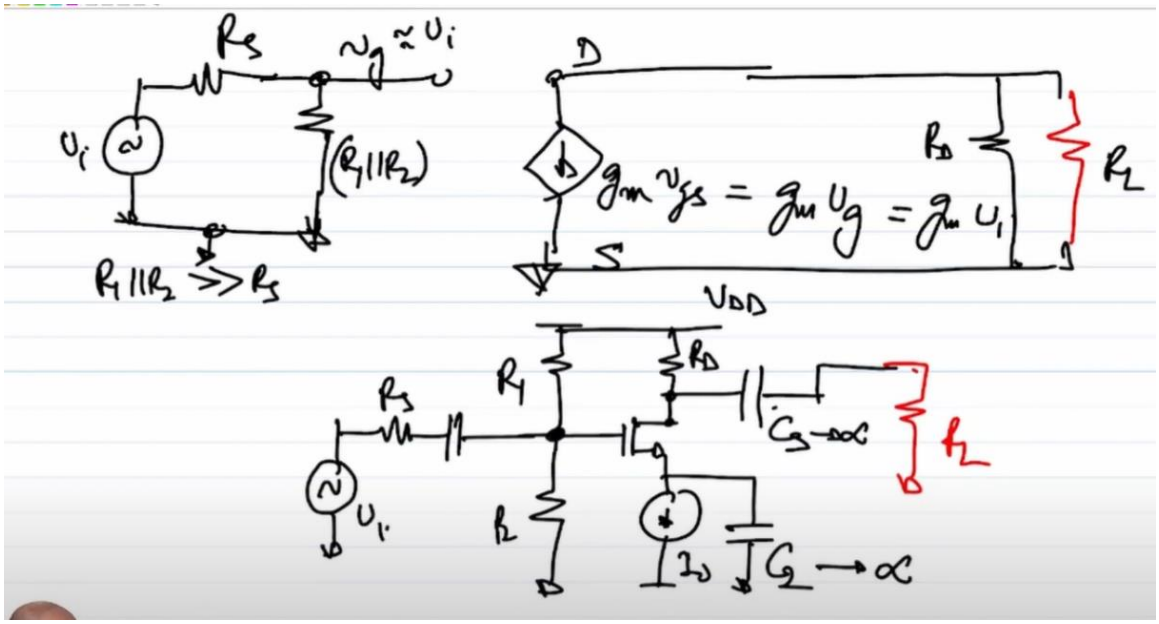
So, this means incrementally grounded. So, in this case as we saw the source is open circuited right in the incremental picture we saw that the source is open circuited because we had a current source connected at the source of the MOSFET and in the incremental picture the current source opens and the source is incrementally open circuited. Then what should we do? What should we do to incrementally round the source? Again what is the if this voltage quiescent wise is Vgq what is this voltage? This voltage will be Vgq minus the Vgs of M1 for a current of I0 and what is incrementally grounded what does incrementally grounded mean? Incrementally grounded mean not increment if some node is incrementally grounded all it means is that it is not changing with time right it is not changing it is a small signal excursions is 0 right. For example, if you have a battery if you have a battery a battery of a certain value is incrementally grounded right the terminals are shorted between the battery because they are not incrementally changing right. So, in this case in order to honor the biasing picture we need to ensure that this voltage is equal to voltage at the source is equal to Vgq minus Vgs times Vgs of I0 right.

So, what can we do we can put a battery of value Vsq which is exactly equal to Vgq minus Vgs of I0. So, nothing changes right what will be the current through the battery in the biasing picture there will be no current through the battery because before I connected the battery the voltage at the source was Vgq minus was Vsq essentially which is V let me call this Vsq the voltage at the source was Vsq after I connected the battery the voltage at the source is still Vsq ok fine. But you might say that again from where can I get a battery because ultimately I have made a point in the previous few lectures that you cannot have indefinite number of batteries you cannot have one you will only have one master battery. So, what was this what was that hack the hack was instead of a battery I can use a infinitely large capacity right. So, which essentially means that I can replace this battery with a very large capacitor.



So, let us do that. So, we can replace this battery with a very large capacitor let me call this C2 and assume C2 tends to infinity ok. So, in the incremental picture how does I mean till now how has the incremental picture gotten affected right how was the incremental picture gotten affected. So, incrementally or the input side what has happened at the input side we have Vi Rs input capacitance is shorted this is R1 parallel R2 again we have to ensure that R1 parallel R2 is much much greater than Rs if this is ensured this voltage will be approximately equal to Vi right ok. So, this is the gate voltage right.

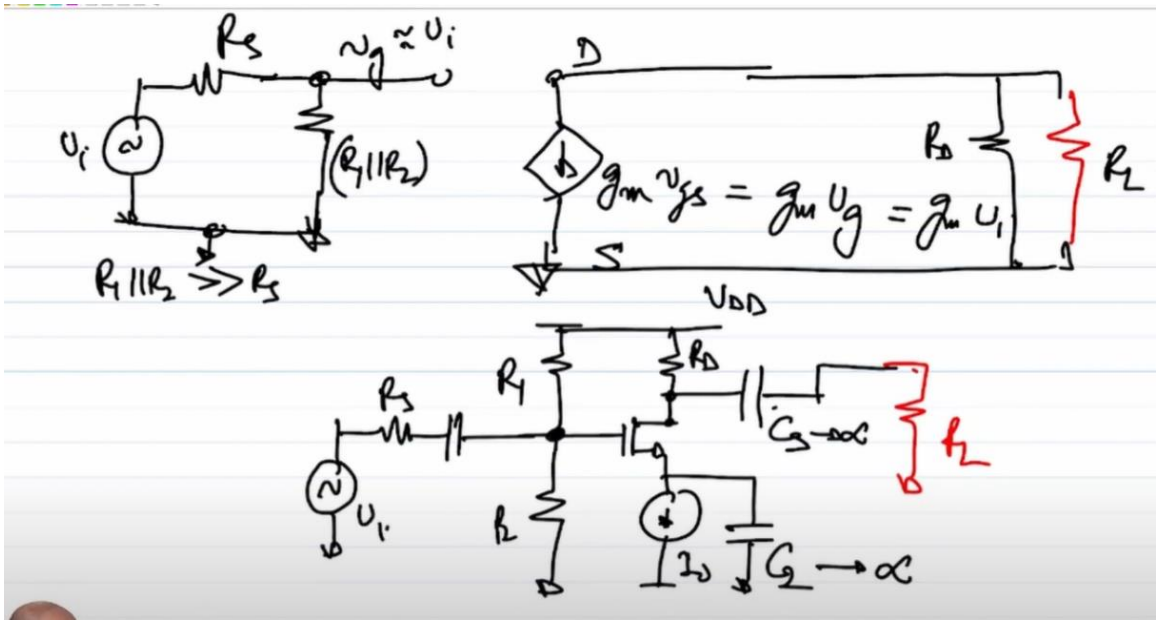
So, this is the Vg which should be approximately equal to Vi what is happening to the other side this is rounded this is the train what is drain connected to drain is connected to a short circuit incrementally because it is connected to a it is connected to a voltage source Vdd. Now what is connected to a source what is connected to a source the source is note that source is now connected to a ideal current source and an infinite capacitor the ideal current source is open and infinite capacitor is a short right in a incremental picture the incrementally this becomes the source becomes a short circuit right. Notice common source amplifier rounded source using that infinite capacitor we are able to sort out the source which means that which means that which means that if there is an increment at the gate voltage this the current here will be Vgm times Vgs, but s is rounded. So, the current is gm times Vg, Vg is almost equal to Vi which means this current becomes gm times Vi right. So, let me write it fully.



So, this is gm times Vgs which is gm times Vg which is gm times Vi ok. Now all the now we are able to generate the incremental current gm times Vi. Now if I ask you what would have happened if I had not put this capacitor C2 infinite capacitor if I had not put that infinite capacitor also let me not connect this if I had not put that infinite capacitor this source terminal would have been open right this source terminal would have been open which means there was no way the gm times Vgs current would have been able to flow

right. So, if gm times Vgs current would not have been able to flow which means this current had to be 0 right if gm times Vgs has to be 0 and we know that gm is not equal to 0 then what is likely to happen which means that Vgs is 0 incremental Vgs is 0 which means that incremental Vg is equal to incremental ds right. So, if this capacitor were not there any change in Vgq right any change in Vgq would have been accompanied with a change in Vsq right.

But in the presence of a capacitor the presence of a infinite capacitor is not allowing the source voltage to move at all since it is not allowing the source voltage to move at all which essentially means that this is incrementally grounded hence we are able to short the incrementally short the source. But note that we have still not arrived at a common source amplifier because what we have not yet looked into the load picture right. What is the load picture? In the load picture of it is you have to ensure that the load is incremental current right. So, now where is this incremental current flowing? This incremental current is now flowing into this short into this into this loop right right. We have to ensure that this incremental current does not flow into the loop we have to ensure that the incremental current flows into the resistance RL our load RL right.



So, we can connect the load RL somewhere here. So, let us say we connect the load RL somewhere in the loop and then we should be we should be done right. So, if this is load RL. So, this is in the incremental picture, but what happens in the total picture because ultimately incremental picture is a model that is not you cannot give your customer an incremental picture in incremental design you have to give the customer a total design right. So, what will be the total design that that will end up with? So, again your Vi, Rs, capacitor C1, R1, R2, MOSFET, constant current source, very large capacitor.

Now we have an RL. Where should RL be connected? RL obviously has to be connected

at the at the drain correct, but what was the issue? The issue is and they needed to be biased at VDD. Now if drain needs to be biased at VDD to maintain to maintain saturation condition of the MOSFET then we land into trouble, but we have solved this issue in case of the common source amplifier right. What was the solution? The solution was do not connect it directly connected through a resistance Rd and then use another capacitor, let me call this C3 and let us say this C3 is infinitely large also at C2 is also infinitely large. So, if that is the case it seems like the incremental current will now flow into the incremental current will now flow into a parallel combination of Rd and RL right. So, this will get modified as parallel combination of Rd and RL and this incrementally is the is the common source amplifier.

Incrementally this picture is exactly equal to the common source amplifier that we initially had, but what is the difference? Why would you want to go through all this trouble? If the original common source amplifier was serving the purpose you would want to go through this trouble because it gives you it gives you a configuration where the gm is invariant of any threshold voltage variation and less variant with respect to mobility variation. In other words this configuration has is robust much more robust towards change in ambient conditions rather than the original common source amplifier topology that we had studied right with respect to with respect to change in change in ambient conditions ok. So, let us stop here. Thank you.