Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 1
Lecture- 2, module-01

So, welcome to Analog VLSI Design, this is lecture 2. So, in the previous lecture, we tried to see what exactly we wanted out of this course in the context of an amplifier design. Then we saw that we wanted, we wanted to design an amplifier that amplifies power. And then we also saw that this is different from, this is different from a voltage right. And we saw it with an example of a transformer, a transformer can act as a voltage amplifier, but it is not a power amplifier because a transformer is a passive device and obviously, a network can a passive network can only pass on the power that it receives in the if the passive network in question is lossless right. If the passive network in question is lossy, then obviously, it cannot even do that.

So, it will consume some power and the power that will be delivered to the load will be lesser than the power that you are extracting from the source. And that is our good old power consumption or law of conservation of energy right ok. So, this is something that we motivated for half of lecture 1. And while we were closing in at the end of lecture 1, we were also trying to see what aspects a network must have if its output voltage is largely independent of its output voltage of the load resistance that it is driving.

So, this was the question, this was the question that we were delving into when we stopped at the stop at lecture 1 right. And the example that we were concentrating on one was the following. So, let us say I have a supply Vdd and let us assume it is an ideal supply with no internal resistance. If it does not have an internal resistance, it effectively has an infinite driving capacity. Now, we said that we wanted if this is equal to 2 volts, and we wanted an 1 volt output right.

If you wanted an 1 volt output and then we said that this can be easily be achieved by making a voltage width divider using a resistor divider stack. And we will be observing the voltage at the location mark. However, now what happens if I connect a resistance on del because ultimately when you are making some network, you are making the network in order to drive something right. There is no point in making a network which cannot drive a load. So, all networks, all electrical networks that we make is made with the purpose of driving something.

So, in this case we said that whatever is if this network is supposed to drive an RL and

on top of that we would want this voltage Vo to be approximately equal to Vdd by 2 per 1 volt, then what is the constraint on RL and R and so on right. So, we did this from the perspective of output resistance, and I hope you have also done it from the perspective of figuring out the total resistance or the total Vo right and then I am sure we came to the same conclusion. Now the curious among you might also be, might also have gotten a third way of looking at it and let me spend couple of minutes on the third way. The third way is that of if I use Thevenin's theorem or if I rather Thevenize this circuit in the box right, if I Thevenize this circuit in the box right and I try to Thevenize a circuit from looking from this port right. If I try to Thevenize a circuit looking from this port, what should I get? What will be the, what will be the Thevenin equivalent network? The Thevenin equivalent network will be the same network or in other words how do I derive a Thevenin equivalent network in order to derive a Thevenin equivalent voltage, I will have to remove the load that is connected between the ports and I will have to find out the voltage.

So, this voltage will be my Thevenin equivalent voltage and what will be the Thevenin equivalent resistance right. The Thevenin to find out the Thevenin equivalent resistance again we will have to remove RL, we will have to remove R L right. We will remove R L and what we do next? We desensitize or de-energize all the voltage sources, that is we set all the voltage sources to 0, if there were current sources, we had to set the current sources to 0. So, setting a voltage source to 0 is equivalent to short circuiting the voltage source, setting a current source to 0 is equivalent to open circuiting a current source. In this in this network we have a voltage source.

So, we short circuit the voltage source right and if we short circuit the voltage source what do what we what do we end up with? We end up with this network and what is the effective impedance looking in? The effective impedance looking is nothing, but parallel combination of R and R which is R by 2 right. So, this is R th Thevenin equivalent resistance is R by 2. So, now that we have both the Thevenin equivalent voltage and Thevenin resistance how do I how do I modify this or how do I redraw this circuit? I can, I can replace this circuit, which is Thevenin equivalent which will be nothing, but a Thevenin equivalent voltage source, a Thevenin equivalent currents, a Thevenin equivalent resistance and these are my output ports. So, this is equivalent to the output ports of the network and my R L gets connected here and the voltage that I will observe across R L right. The voltage that I will observe across R L is identical to the voltage that will that I will observe across R L in the original network right.

So, in our case what is Vth? In our case Vth is 1 volt, what is Rth? Rth is R by 2 right, right. So, now, if I let us go to the next page and if I redraw the Thevenin equivalent network what do I get? So, this is Vdd by 2, this is Rth, this is V naught, this is R L right. So, what is V naught? Vo is Vdd by 2 times R L by R L plus Rth. So, for Voto be almost

equal to Vdd by 2, what do I need to satisfy? We need to satisfy that R th has to be much, much less than R L and if R L has a range of, has a range that is R L can have a minimum value and a maximum value, what should Rth be? Your Rth should be your Rth should be less than R L min correct and in an example that we had taken, in the example that we had taken R L the range of R L was it was going from 100 ohm to 100 kilo ohm. So, if we were, if we were in charge of designing, finding out the values of R right, what would have been my constraint? My constraint would have been Rth should have been much, much less than 100 ohms or in other words Rth is R by 2.

So, R by 2 should have been much, much less than 100 ohms which implies that R should have been much lesser than 200 ohms right. So, if you can, if you can ensure that R is much lesser than 200 ohms then you are all set. So, you can ensure that the output voltage Vo for this network output voltage Vo for this network will remain at approximately V d by 2 for the entire range of entire range of R L ok. This is so far so good, but is there an issue is there an issue that you foresee with this type of implementation? There is indeed an issue and the issue is as follows. Now let us go back, let us go back to the original circuit that we started off with.

So, let us say this is 2 volt, this is R L and we sized R to be much, much less than 100 ohm, let us say we sized R to be 10 ohms ok. So, now what do you think, what do you think is the power consumption of this network or in other words what do you think is the power that I am or current that I am drawing from the battery? Now note that these 10 ohms are hard coded right, you are not changing these 10 ohms. So, when R L is let us say 100 kilo ohm right, when R L is 100 kilo ohm the effective resistance that you are seeing right, the effective resistance that is battery is seeing is 20 ohms because you can essentially neglect R L right. So, what is the, what is the approximate current that you are drawing? The approximate current that you are drawing is 2 volts by 20 ohms right. So, this is, this is approximately equal to 100 milli amps.

So, note that regardless of the value of R L right, regardless of the value of R L you will at least be drawing 100 milli amps through the battery and this is for maximum value of R L. If R L, if R L reduces you will be drawing more current maybe slightly more than 100 milli amps, but the key point to note here is that whether you have an RL or not in order to ensure that the entire range of R L is satisfied you will have to always draw 100 milli amps of current. But out of these 100 milli amps how much current is actually going into R L? So, what is I R L? I R L is approximately equal to this voltage Voor rather I R L is equal to Vo over R L and Vois approximately equal to 1 volt right that is what we designed it for. So, essentially this is 1 volt by R L and since R L varies from 100 ohms to 100 kilo ohms. So, I R L varies between when it is when R L is 100 kilo ohms the amount of current that I R L is drawing is 1 volt by 100 kilo ohm and when it is when R L is 100 ohms the

amount of current is drawing is 1 volt by 100 ohms.

So, this is this is nothing, but 10 milli amps and on other side it is this is 10 micro amps right. So, essentially your the load current for which you have designed this circuit is supposed to vary between 10 micro amp and 10 milli amps. However, in order to support this load current, you are drawing you are always drawing at least 100 milli amp current from the supply. So, what percentage of the supply current is actually going into your load? Only maximum 10 percent of the supply current is going into the load and the 90 percent is getting wasted right. So, clearly this is not a feasible solution or this is not a very power efficient way of making a voltage regulator right or rather a more rather more efficient way of expressing the problem here is the fact that this is an this is a power hungry way of setting up setting up a voltage regulator which can accommodate a variety of variety of loads.

Now why am I harping on this? I am harping on this because even though we are not at that stage of the course can you intuitively think of a solution, can you intuitively think of a architecture which can help mitigate this problem? Mind you I am not asking for a final architecture I am asking you to think in put yourselves in the shoes of a designer and think if this is the problem what can be the potential solution? Thank you for a moment and we will come back. Thank you.