Course name- Analog VLSI Design (108104193)
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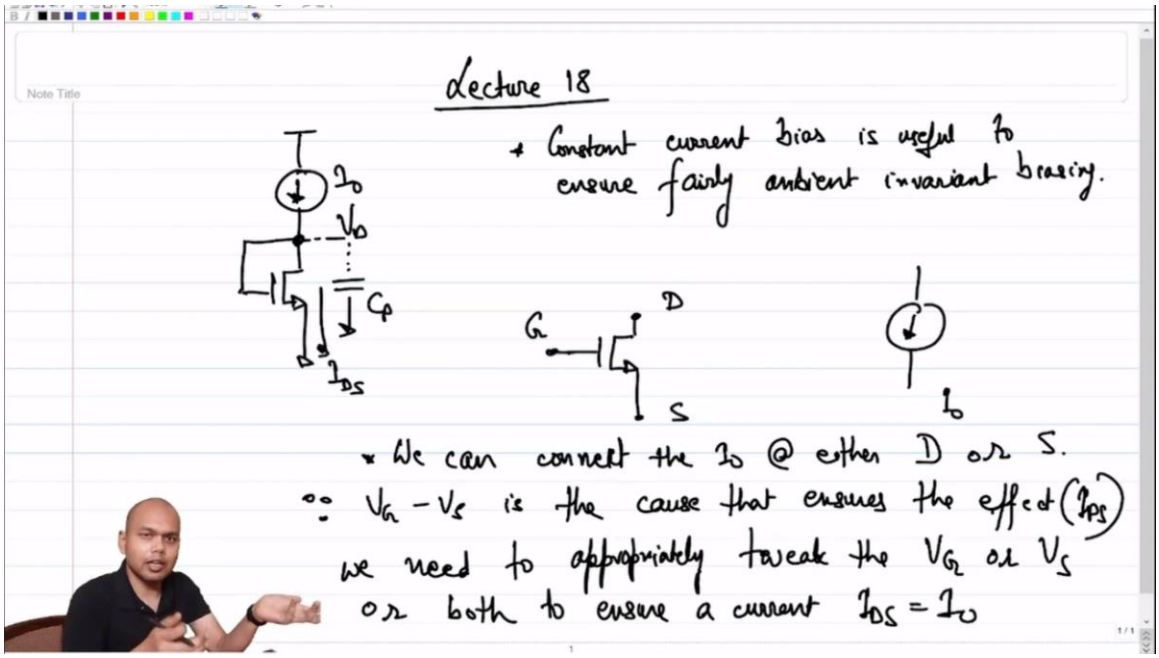
Week- 6
Lecture- 18, Module- 01

Welcome back, this is lecture 18. In the previous lecture, we were, we saw one of the ways of biasing a transistor using a constant current source. And what was the context? The context was, if we use a constant current source bias or in other words, if we use a constant current source to bias a transistor, then we are implicitly assuming that the overdrive of the transistor is fixed. Right? If the overdrive of the transistor is fixed, then naturally the gm of the transistor is invariant of any threshold voltage variation because overdrive is Vgs minus the threshold voltage, the overdrive is fixed, which means if the threshold voltage changes, the corresponding Vgs also has to change in order to keep the overdrive fixed. And how did we go about arranging the circuit? We argued that this can be done using the concept of negative feedback. And why using the concept of negative feedback? It was because we observed, we observed the voltage at the drain, right? We observed the voltage at the drain, we fed the current source at the drain of the MOSFET and we observed this voltage Vd and it always helps to assume that there is a parasitic capacitance Cp to understand which side the voltage at Vd might increase or decrease if there is a mismatch of current between I0 and the current that is flowing to the transistor.

In this case, we argued that if Ids were higher than I0, right? If Ids were higher than I0, then the voltage at Vd would have dropped, which essentially means that we have to do something to the transistor in order to ensure that the Ids becomes equal to I0. And what was the fix? The fix was to decrease the overdrive voltage because if we decrease, the information that we are attaining from the fact that Vd is going down is that the transistor has higher overdrive voltage than required, which means we need to reduce the overdrive voltage. So, how do I correlate the voltages of the drain and the requirement of the transistor? The correlation is if the voltage at the drain drops, I need to drop the, I need to drop the gate voltage also, right? Or the gate to source voltage also, but the source is here grounded, which essentially means that I need to drop the gate voltage. And what was the easiest way to do that? We saw that the easiest, most convenient way to do that was to connect the drain and the source, then we use this configuration to bias our common source amplifier, which was also supposed to be invariant threshold voltage, threshold voltage variations, right? Okay.

So, now the crux of the matter is that current source bias or rather constant current source bias, current bias is useful to ensure fairly robust biasing, right? So, we were exploring the

ways of, we were exploring the ways of setting up our transistor in such a way that we will be able to use a constant current source to bias the transistor. Now this, the one that we explore is barely one of the many possibilities. Why do I say so? Because note that the transistor has three terminals, right? One is the drain gate source and let us say I have this current source I0, what are the possibilities, where can I connect this I0 in order to ensure that the drain to source current of the transistor is equal to I0? One obviously is at the drain, the one that we explore. What is the other option? The other option obviously is to connect it at the source, right? So, there are two ways of connecting the current source, right? So let me remove it for the time being. So I can connect the, so we can connect the I0 at either drain or source, right? So fine, that is that, those are the two options, but in order to connect, in order to take an action, it is not like we connect the current source and the circuit will start working.

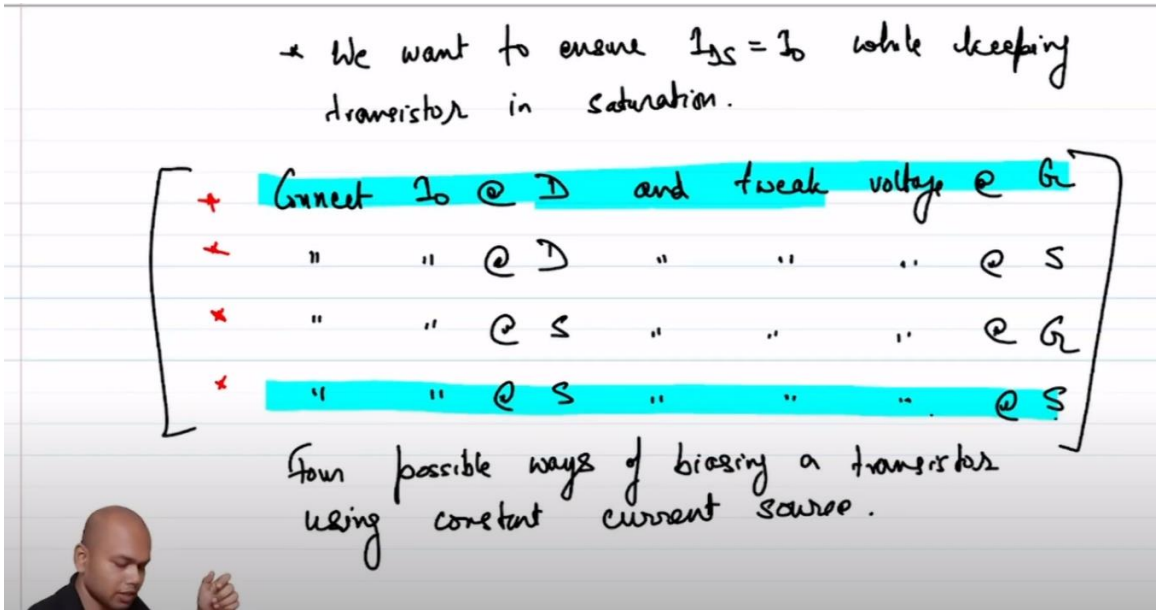


We have to take some action just like we did in case of drain, right? So we have to do something to the, we have to do something to the gate or the source terminals of the device, right? Because we know that since Vgs or Vg minus Vs is the cause that drives, that ensures the effect. What is the effect? Effect is Ids, that ensures the effect. We need to ensure or rather we need to appropriately tweak the gate voltage or the source voltage or maybe both, right? We need to appropriately tweak the gate or gate voltage or source voltage or maybe both to ensure a current Ids equal to I0, right? Just because you have connected a current source I0 into the drain or at the source I0, it does not necessarily mean that the transistor will be pushing or pulling this current in or out while being biased at saturation, right? So the whole context is to ensure. So this whole context is, why do we want to do this? We want to do this that we want to ensure Ids is equal to I0 while keeping transistor in saturation. Because if you use an ideal current source and you connect it to the drain or the source of the transistor, that ideal current source by virtue of KCL will, that current has to

flow through the transistor.

There is no doubt about that. However, we also want to ensure that while this current is flowing, while this current is flowing, the transistor is not going out of saturation region. That's why we are observing in the previous case, we are observing the voltage at the drain and we were trying to see whether the drain voltage is moving up or moving down, because if it's slightly moving up or moving down, then something bad can happen. By bad I mean the transistor can go out of its proper operating condition, right? So all these arguments are we are making, right? So in order to ensure that while the transistor is biased with a constant current source, it should also be in saturation. If it's not in saturation, you cannot use it as a, you cannot use that bias as an amplifier, right? So that's the whole context of it.

Okay, so now what are the, so we established that there are two ways of connecting the current source. We can connect the current source at the drain or we can connect the current source at source of the transistor. Then I mean, what are the ways of tweaking the gate to source voltage? We can either independently tweak the gate voltage or we can independently tweak the source voltage and we can do combination of both. Let's keep the combination of both argument aside for the time being. So let's say that we can either independently tweak the gate voltage or independently tweak the source voltage while connecting the transistor, while connecting the current source at either the drain or the source.



So how many possible combinations of applying the current source and tweaking the gate and source voltage can I come up with? Clearly, I can come up with four possible combinations, right? So the first combination was connect I0 at drain and tweak voltage at gate. This is what we did in the previous lecture. What are the other options? Obviously, the other one of the other options is connect I0 at drain and tweak voltage at source, right?

In principle, I can do that, right? How to do that is a matter of detail, we will have to look into it, but in principle, we can do that. Similarly, there is another option of connect I0 at source and tweak voltage at gate, correct? And what is the last option? I am just writing out the permutations, connect I0 at source and tweak voltage at source, right? So these are the four possible combinations by which I can use a constant current source bias to bias my transistor, right? So these are four possible ways of biasing a transistor using constant current source okay? So we have already seen this, we have already seen this. What I would like to do in this lecture, I would like to concentrate on the last one.

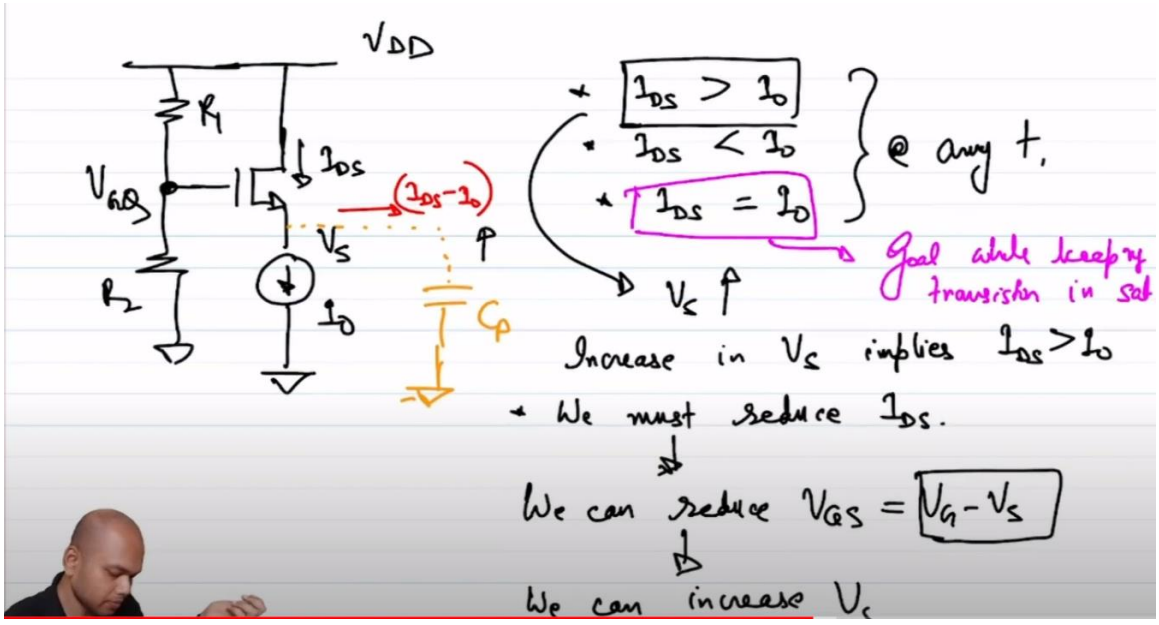
We will look into the other two sometime later in the course, okay? So let us look into the last one that is connect I0 at source and tweak the voltage at the source, okay? So the first thing is we have our MOSFET and the problem statement is I need to connect the constant current source at the source, right? And we have to do something at the source, right? We will do that but moment I say I am interested in the last configuration, what am I saying? I am essentially saying that I will not be touching the drain and the gate, right? That is the whole premise of connecting the current source at the source and tweaking at the source, right? So we will do something at the source, we have connected the current source at the source of the transistor. In this case, current is sinking, right? But let us stick to the terminology of current source. So we don't plan to do anything with the gate and the drain of the transistor. However, we know that the gate and the drains need to be biased, right? So let us say the drain is biased with VDD and clearly the gate also needs to be biased at certain voltage. What voltage? We don't know.

So let us assume it is biased with a certain voltage, right? So let us assume it is biased with a certain voltage. Let us say this is some R1 and R2 and let us assume this is some Vgq, okay? What is this Vgq? We will see. It is our job to determine what is this Vgq, what is the requirement of the Vgq but for the time being, let us assume that some gate voltage has been established, okay? So this becomes I0, okay? So now let us argue the same way we argued in the previous case. What was the argument? The argument was like before, let us assume some parasitic capacitance exists, right? So let us assume some parasitic capacitance exists. It helps us in seeing the effect, the effect of the voltage rising and falling without a capacitance, it becomes difficult to visualize the effect of voltage rising and falling, everything becomes instantaneous, okay? Right? So let us assume that, so let us assume that, so this is Ids.

So we have connected it in like this, the circuit is set up like this. So if Ids is greater than I0, right? What are the three possible conditions? So let me just write down, but the three possible conditions are Ids is greater than I0, Ids is less than I0 and the third one is Ids is equal to I0, right? So this is what at any time t, we would like to see, correct? So this is at any t, okay? So let us say I have turned on the circuit, right? What is it that we will observe?

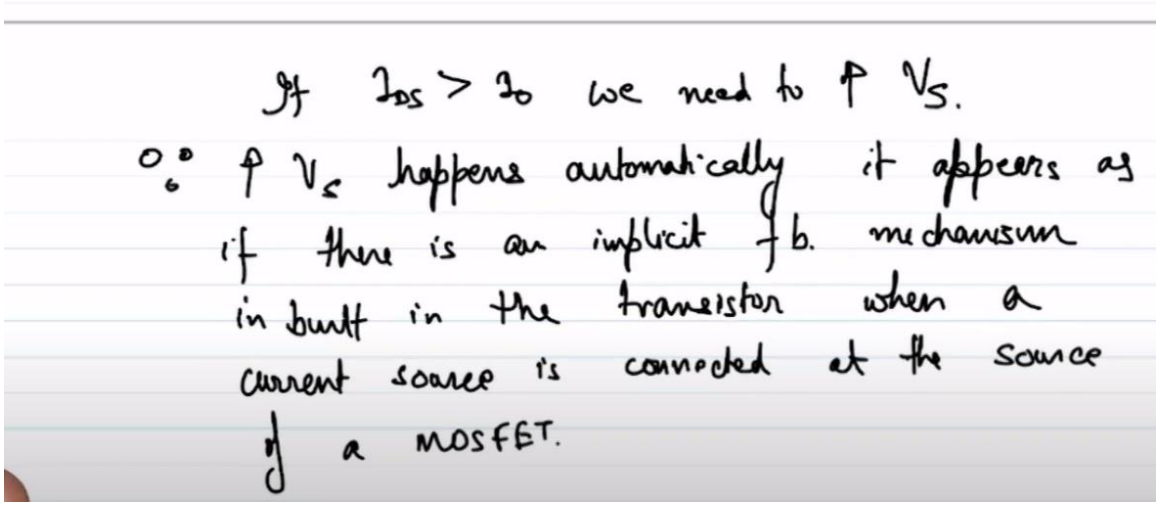
Let us consider the first case. So if Ids is greater than I0, what is going to happen? If Ids is greater than I0, clearly some current Ids minus I0 will flow into this capacitor, right? So if Ids is greater than I0, what information am I gathering? What information am I gathering? The information that I am gathering, I will be gathering by only observing the source voltage, right? So what is the source voltage? What will happen to the source voltage? The source voltage will increase. So source voltage will increase, right? So this, so just mark it like this. So the source voltage will increase, right? So I am considering this case, this is Es, Es will increase, right? So Ids greater than I0 will result in increase in source voltage.

If I flip the argument around, I would say that increase in source voltage will imply Ids is greater than I0, right? So if I flip the argument, what I am saying, increase in Es implies Ids is greater than I0, right? So if increase in Es implies Ids is greater than I0 and our goal is to reach Ids equal to I0, right? So this is the goal, this is the goal, right? While keeping transistor in saturation. So if Ids is greater than I0, what should I do? I should, I should take some corrective action to reduce the Ids, right? So what should we do? We must reduce Ids, right? Okay. So how can we reduce Ids? What control do I have? One can obviously say I can reduce the W by L of a transistor to reduce Ids, but that we cannot do, right? Because once the transistor size is fixed, it is fixed, we cannot change W by L. What else can we do? We can, in order to reduce Ids, we can reduce Vgs, right? Or Vgs is equal to Vg minus Vs. We can reduce Vg minus Vs, correct? However, Vg is equal to Vg cube is that.



So what can we do? We can increase Vs, right? So what is? So in plain English, what we need to do? If Ids is greater than I0, we need to increase Es, right? Similarly if Ids is less than I0, so okay, before I move into the next case, let me conclude this thought. So since if Ids is greater than I0, we need to increase Vs, we need to do something, right? We need to increase Vs. But what is happening to Vs if we do not do anything? If we do not do

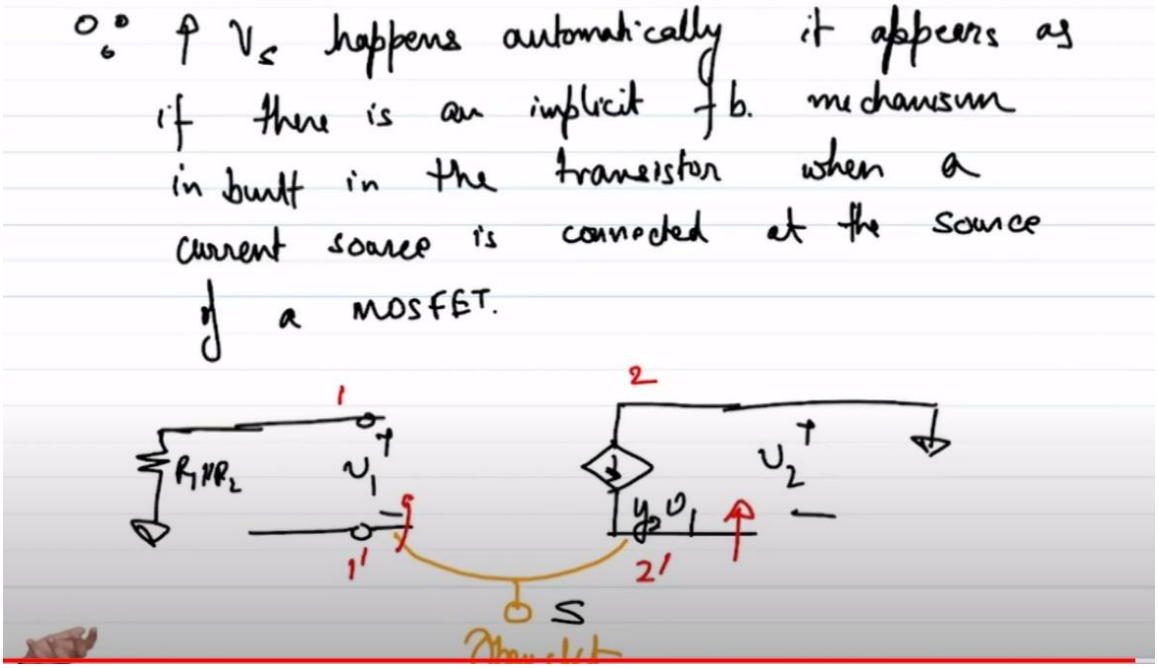
anything, Vs is increasing. So which means, which looks like by connecting the current source at the source in the way that I have shown here, the transistor has auto bias, right? So there seems to be an implicit negative feedback, an implicit feedback inbuilt into the operation of the transistor when we are connecting the, when we are connecting the current source to the source, right? So this seems like this is C, there is that, there is a, so since increase in Vs happens automatically, it appears as if there is an implicit feedback mechanism inbuilt into the operation in the transistor when a current source is connected at the source of the MOSFET.



So we can argue the same thing when we, if we assume that what happens if Ids is lesser than I0? So if Ids is lesser than I0, right? So if Ids is, let us say, if Ids is lesser than I0, if I use a different color, right? Then clearly a current of I0 minus Ids will flow out of the parasitic capacitance, which means the voltage will decrease, right? So when, so the decrease of the voltage at the source implies that Ids is lower than what is needed to be, which means I need to keep the transistor in the direction as to increase its Vgs, right? I have to increase the Ids, which means I have to increase the Vgs, since Vg is constant.

How do I increase Vgs? I have to reduce the source voltage and that is automatically achieved because if Ids is lower than I0, current will be pulled out of the, okay? So one might be curious and ask, right, why, I mean, in case of connecting that the, in the previous example, when we connected the current source to the drain, it seemed like everything, I mean, we had to do something, it was not as if things started to work automatically, we have to make a connection between the drain and the gate. But looks like in this case, we do not have to do anything, we just connect the current source at the source of the transistor and things will start to work. So what is happening, right? So as it turns out, if I, the answer to that is in the incremental two port network model of a transistor, right? So what was the incremental two port network? What was the generalized model of an incremental two port network? The generalized model was, I had or rather if I just restrict myself to the model where I had and only the Y21, right? So only gm or let me restrict myself to Y21, so this

is V1, this is V2, right? Okay, so this was the, so the two port, four terminal, this was the two port, four terminal model of a network. In case of a transistor, these two ports are connected together, right? And therein lies the magic. Why? Because note that when we put a current source, when we put a current source in the actual picture, in the total picture, what are we doing to the incremental picture? We are opening it, right? So this is open circuit here, correct? This is open circuit in the model of, in our transistor model, right? So if I have to complete the picture, so since the drain, what is the drain connected to? The drain voltage is grounded, right? What is the source connected to? The source is essentially open circuited, correct? So this is the source, the source terminal is open circuited.



What is happening at the gate? The gate is connected to a parallel domination of R1 and R2 and connected to ground because I have not connected any input, right? So essentially this becomes R1 parallel R2 connected to ground, correct? So where is this implicit negative feedback coming? The implicit negative feedback is coming at the source because if for example, this voltage, I mean if for example, this voltage increases for some reason the voltage at this terminal increases since the two terminals, let me call this 1 dash and 2 dash, it is 1, 2. Since the terminals 1 dash and 2 dash or 1 prime and 2 prime are connected together, if the terminal 2 prime increases, the terminal 1 prime also increases, right? So there is a transference of information from the output port to the input port through the connection in the source provided that the source is open circuited or provided the source is not grounded. In a common source amplifier, the source was always grounded. So this information was not getting transferred. In this particular configuration, since the source is open circuited, right, by virtue of the operation of a transistor, by virtue of the model of a transistor, there seems to be a implicit negative feedback that is existing all the time, right? Okay, so let us stop here. Thank you.