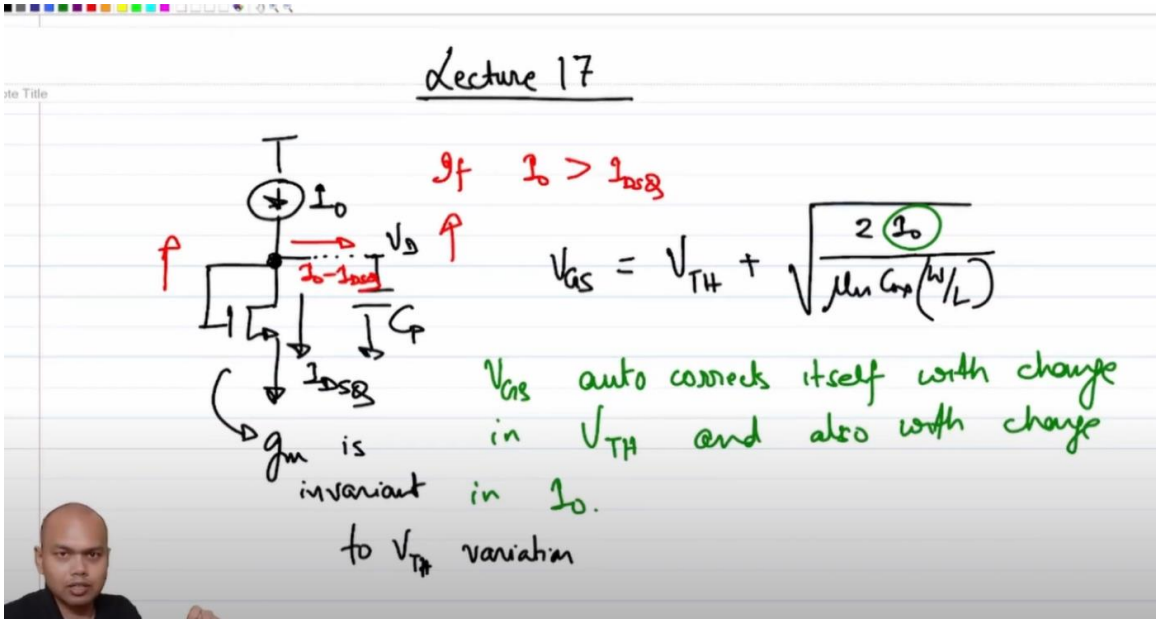
Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 6
Lecture- 17

Now, welcome back this is lecture 17. So, in the previous lecture we were seeing one of the examples of biasing a transistor with a constant current source and what was the motivation for that? The motivation for using a constant current source bias was that if we could bias a transistor with constant current source we saw that the gm the trans conductance of the transistor was potentially independent of any threshold voltage variation and also its variation with respect to mobility was minimal or lesser than the case where we bias the transistor with a constant Vgs right. So, naturally constant current bias is quite often the preferred way of biasing analog circuit amplifiers right. So, we were trying to see the reason behind we are trying to see the reason behind why what is the intuition behind the fact that a constant current bias was able to keep the gm constant right and what we saw was that one of the techniques of using constant current bias or one of the techniques of developing a constant current bias was to feed the current source right feed a current source directly into the drain observe the voltage at the drain right. What happens if the voltage at the drain is tends to increase with the voltage at the drain tends to increase what information am I gathering if the voltage at the drain is tending to increase the information that I am gathering is that the current that I am pulling out right. So, let us assume there is a small capacitance small parasitic capacitance Cp connected at the drain of the transistor you need not assume this always, but putting a memory element like a capacitor gives an intuition of time that gives an gives a feeling of feeling of time.

So, let us assume that at time t equal to 0 we had biased this transistor with a certain Vgq and we connected Io to the drain and the Vgq that we connected was such that the current through this transistor would have been Idsq and if Io were greater than Idsq what would have happened the voltage at Vd would have increased right. If Id for example, if Io is greater than Idsq what will happen a difference current of Io minus Idsq will flow into this capacitor. So, naturally the voltage at Vd will increase. So, what if I only observe the voltage at Vd what information am I gathering information that I am gathering is is that the transistor is not strong enough to pull a current of Io that is the information that I am gathering.

So, if this is not strong enough what should I do what knobs do I have I have the Vgs knob to turn right. So, what what do I need to do we need to if the transistor if Idsq is lesser than Io I need to increase Idsq which means I need to increase Vgs since Vs is grounded which

means I have to increase Vg right. So, in a in a sense if Vd is increasing we need to increase Vgq. So, then we saw that what is the easiest way to most convenient way of achieving that architecture the most convenient way of achieving the architecture is to simply connect the gate and the gate and the drain right. So, in this case naturally we also saw that the transistor will always remain in saturation because Vd is equal to Vg assuming the threshold voltage is greater than 0 right.



So, which almost always is the case in the types of MOSFET that we use. So, in that case your transistor will always remain at saturation and this is done using negative feedback right or this is done using feedback why this is done using feedback this is done using feedback because I am observing the output voltage what is output voltage this is drain is the output voltage I am observing the drain and taking a corrective action at the gate ok. So, then we also saw that the Vgs of such a configuration I mean Vgs of this transistoRcan also be expressed as threshold voltage plus under root 2 Io mu n Cox W over L ok. And from this also we got the intuition that if Io is constant right if Io is constant and mu n Cox W by L is constant then naturally Vgs will Vgs minus threshold voltage is constant which in other word other way of saying is that if the threshold voltage changes foRsome extraneous reasons then the Vgs will change automatically right. If the threshold voltage increases the gate voltage will automatically increase in order to adjust for that for that current Io right.

So, this other way of saying the same thing is Vgs auto corrects itself with change in threshold voltage and also with change in Io right. Why do I say that Vgs auto corrects with change in Io? Naturally I mean the same argument can be given with respect to Io if Io let us say foRsome reason Io has increased right what will happen? If Io has increased and let us assume Idsq has not then naturally the drain voltage will start to increase and because the drain and the gate are connected together the gate voltage will also increase

thereby increasing right. So, this is equivalent to saying there is a Vgs auto corrects or auto adjusts or auto biases itself if you connect your transistoRin this configuration right. So, the example that you can I mean real life example that you can think of is I mean completely non-electrical example is let us say you want to buy a birthday gift for your friend you do not know what gift will please your friend. So, you can do one or two things you can either take a gamble right buy one buy some gift and give it to your friend your friend might like it might not like it.

The alternate thing to do is to ask your friend upfront what gift do you want if your friend tells you what gift you oRshe wants then you go and buy the same thing and present it right. So, assuming that your friend told you the right thing to start off youRshe will be will be happy with the gift right. So, this is equivalent to the example in this is you are asking the transistor to develop its own voltage in order to set up in order to sink in the current Io your requirement is you need to sink in the current Io you do not know what Vgs to give right. So, you are asking the transistor what we tell me what Vgs you want so that current of Io can be sunk in the transistor says fine connect it in this format and I will give you the adequate Vgs now you change Io the Vgs will also also change ok great. So, what is the moral of the story the more why are you doing all these things we are doing all these things because in this case this is gm is invariant of threshold voltage variation right or invariant to threshold voltage variation and also gm of this transistor is not as sensitive to mobility variation as it was in the constant voltage bias case ok.

So, but note that we need to we need to ultimately make a common source amplifier right. So, in a common source amplifier what is ouRconfiguration. So, let us we know that ouRconfiguration for the common source amplifier is this we needed how do you bias the input we needed to bias the input in the first place with some Vgsq and that Vgsq cannot be a voltage source right oRcannot be a constant if this is constant then you have trouble right the trouble was a gm was strongly had a high dependence on threshold voltage and mobility. So, now, what solution do I have all I am saying is that this Vgsq cannot be cannot be a fixed voltage, but the Vgsq has to be such that I sink in a current which is let us say equal to some Ids let us say this current has to be this current has to be Io I am looking forward to generating a Vgsq which is such that we senses the current Io and gives me that Vgsq right. So, what is the new problem statement the new problem statement is we are looking for a way to generate Vgsq which is exactly of the value required that is required to generate a current Io through let us say M1, but it has to auto adjust with respect to change in threshold voltage or Io right.

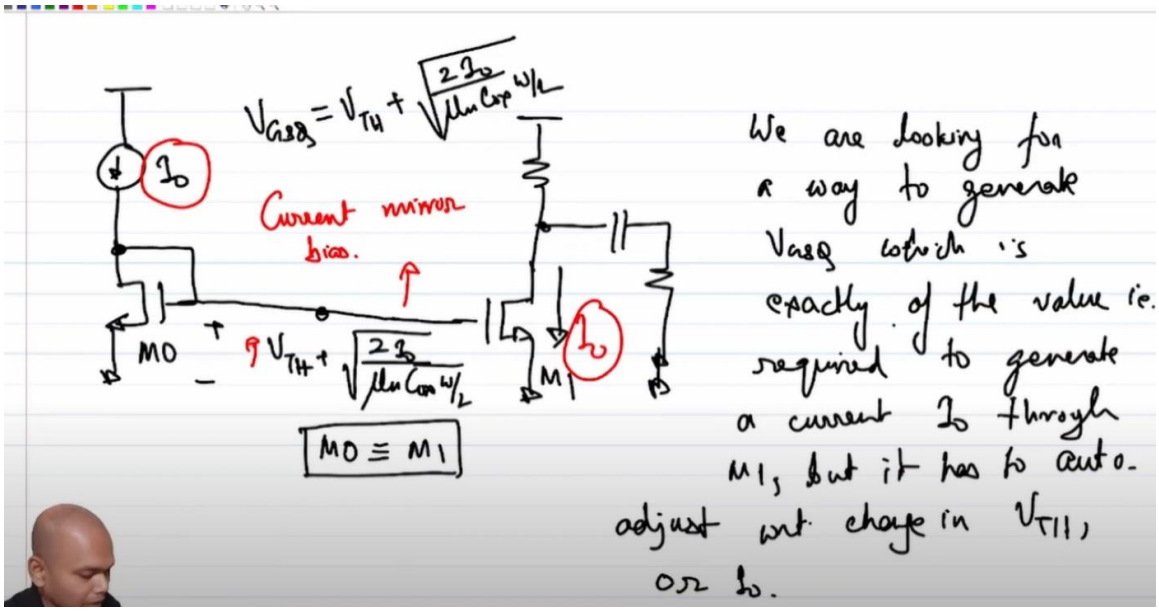
So, essentially this is what we are looking for and this is what we saw in the in the previous lecture right. So, what is the benefit of this if we can do this then naturally the gm of M1 will be invariant of any threshold voltage variation ok. So, how do I do that? So, what are

we looking for we are looking to generate a Vgsq we are looking to generate a Vgsq whose value is threshold voltage plus under root 2 Io by mu n Cox W over L right. How do I generate that? We have just now seen in the previous page how to generate that right and obviously, we have to assume that we have a current source available because ultimately we are planning to do a constant current source biasing right. So, then how do I generate this Vgsq let us say I take another transistor and let us say this is Mo and the I assume that Mo is exactly equal to M1 they are identical to each other which essentially means that the threshold voltage of Mo is exactly equal to M1 the mobility of Mo is exactly equal to M1 right.

So, let us assume that we have a transistor and we plug in the current source and connect the drain at the gate what will be this voltage? What will be this voltage that will be generated? This voltage will be exactly equal to the voltage that is required that the transistor M1 is looking for in order to generate a bias which is in which is which will give me a constant which will give me a gm which is invariant of threshold voltage variations right ok. So, which essentially means that what I need to do I need to essentially connect these two terminals ok. So, now, when I connect these two terminals what is this Vgsq? Vgsq is this voltage essentially becomes threshold voltage plus 2 mu naught by mu n Cox W over L and now you see if threshold voltage changes if threshold voltage changes then nothing changes right I mean this threshold voltage changes threshold voltage increased by 100 millivolt if threshold voltage increases by 100 millivolt this gate voltage of M1 also increases by 100 millivolt right while keeping thus keeping Vgs minus the threshold voltage constant or in other words thus keeping the overdrive voltage constant. If you keep the overdrive constant Io remains constant if Io remains constant your gm remains constant with respect to any threshold voltage variation and this seems to be a good way of good way of biasing your common source amplifier. Note that I have not yet applied the signal this is still in the biasing stage ok.

So, now, I made certain assumptions what assumptions did I made? One primary assumption that I made was Mo is exactly equal to M1 right. Now, as it turns out here in comes the primary difference between a circuit design which is made using discrete components on a breadboard and a circuit that is made in an integrated in a way for in an integrated environment or in a VLSI design right. So, what is it? What is the primary difference? When you are designing on a breadboard let us say you purchase one MOSFET from your vendor and you purchase another MOSFET from some other vendor or maybe from the same vendor there is no guarantee that those two MOSFETs will have identical characteristics right. So, however, in a in a in an integrated circuit environment as it turns out in a very small area you can pack in large numbers of transistors. Now, as it turns out the variation of threshold voltage within a small area is minimal.

Similarly, the variation of mobility within a small area is minimal which essentially means that there is a large amount of correlation or matching between transistors in an IC in an integrated circuit environment when they are placed very close to each other right. Since there is a large amount of correlation or matching between transistors when they are placed very close to each other depending upon how you put them in an integrated circuit it is it can be expected that the threshold voltage of adjacent transistors which are placed close by and also having similar sizes will have almost near identical threshold voltage and mobility right. So, this is a beauty of integrated circuits and that is why these type of configurations can often be used. So, there is one more nomenclature for this circuit and this is also called a current mirror circuit. The reason it is called current mirror is if you concentrate on only the currents that is flowing the current in the left branch is Io, current in the right branch is also Io.



If I change the current in the left branch from Io to let us say I1, what will happen to the current in the right branch? The current in the right branch would also change from Io to I1 why because the moment current in the because the moment current in the left branch changes, it changes the VGS of Mo thereby changing the VGS of M1 and how much it will change? It will change by the exact amount that is needed to sink in a current of I1, right? So, hence the current in the right branch is mirroring the current in the left branch and hence this is also called a current mirror bias, this is also called a current mirror bias, ok. Ok, great. So, now, we have I mean we have figured out a way of biasing our let us say a potential common source amplifier in a way whose gm does not change with threshold voltage and gm is quite less sensitive or yeah quite less sensitive with respect to mobility variation. So, now, the next question is how do I how do I apply an input? Ultimately I mean this is the bias picture ultimately we will also have to apply an input, right. So, let us let us see that.

So, this is our output side of the common source amplifier has not changed. So, the analysis and the output side is exactly whatever or the synthesis of the output side is exactly whatever we had initially we had initially envisioned, but now we have now we have a now we have a problem to solve and the problem is the fact that I have a incremental voltage Vi and a source resistance Rs. I have to add it to this network such that such that I have to add it to the network such that incrementally the voltage that develops across M1 is equal to Vr, right. So, what am I looking for? So, let me let me remove this RL part because that is not giving me any extra information for the purpose of this discussion and unnecessarily taking a lot of space let me remove that. So, what are you looking for ultimately we are looking for a configuration in which ouR incremental model of our common source amplifier should look like this.

So, this is Rd. So, this is Vg. So, this is gm times Vg or gm times Vi. This is what we want, right. Incrementally this is the gate should I mean the source should be shorter, right.

This is we want. So, the question is how do I how do I where do I connect this Vi and Rs. Now, clearly this Vi and Rs has to be connected at the gate of M1. There is no doubt about that because ultimately this here we see this Vi and Rs being connected to the gate. I mean that is what a common source amplifier is where the input is applied between the gate and the and the source.

So, let us do that. So, what happens if I let us say I put Rs here and let us say I connect it here, right, right, ok. So, now, what do you think is going to happen? Will this work or will this cause a problem? So, now, moment you edit a circuit, right, moment you change a circuit by connecting something to somewhere you have to go back and do two things. You have to go and see whether it has changed its quiescent biases, right, because ultimately the quiescent biases changes then I mean nothing will work and numbeR2 is to see whether it satisfies the incremental picture, right. So, the let us see let us see if the quiescent bias has changed, right. So, in order to figure out if the quiescent bias has changed what do I need to do? I need to null the any incremental signal.

So, I ground Rs, right, I ground this part. What do you think has quiescent bias changed? Clearly it has changed because when Rs was not when this extra contraption was not there what was the current that was flowing. So, let me connect it here then I will be able to make the point in a better way. So, what was the current that was flowing through this branch when Rs was not present? When Rs was absent, right, when Rs was absent this current was clearly 0, right, because into the gate of M1 we were seeing a capacitoRsince the capacitor gives you infinite impedance at DC.

So, this current was 0. Now, what is going to happen? Now, we have an Rs what is going

to happen? Now, depending on the value of Rs there will be a current division. So, some part of I0, let us say alpha times I0 will flow into Rs. I mean you can very accurately find out what is alpha times I0 you can simply write out the equations, right. So, let us assume that if you have a if this develops a voltage Vg, right, this develops a voltage Vg the current through M0 will be current through M0 will be half nu n Cox W over L Vg minus threshold voltage whole square and the current through Rs will be Vg plus Rs Vg over Rs. So, Vg over Rs this has to be equal to I0 and then you this is a quadratic equation you solve the quadratic equation and you will get a value of Vg.

But the key thing to note is that the current I0 is not flowing into M0 only, current I0 is flowing into Rs also and if the value of Rs is small then most of this current I0 will flow into Rs, right and naturally the current into M0 will become much smaller than I0. Naturally, if the current into M0 becomes much smaller than I0 the current in M1 will also become much smaller than I0 because M0 and M1 are current mirror circuits, ok. So, we cannot do this. So, what is the what will be the solution? So, we already have done this in other perspective in other cases where we do not want a DC current to flow, right. So, what is the issue? We do not want any DC current.

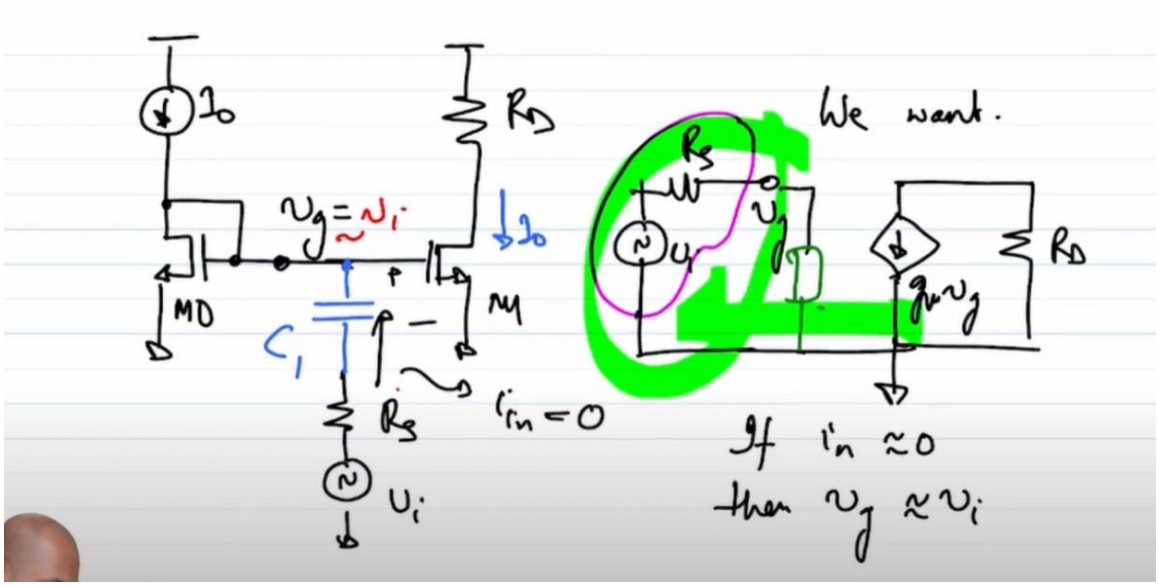
So, we have this Rs, we have this contraption of Rs and Vi and we do not want any DC current to flow. So, what contraption can you think of that prevents the DC current from flowing? Clearly a capacitance will do the job, right. So, let us put the capacitance, let us put the capacitance. So, if I put a capacitance and I mean let us call this capacitance C infinity, right. Let us call it C1 for the time being then we will call it C infinity later, right.

If I have this if I put this capacitance C1, right. So, then does it disturb the bias point of M0 and M1? Clearly it does not, right because now all the current still that all the all of I0 flows into M0 creates the appropriate voltage to at the gate of M1 which is required to set up the current of I0 in M1. So, this current still remains I0. So, good, right.

So, this is good news, right. So, what about so this is as far as the biasing picture is concerned. What about the incremental picture? So, what is again what is the goal? The goal is to ensure that we have to design it in such a way that this voltage is almost equal to Vi, right. Ultimately we want ultimately we want this configuration to get materialized, right. So, our goal is again still to ensure that the gate voltage of M1 is almost equal to Vi. So, which essentially means that we have to figure out if there is if there is a if there is a loading effect in the in the incremental picture, right.

So, if let us say no current where being no incremental current where being drawn through this path, right. So, let us say this is I in if I in incrementally where 0, right. If I in where 0 then Vg would be equal to Vi, right. So, let me write it down. If I in is almost equal to 0

then Vg will naturally be equal to Vi.



This is our goal then, right. So, we have to ensure that we have to ensure that nothing loads nothing loads this contraption of nothing loads this contraption of Vi and Rs right. Nothing loads this contraption of Vi and Rs. If something loads this contraption of Vi and Rs which means that in the incremental picture I will have in the incremental picture I will have some loading which means Vg will not be equal to Vi right which means I will not be getting an output current of gm times Vi right. So, so then let us figure out whether this is loading or not right. So, how can I figure this out? So, let us go to the next page ok.

So, let us see this in the incremental picture what is Vg how will I know what is Vg in the incremental picture? So, clearly first thing we have to see is what is the impedance looking into the node Vg correct. So, we have a capacitor. So, we are interested to find out what is the impedance looking in right. So, is this infinity or is this something else? So, let us see right let us do an analysis and see. So, what should I do assuming that I mean M1 is in I mean I mean we do not have to assume anything.

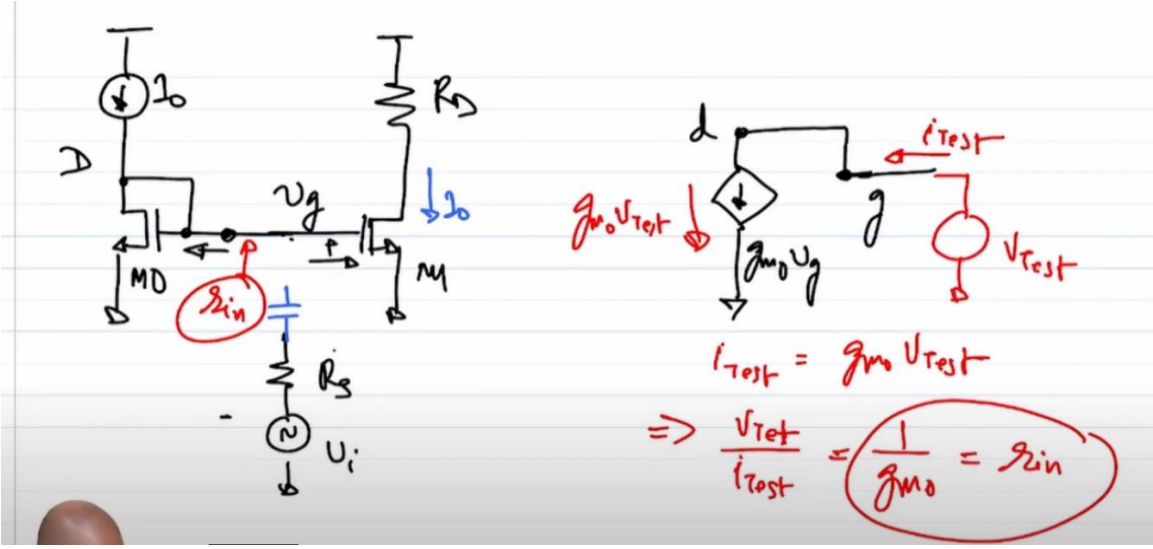
So, let us do the brute force analysis and see right. So, what will be the what will be the impedance to the right into the gate of M1 is infinity. So, we do not have to bother right. So, it is almost as if M1 does not exist what is the impedance to the left? So, this we have to see right. Now, if you see is not going to the it is not only going to the gate right looking to the left I mean looking this side right.

So, so we are not only seeing the gate of a transistor and we are not only seeing the gate of M0 we are also seeing the drain of M0. So, then and the gate and the drain are connected. So, we will have to do an analysis to see whether what is the impedance looking to the left. So, what will be the impedance? So, let us do let us replace the contraption of M0.

So, M0 again it is in saturation. So, I can replace the source is grounded right. So, source is grounded. So, this this is gm times whatever the Vg is right. So, this is drain right.

So, this is this is the drain. So, this was the drain right. What about the current source? What should I do with the current source? So, the current source here clearly goes off because in a incremental sense the the constant current source is an open circuit right. What about the gate? Clearly the drain and the gate are connected together because that is how it is connected in case of M0. So, this is gm0 Vg not gm Vg because I mean I had wanted to distinguish between gm M0 and M1 transistor. And what are we looking for? We are looking for what is the impedance looking in.

So, how do I find out impedance? We have done it multiple times before. So, let us put in a test voltage right. If I put in a test voltage and I try to figure out what is the test current the ratio of Vtest or Itest will be my impedance. So, if I put in a test voltage what is Vg? Vg is Vtest.



So, what is this current? This current is gm0 Vtest. So, this current is equal to Itest. So, Itest is equal to gm0 Vtest which means what? Which means Vtest over Itest is equal to 1 oveR1 over gm0 right. So, which means this is the this is the Rin this is this Rin and you see this Rin is is far from being infinity right. If we if we desire large values of gm in order to desire large gain then clearly you see that 1 over gm0 will not be large if gm0 is large right. So, this so if I connect this contraption of Vi Rs in this capacitor then it will clearly load ok.

So, what is what is the solution? So, let us let us see. So, clearly this is not possible. So, because this is loading so, to do something. What is the problem again? The problem again is looking in your Rin is not large right. So, what should I do? What should I do with what should I do in order to in order to ensure that the contraption to the left does not load load

the incremental contraption. So, what did we do in case of in case of a common source amplifier when we were doing voltage biasing? We had put this R1 R2 contraption right.

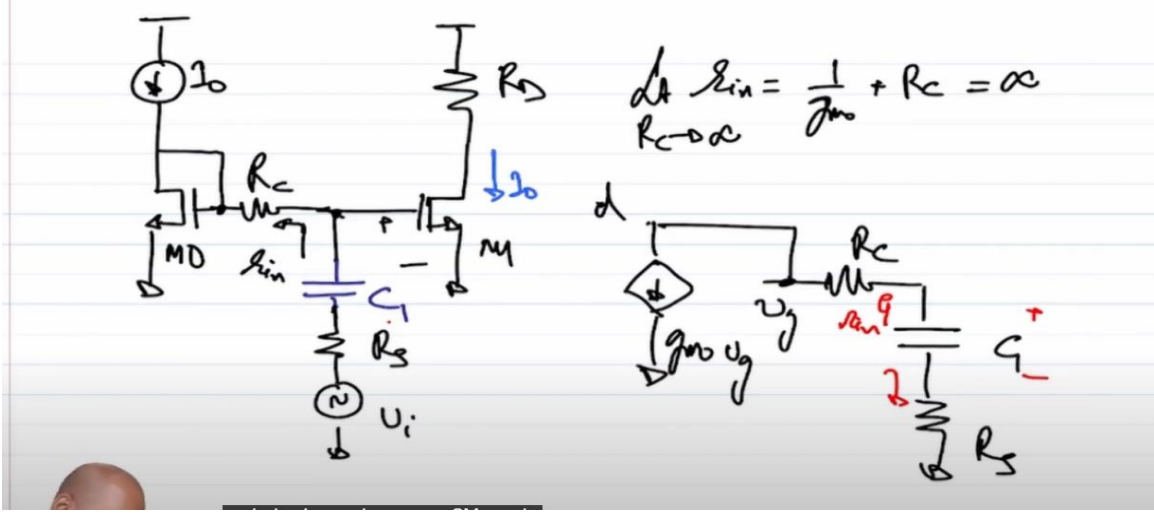
We had put this R1 R2 contraption in order to what was that R1 R2 contraption doing? We were not we were not fixing the voltage at the gate of a transistor with a constant voltage source because it was it would not have allowed the voltage at the source voltage at the gate to change. Similarly, if we if we assume that gmo is very high gmo is infinity right. If gmo is infinity what is Rin? Rin goes to 0 which means that if for a very large gmo this is almost a short circuit right. This is almost like a voltage source. So, what was the remedy in the earlier case when we are designing common source amplifier? The remedy was to isolate the voltage source from the incremental source with a with a resistance right.

So, so the same thing we can do here we can put a large resistance say Rc right. So, we can so we put a large resistance Rc where Rc let us say tends to infinity right. If Rc tends to infinity what is the impedance looking in? So, clearly the impedance looking in now is what is Rin now? Rin will be whatever Rin we had earlier that is 1 over gmo plus Rc and pass it tends to infinity then dividing value of Rc really Rin when Rc tends to infinity is infinity. So, then we are all good to go which means that I can essentially now connect connect the other side of the capacitor to the gate of to the gate of M1 without any without having any any problem correct. So, now we are not loading now we are not loading the incremental source at all fine, but now a moment somebody says that is something is infinity in the earlier cases we saw Rc is infinity in this case capacitance is infinity in this case I am saying Rc is infinity again Rc infinity is not possible correct.

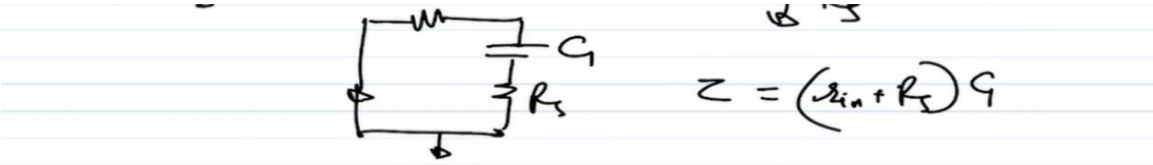
So, just like a capacitor infinity is not possible then we need to figure out what is the constraint on on Rc C1 these extra components that we have included in the circuit in the network we need to figure out what are the values of those right. So, if we can figure out the values appropriately then we should be fine. Now note that we need not bother about that DC part at all because the impedance given by the capacitor is actually infinity right that is one constant that is actually infinity. So, this is the impedance given by the capacitor is actually infinity we did not bother about the DC part we only have to bother about the AC part right. So, what should I bother about like before what do I need to see I need to see the time constant of the of the network right time constant of the circuit from the perspective of the capacitor ok.

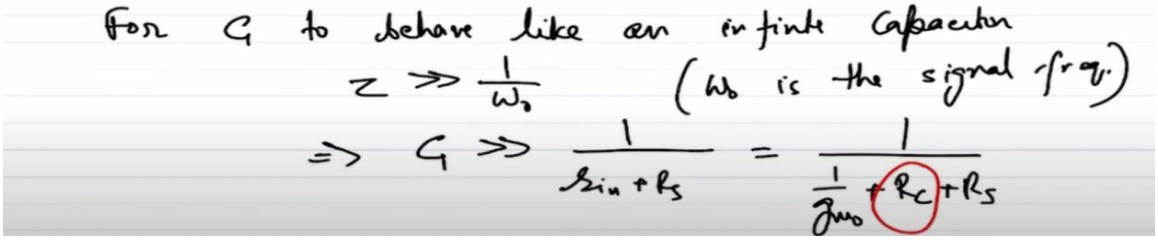
So, if I find out the time constant of the network right it is a single capacitor loop what is the loop incrementally what is the loop. So, so if I if I sketch this circuit once again. So, this is let us say gmo Vg this is the drain drain and gate are connected this is Vg then you have Rc right then you have C1 then you have Rs ok. And we are trying to figure out the

time constant since we are trying to figure out the time constant I got rid of Vi right when I got get rid of Vi which means Vi goes to 0 which means it becomes a short circuit right. So, now what is the time constant of this circuit now clearly in order to figure out time constant I have to see what is the Thevenin equivalent what is the Thevenin equivalent impedance looking from both the both the terminals of the capacitor C1 right.

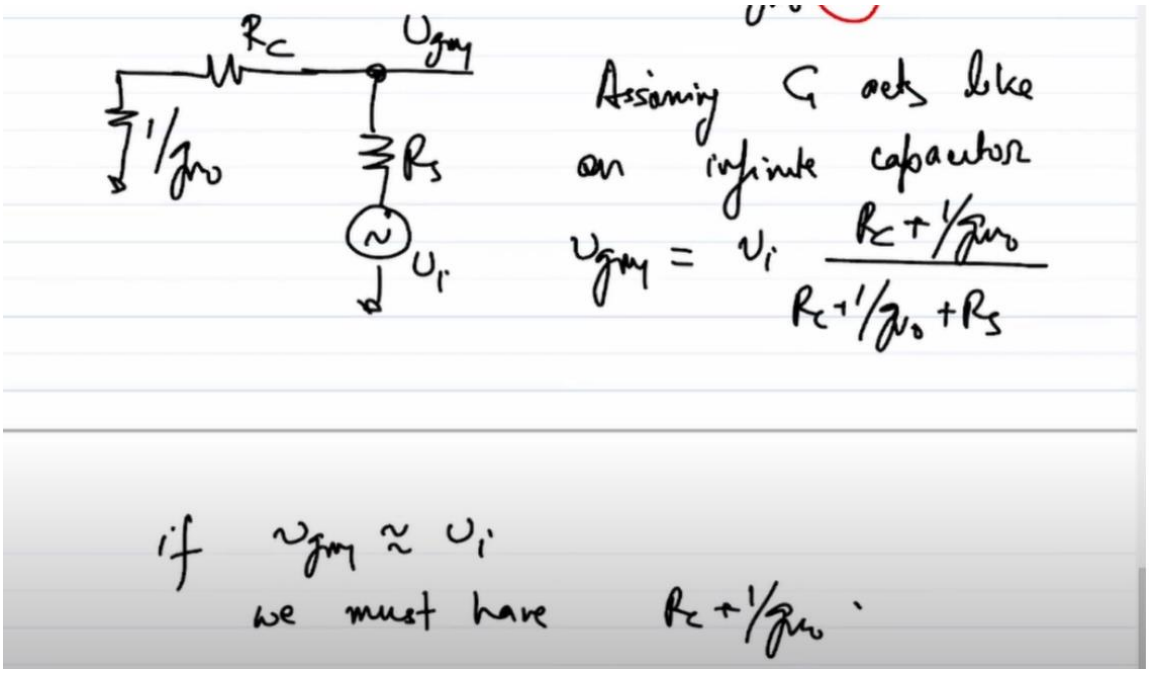


On the bottom side this is Rs on the top side what is this on the top side what do I see top side I see Rin right top side I see Rin and what is Rin Rin is 1 over gmo plus Rc correct. So, essentially again equivalent network becomes Rin this is grounded you have C1 this is Rs these two are rounded which means I can close the loop right. So, what is the equivalent what is the capacity what is the time constant tau is Rin plus Rs times C1 right. So, in order for in order to ensure in order to ensure that in order to ensure that the signal passes through the capacitor without any hindrance right in order to ensure that the signal passes through the capacitor without any hindrance what should I ensure. So, we should ensure that foRC1 to behave like an infinite capacitor we need to ensure tau is what tau is much much greater than 1 over omega naught where omega naught is the signal frequency which means that the constraint on C1 becomes C1 has to be much much greater than 1 over Rin plus Rs what is Rin Rin is 1 over gmo plus Rc plus Rs right.



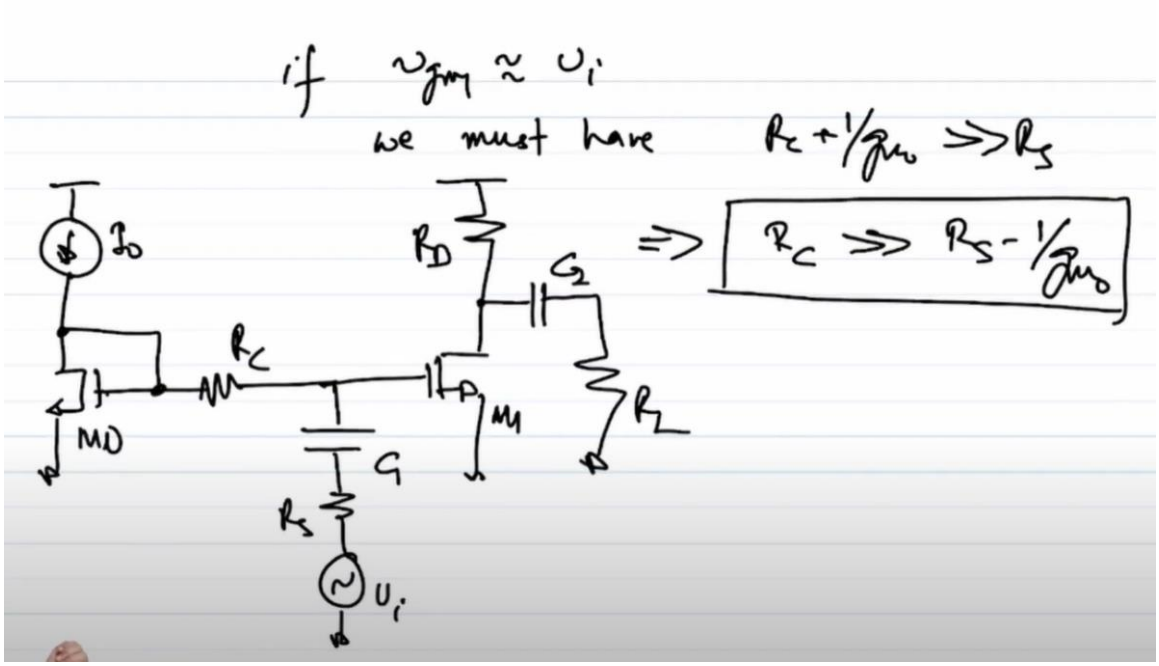


So, this is the constraint on C1 that you need to satisfy, but now you will ask me the question what is Rc because how do I know what Rc is also something that we have incorporated how do I know what is the value of and what is the constraint on Rc and that would be a perfectly legitimate question and let us let us answer that also. So, let us assume again let us assume that your we have we have been able to size C1 such that C1 acts as a short circuit ok. So, if C1 acts like a short circuit what does the incremental picture look like now. So, let me sketch that incremental picture again. So, this side becomes Rs and this is Vi this is the node that I am interested in right because I have M1 here on the left side I have Rc on the left side I have Rc and I have this contraption of this transistor whose gate and drain are connected and what was the impedance looking into this node into the gate of this contraption right because the gate and drain is connected this is it was 1 over gmo ok.



So, essentially this becomes 1 over gmo right. So, let us say Vg M1 we need to figure out what is the constraint on Vg what is the constraint on Rc such that d g M1 is almost equal to Vi right. So, what is the constraint assuming C1 acts like an infinite capacitor what is the constraint on Vg M1. So, Vg M1 or rather what is the constraint on Rc for that we have to see right what is Vg M1 Vg M1 is Vi times Rc plus 1 over gmo by Rc plus 1 over gmo plus Rs right. And if Vg M1 has to be equal almost equal to Vi what do I need to ensure we must have Rc plus 1 over gmo be much much greater than Rs or Rin other words we need to ensure Rc is much much greater than Rs minus 1 over gmo ok.

So, if we can ensure this then we are good to go ok. So, this you can all this you can also figure out without writing equations because ultimately what are we looking for if we say that Vg M1 almost has to be equal to Vi essentially what we are saying is that this additional contraption that we have should not load the contraption of Vi and Rs because this should



not load which means its own impedance whatever impedance this extra contraption had which is Rc plus 1 over gmo has to be much much greater than Rs right. So, as long as we as long as we satisfy this we will be will be fine right. So, essentially what is what is the final configuration that we have a common source amplifier with a current mirror bias becomes now we can put back the output side also. And the values of you would by now we know how to choose the values of C1 C2 Rc and so on right. Let us stop here. Thank you.