Course name- Analog VLSI Design (108104193)
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Lecture- 16, Module-1

Welcome back, this is lecture 16. So, in the previous lecture we were looking into the architecture of a common source amplifier where we used capacitors in place of to replace the multiple batteries that are required in order to bias the transistor and apply the voltage, apply the incremental voltage simultaneously. And the architecture that we ended up with was the following. So, note that we have only one voltage source VDD, the bias at the gate of the transistor is being derived from the resistor divider network formed by the resistors R1 and R 2. At the gate of the MOSFET no current is getting diverted, no DC current is flowing this side or that side there is absolutely no DC current because in both sides one side I see a capacitor which is open at DC on the other side I also see kind of a capacitance of the MOSFET which is again open at DC which means that I do not have to worry about loading right. So, nicely my R1 and R2 network will be able to provide the appropriate bias for the transistor.

How are we, and then we saw that we needed to apply we needed to apply a DC ,we needed to apply the incremental input also and needed to ensure that the gate of the transistor has swings with the entire almost the entire incremental input. So, for that what we needed we needed a, we needed a battery, we needed a battery between the gate of the MOSFET and the input source. What was the role of the battery? The series battery was supposed to, was supposed to give us a lift in voltage right. So, then we saw that a series battery we cannot use a battery in series because of multiple reasons then we were the observation that a sufficiently large capacitor can act as a battery.

Initially, we notice that an infinite value of capacitor will do the job. So, we put C1 to be equal to infinity and we coupled the input Vi and Rs and by the way this type of coupling the input from one side of the capacitor plate to the other side is essentially is also called AC coupling right. Very often if you talk to circuit design professionals they will sometimes say why do not do AC couple your input when one says why do not do AC couple your input. It is implied that you understand that there is probably a coupling capacitor which is being used to which is being used to store a different DC voltages on either plates. However, the role of the capacitor is to pass the input pass the incremental input as and when it appears in one of the places.

So, this is what exactly this capacitor C1 is doing. So, the C 1 is holding on to a DC voltage of Vdd times R2 by R 1 plus R 2, but also C1 is large enough it is not storing any AC voltage across it right. It is not storing any incremental voltage across it because if I infinitely large a capacitor essentially will look at the short circuit right. Then we notice that I mean we how long can we theoretically we can deal with infinitely large capacitance, but ultimately we are circuit designers we will have to make circuits and you cannot get a capacitor with infinitely large value. So, we needed to figure out what is the constraint on the capacitor.

So, that I can use a finite value of capacitance and yet mimic the role of an infinite capacitor. Then we saw that one way to approach it is to we saw multiple ways of approaching it, but it seems like the time constant method of approaching it is the most intuitive one. What was the time constant method of approaching? The time constant method of approaching it was if this is a first order network all we need to ensure that the time constant associated with the capacitance is much larger right than 1 over omega right. So, this was where omega was the frequency of interest. So, this was essentially the crux of I mean one of one major outcome of the previous lecture, then we shifted our focus to the output side and again we saw that there was a constraint that R L is the load R L need not necessarily be a explicitly defined resistive load where you have access to both the terminals.

The RL can be an implicit load of a next stage where you probably had only access to one terminal and the other terminal is probably implicit ground or maybe something else. So, since you have only access to one terminal you cannot put that RL between the drain of the MOSFET and the source and the power supply. So, that job has to be done by a separate resistor RD and we again AC coupled the value the resistance R L. When I say AC coupled why did we need to AC couple? We needed to AC coupled because the quiescent voltage across a resistor which is rounded at one side is 0. However, the quiescent voltage at the drain of the MOSFET is a finite value.

Now, if I connect these two together obviously, the resistance RL will draw DC current. In other words the resistance RL will load the network. We did not want it to load what was the one way of fixing that? One way of fixing that is to lift the quiescent voltage of across, leave the quiescent voltage on one I mean or one way to fix that was to make sure that the quiescent voltage on both the sides like the MOSFET side on the resistor side are identical. One way to do that was to put again a series battery across I mean in series with the with the resistor such that the value of the battery is exactly equal to the quiescent voltage of the MOSFET at the drain of the MOSFET. Then again we saw we know that putting a series battery is not possible, but by now we already know that there is a solution what is the solution put a very large value of capacitance.

So, we say that we will put a very large value of capacitance arguably an infinite value of capacitance and then we will want to figure out I mean then we saw that this probably gives us what we want right. So, now, when we stop we did not evaluate what will be the constraint on the value of C 2 right. So, now, in this lecture at least at the beginning of this lecture I would like to evaluate what is this what is the constraint on C 2 because like C1 I cannot assume C 2 to be infinitely large right. So, what is one way of going about it the most obvious way of going about it is to write the entire transfer function and then see what is the constraint in C 2 such that the drop across C 2 is negligible right. So, what we want we want under AC circumstances when the signal is swinging this entire contraption should behave like as if the capacitors were not there in the network in the first place right.

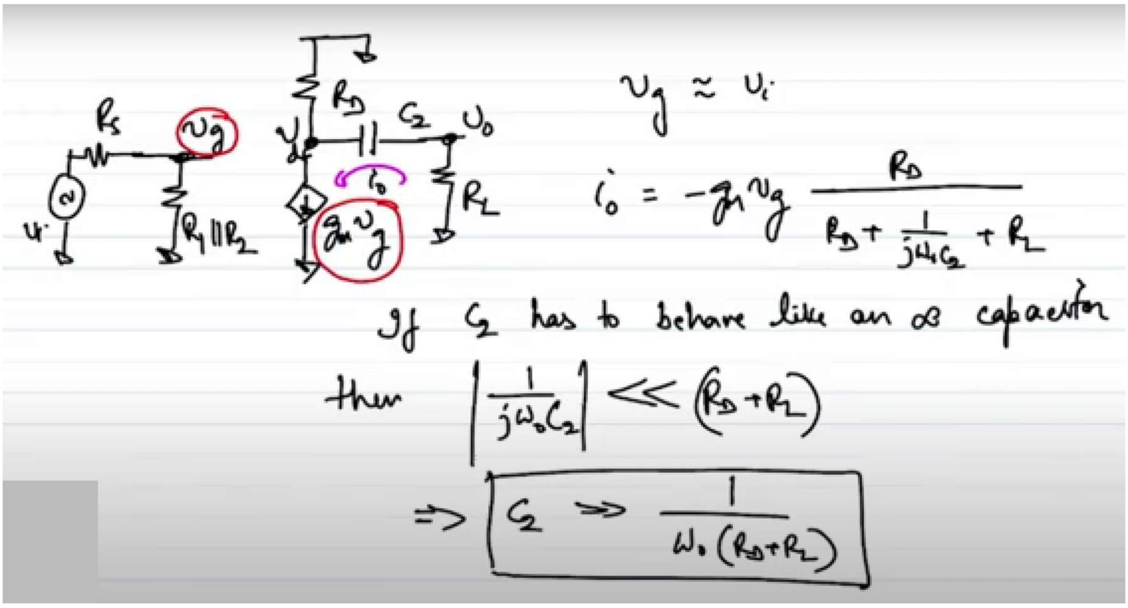
So, if I, if we sketch the incremental equivalent of this network what will we get, we will get this is Vi this is Rs and let us assume that C1 is large enough to be treated as a short circuit right. If C 1 is large enough to be treated as a short circuit this becomes R 1 parallel R 2 right because V d d is grounded in incrementally V d d is grounded. So, this voltage is Vg what should I replace the MOSFET by what is the assuming that the MOSFET is biased in saturation what is the incremental equivalent of the MOSFET the incremental equivalent of a MOSFET is only gm times Vgs what is the source? Source is grounded. So, essentially this becomes g m times V g what happens to resistor R d this remains as is the top of the resistor is grounded because a DC voltage source Vdd in an incremental model is grounded then what happens here we have this capacitor C2 and we have the resistance RL correct. So, and V naught is the voltage across RL that we are interested in.

So, what is V naught over V i? So, what we need in order to figure out V naught over V i? In order to figure out V naught over V i we need to know what is the value of this current because this is the current that is flowing into part of this current is flowing into RL to develop the voltage Vi. So, what does this voltage depend on? This voltage clearly depends on Vg right this voltage depends on Vg. So, what is V g? Vg is nothing, but Vi times R 1 parallel R 2 by Rs plus R1 parallel R 2 right and if you go back to lecture 15 what did we, what comment did we make on sizing these values of R 1 and R 2 we made the comment that we understood that we would want the entire signal to appear at V g right. Why do we want that? We want the entire signal to appear at V g simply because you would want maximum gain we want Y 1 1 of this entire contraction to be 0 which means that we do not want this R 1 parallel R 2 to load our load the input source right. So, if R 1 parallel R 2 is much greater than R s V g becomes approximately becomes equal to V i ok.

So, V g becomes V i what happens to so let me let me copy this. So, V g is approximately equal to V i right. So, now, this focus shifts completely to the to the output side right this is the drain this is the V d. So, what is the what is the voltage across R L? So, clearly this part of this current part of this current g m V g flows into R into I mean the current gets divided at the node V d right. The g m V g comes at so g m V g is flowing downwards.

So, if I say if I want to argue from the perspective of what is the current flowing upwards then minus gm Vg is flowing upwards. So, - gm Vg arrives at the node Vd and part of it has to go right and part of it has to go top right. So, what part of it will go to the right? So, clearly the we know this is, this is like an impedance divider. So, the part that will go to the right that is I naught let us say this is I naught this will be minus g m V g times R d over R d plus 1 over S C 2 or rather 1 over j omega naught C 2 plus R L correct ok. So, now from there, from here what can we what will be what constraint on C 2 do we get? Clearly we see that if C 2 has to behave like an infinite capacitor then 1 over j omega naught C 2 mod of this has to be much much less than R d plus R L right.

So, if C 2 were infinite then the denominator root simply have been R d plus R L right. So, we are trying to figure out what is the constraint on C 2 so that it behaves almost like an infinite capacitor which means the constraint on C 2 becomes, C 2 should be much much greater than 1 over omega naught R d plus R L right. This is this is a pretty straightforward you do you basically follow KCL and you do the algebraic manipulation and you arrive at that right. However, we know a more easier way of arriving at the same arriving at the same result we discussed this in the previous lecture and what was the discussion about the discussion was from the perspective of time constant. It is not always easy or it is not always intuitive to write out the full blown transfer function and then try to figure out what will be the constraint on various capacitances.



In fact, I mean if you want to do that you can do that in principle and you will get a good close from solutions, but sometimes it becomes too exhaustive analysis. So, engineers found out multiple ways of reducing the analysis analytical burden on our mind right. So, we one of the ways of dealing with first order networks is to look at the time constant of the network and coming to conclusions and we saw that in the in lecture 15 and what did we see? We saw that if we look at only the time constant of the network right or if we need to figure out a constraint on the value of certain capacitance all we need to do is to find out what is the Thevenin impedance the capacitor is C right. If I sit on the capacitor and I see what the Thevenin impedance it is C then I will be good right. So, what is the Thevenin impedance or Thevenin resistance in this case across C2 what will you do? Firstly moment I asked you to find or anybody asks you to find resistance or output resistance impedance or whatever then the first thing to do is to desensitize all sources.

So, in this case V1 goes to 0. So, V1 goes to 0 means this gets shorted. So, let me also short all the grounds together because it gives a good visual representation of what is actually happening. So, if the input is shorted what comment can you make on the voltage Vg? Vg clearly is equal to 0 if Vg is equal to 0 what comment can you make on the control current source gmVg this clearly goes to 0. In other words that does not exist if it does not exist what do you see? You see only what is remaining the only stuff that is remaining is this loop correct the only stuff that is remaining is this loop ok.

So, what is the, and if you are sitting if you are trying to figure out what is the Thevenin impedance looking on both sides of the looking from the capacitance what are you essentially saying? I am saying that this is the port right. So, this is the port across which I am trying to measure the resistance and how do you measure a resistance? You apply a test voltage V test correct. You apply let us say I apply a test voltage V test and I find out what the test current is. So, in this case clearly the test current will be V test over Rd plus RL right. So, this test current I test will be equal to V test over Rd plus RL.

So, in other words in other words R Thevenin will be V test over I test which will be equal to Rd plus RL which means what? Which essentially means that the time constant tau is C2 time constant tau associated with C2 right, time constant tau associated with C2 which is tau 2 let us say is equal to Rd plus RL times C2 right. And if you want the capacitor to act as a short circuit which means you want the capacitor to be large enough what is the constraint? The constraint is this time constant has to be much much greater than 1 over the frequency of interest right. Or in other words you would want you would want any signal at a frequency omega naught to pass through the capacitor without seeing any voltage drop or in other words you would like the capacitor to act as a short circuit as a frequency of interest right. So, which essentially means that you get the constraint C2 should be much much greater than 1 over omega naught Rd plus RL right. Note that we have come to the same conclusion using both analysis.

$$\Rightarrow R_{th} = \frac{V_{Test}}{i_{Test}} = R_D + R_L$$

$$\tau_2 = (R_D + R_L) C_2 \gg \frac{1}{\omega_0}$$

$$\Rightarrow C_2 \gg \frac{1}{\omega_0 (R_D + R_L)}$$

The reason I have I am doing this multiple analysis repeatedly at this stage of this course is because I am trying to I am to, I am trying to give you an give you an idea that it does not matter from which direction you approach the problem you will essentially get the same same answer. Going forward what I will do I will drop the transfer function analysis in order, to figure out what the capacitances are I will resort to only time constant based analysis because as you will see as a circuit gets more and more involved it is much easier to figure out what the time constants are rather than trying to, trying to put together entire transfer function all the time ok. Thank you.