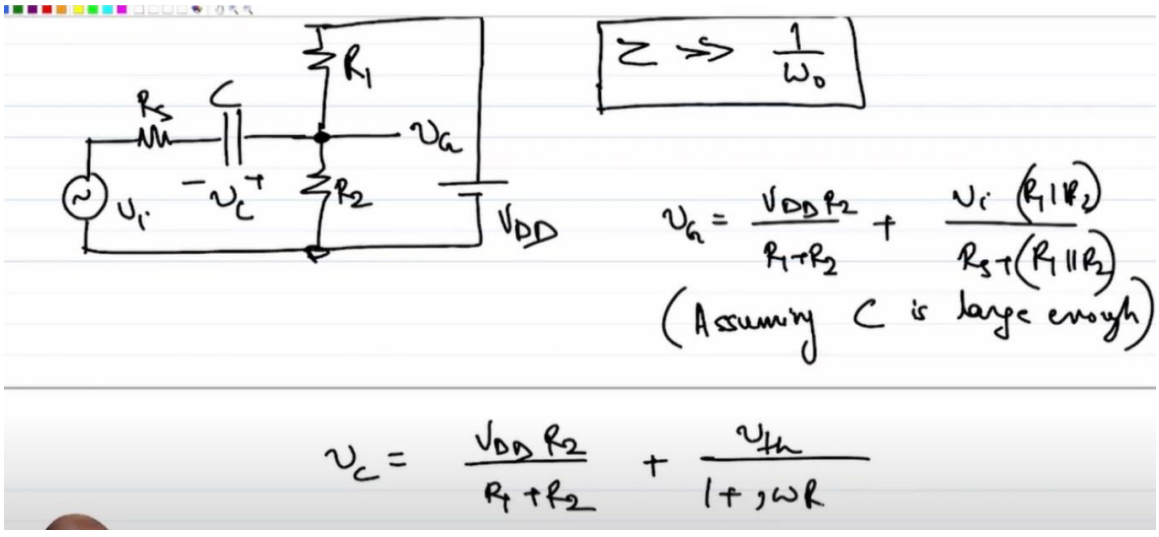
Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 5
Lecture- 15, module-02

Welcome back. So, what is the conclusion of whatever we discussed to quickly recap. So, if you have a structure like this, what we and we want, we want the capacitor to act as a short circuit at the frequency of interest right. And so, what will be the, what will be the voltage at this node, what will be the total voltage vg, the total voltage vg will be and I can use superposition because completely linear network, what will be the superposition of this B, we have two sources one is Vdd, one is Vi right. So, if I assume in case of superposition, I take one source at a time and de-energize the other source, both are voltage sources, de-energizing a voltage source is essentially equivalent to, is essentially equivalent to shorting it. Let me connect everything together so that it makes a bit more sense right.

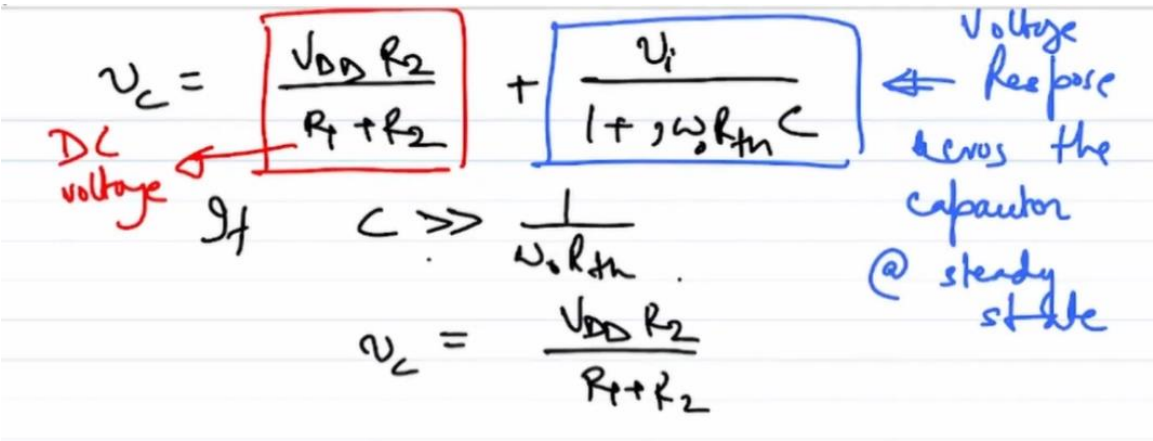
So, if I assume that Vi is shorted, what will vg be? vg will be Vdd times R2 by R1 plus R2 and if I subsequently assume Vdd is shorted, what will be gb? This will be, if I further assume that the C is large enough to be treated as short circuit, so this will be approximately equal to Vi times R1 parallel R2 by Rs plus R1 parallel R2 right. This is assuming C is large now right. So, what is the assumption, what is the total voltage across the capacitor? What will be the total voltage that we will see across the capacitor? Let me mark the voltage in this direction, let us say Vc. So, what will be the total voltage across the capacitor? Vc will be again I can do superposition right.



So, what will be, if I assume Vi to be de-energized, Vc will be what? Vc will be simply

Vdd times R2 by R1 plus R2 and this is expected because that was the quiescent voltage that we anyways wanted. Now what is the effect of Vi? Again because I am using superposition, I can short Vdd, by short Vdd R1 and R2 come to come parallel to each other. What will be the voltage then? Voltage across capacitor will be nothing but whatever we saw in the earlier example will be V Thevenin by V Thevenin by 1 plus j omega Rth times C ok. And V Thevenin in our case was Vi right, V Thevenin for the capacitor was Vi and if this is omega naught, if C is much much greater than 1 by omega naught Rth right, then we see will be R2 by R1 plus R2. So, as you see if the if you if we if we follow the rules right, if we if we if follow the sizing rules of the capacitor, what we will see is that the capacitor is only holding is only holding the DC portion of the information right.

So, this is the DC portion of the information and this is the AC portion of the information right. So, this is amplitude or rather this is the response voltage response across the capacitor right, voltage response across the capacitor at steady state. When I say steady state what I mean is that you have your Vi is a sinusoid, you have applied the sinusoid and you have waited for infinite time, no transients we are talking if there is no transient effects that we are talking about here. So, the voltage across the capacitor is Vi by 1 plus or rather the voltage response of the capacitor is Vi by 1 plus U omega naught Rthc and this the other one this this one is essentially the bias at that bias voltage of the capacitor is holding right, the DC bias or DC voltage we simply say DC voltage. So, as you see the capacitor is doing two jobs here, one is it is holding the DC voltage across it and also it is allowing the AC voltage to go through ok great.



So, now that we have the biasing picture at the input side, let us redraw our common source amplifier right. So, what is our common source amplifier now? Let us go to a new page. The common source amplifier now at least at the input side is looks to be sorted. So, this is Vdd and this is Rn. So, is I mean seems like if I size C R1 and R2 accordingly right, it looks like I mean all our problems are solved we should be and if we take the output, if we take the output from this node it looks like we are good to go right, but the question is are

we? As it turns out there is a slight bit of complication and the complication is again a practical one that remember I told you that there is a problem that you cannot have access to both terminals of a source right.

Similarly, you need not necessarily have access to both terminals of a load because what is this RL? What is this RL? This RL might not be might not be a actual register, this RL might be the input impedance of another stage that it is driving. So, which essentially means that you only have access to one terminal of the load and not the other terminal that you will just connect it to Vdd right. So, essentially the problem is we seldom have access to both terminals of RL ok. So, which means that your RL is just like your source your RL one terminal you can assume it to be implicitly grounded right and you have access to this terminal which means you cannot put RL between the Vdd and the drain of the transistor ok. So, now what should we do? Input side we did something to figure, but what should we do with the output side? Note that the first condition, what is the first condition? The first condition is that we need to ensure that the transistor is in saturation right without that we do not have any story to tell right.

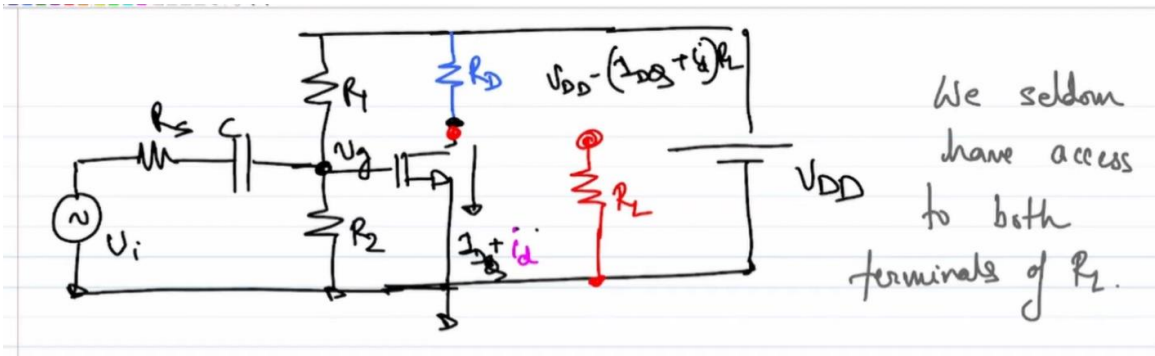
Without that you cannot make the amplifier work like that or you cannot make the transistor work like an amplifier simply because I mean go back to the small signal model of an amplifier the gds or the Y22 or the gds has to be equal to 0. If the transistor is not in saturation that is not possible hence it is a big problem right. So, what is a again if we go back to our drawing boards what is a easiest way of ensuring the transistor is in saturation? One is to say that I will directly connect and that train to train to the Vdd ok right. So, then what should we do with RL? How should I connect how should I connect RL because ultimately what is the what is the incremental equivalent of this? What is the incremental current the increment the what will be the total current of the transistor? Total current will be I d plus an incremental current right some dl I or let me say small id. The small id will be gm times Vg right gm times Vgs where s is grounded.

So, it is basically gm times Vg and if you are done a good job in in biasing the input side Vg will be approximately equal to Vi then essentially the incremental current distilled id plus capital id plus small id or let me say idq plus small id, but where will this id flow? Where will this incremental current flow? This incremental current clearly will flow into the into the Vdd right because incrementally this Vdd is in a short circuit right. So, this id will mark id with my gender color. So, this clearly this id will flow into the Vdd and whatever you do with RL you will not be able to generate any voltage across RL right. So, earlier how do we solve this problem? We put the RL in the path of id, we put the RL between the drain and the Vdd. So, the id had no other option, but to flow through RL since id was flowing through RL it was generating a voltage proportional to id and we were we were reading that voltage out, but now as I said since we do not have access to both

terminals of RL we cannot put RL in the in the path of id.

So, what is the solution? Ok. So, if this cannot be done this cannot be done firstly I mean firstly the first things first we cannot expect to get anything out of this if drain is connected to Vdd right. If drain is connected to Vdd all the incremental current id right this magenta id will always go to Vdd. So, we have to first things first we have to prevent that. So, how do you prevent that? How were you preventing it earlier? From drain being shorted to Vdd we prevented that earlier by connecting a resistor in that case it was RL, but in this case let me say it is not RL let me call this Rd I mean nothing innovative D it stands for drain I am connecting it between drain and Vdd.

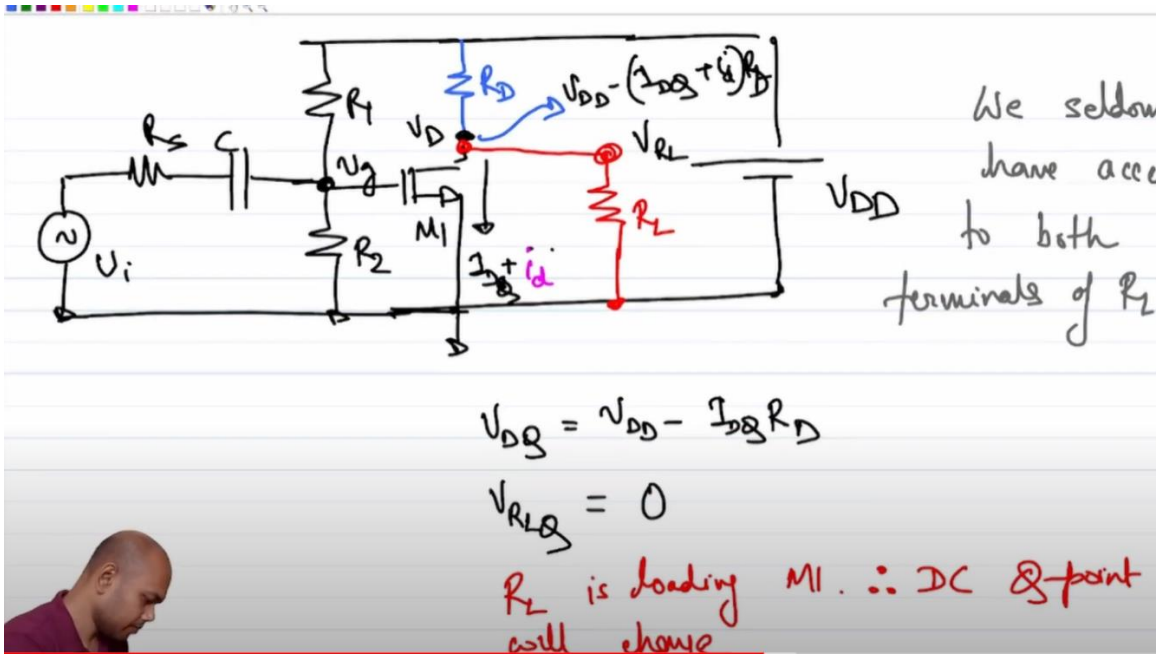
So, I am calling it calling it Rd ok. So, now this drain what will be the what will be the drain voltage I mean this is nothing, but the common source amplifier with Rd instead of RL. So, what will be the drain voltage here? What will be the total drain voltage here? This will be Pdd minus id Q plus id times RL correct ok, but ultimately what do I want? I want I want the id to flow into flow into RL right. I want id to flow into RL because ultimately I want the voltage to develop across RL right. So, how do you think can you can you suggest a way so that if not the full id part of the id flows into RL well one way to say is that I can I have one possible way is simply to connect the drain of the transistor to RL right.



Then one might be tempted to say that this part of this id part of this id will flow into RL and part of this id will flow into Rd right. So, if not I mean earlier we are not getting anything now we are getting something this might be a this might be a decent solution right, but even before jumping into that conclusion let me let me let me now point you point out a important problem with this with this type of if you simply connect RL to if you simply current RL to the drain right. So, what is the problem? Let us let us start again from the beginning let us assume the RL was not connected what was the what is the what is the voltage? So, what is the voltage at the drain? The voltage at the drain is Vdd minus this right. So, let us let us forget about let us forget about the incremental id right. So, the voltage quiescent voltage let me call this Vd.

So, Vdq was Vdd minus idq times this is not RL this is Rd I am sorry Rd ok. So, what is

the voltage across RL? Let me call it VRL what is VRL? VRLq is equal to 0 right if VRL is equal. Now, what will happen if I connect these two? What will happen if I connect these two nodes? If I connect Vd and VRL forget about the incremental forget about the incremental current what about the DC current? What will happen to the DC current? So, clearly some part of the DC current some part of the DC current that was coming out of coming through this will now flow into flow into RL right. What is the problem? The problem is then the value of Vd will drop the drain voltage will drop because now you are essentially loading the drain you are essentially loading the drain voltage with loading the drain with RL in the in the biasing picture also right. So, why again why are you loading? Because the moment you are connecting RL to Vd you are drawing current out of that mode right.



So, what is the crux of loading? If you are drawing current out of a load of a node after you have connected a load the load the resistance is loading the loading the net. So, here you are using RL you are you are loading your common source amplitude right. And what will happen if you load it will draw some current out whatever biasing you had envisaged earlier right after carefully writing out the equations will go for a toss the transistor will might not remain in saturation if you not careful right. So, what is the what is the problem? The problem is RL is loading loading M1 right RL is loading M1 therefore dc few points will change it is loading in the dc picture as well right ok. So, let us draw this redraw.

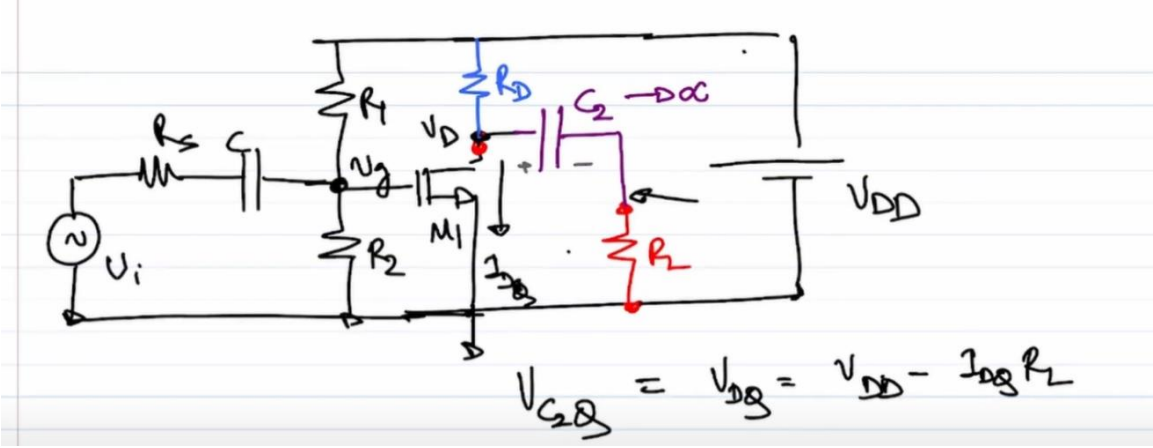
So, let us see what is the problem. So, let us forget about id for the time small id for the time being the problem is this is loading right. So, what is the solution? So, let us say I knew a priori let us say I knew a priori the voltage at Vd is Vdq right. So, let us say I knew this voltage is Vdq and somehow after I figured whatever Vdq was right I put a battery let me do this. So, let us say I knew this voltage is Vdq Vdq equal to id I mean Vdd minus id

Rd right and I somehow I figured out what the battery what the value was and I put a battery Vdq between I mean in series with RL right.

So, what is the voltage here now? The voltage here now is Vdq right. So, now if I connect these two nodes what is going to happen do you think any current will flow through that blue line to that blue where no right because both sides of the where where at identical potential to start off right. So, there is no need current only flows from a higher potential to lower potential in order to equalize the in an attempt equalize the difference in voltages. Since there is no difference in voltage no current no DC current will flow right. Since no DC current will flow my the quiescent point of the M1 will not get will not get happened right ok great.

So, let me let me make it a slightly better drawing. So, what is the solution that we come up with? The solution that we come up with is put a identify whatever voltage Vd was Vdq and put that put that value would put that put a include a battery of exactly that value Vdq. Now some of you might get angry with me and say that a half the lecture you have told us that I mean I cannot use a floating battery and how come I am using a floating battery certainly. You are absolutely right we cannot use a floating battery, but now we have a replacement. What is the replacement? An infinite capacitor right.

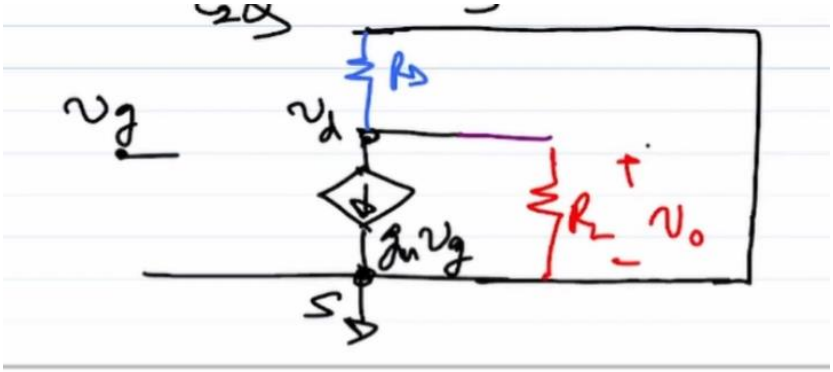
So, instead of using Vdq what will we use? We will use a we will use a capacitor right. So, we will use a capacitor let me call this C2 and let us assume C2 tends to right. So, if I use C2 and I use C2 tends to infinity right. So, what will be the voltage what will be the voltage across C2? What will be the voltage across C2 under DC condition right. So, voltage Vc2q that is a Vc2q the q stands for quiescent what will be Vc2q? So, clearly at DC capacitor is open circuited no current will flow.



So, what is this voltage? That voltage is 0 what is Vd? Vd is Vdq right. So, Vc2q is Vdq which is Vdd minus Idq rel right. So, the so note that by putting a capacitor we are not disturbing the we are not disturbing the quiescent point of the other transistor right. If we can ensure that we are not disturbing the quiescent point of the transistor that is a good start

right. The RL is no longer RL is no longer loading the quiescent point of your a quiescent operation of your transistor ok great.

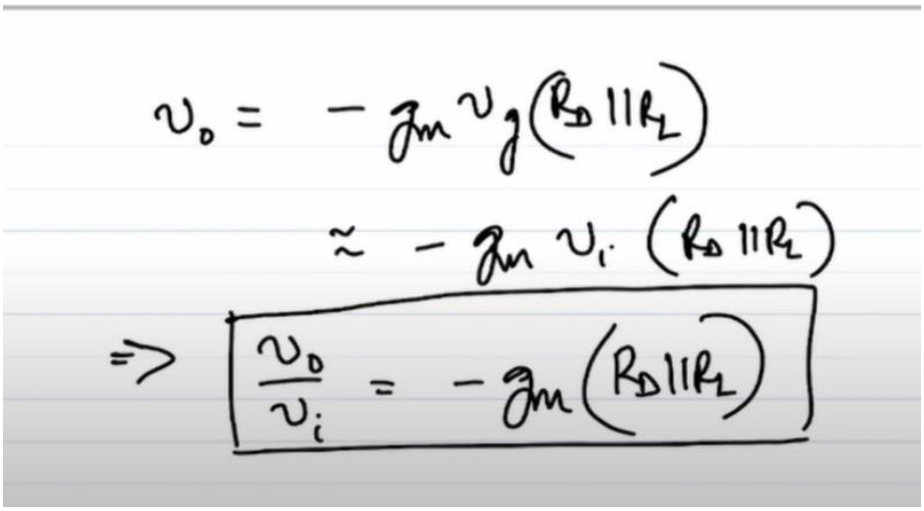
So, what about the AC condition right. So, let us sketch the AC equivalent right before we go into the AC condition let us sketch the AC equivalent. Let us assume the gate is at Vg what is the equivalent of the transistor?



The transistor is a gm a voltage control current source the source is grounded right source is grounded. So, we do not have to bother too much on top I have Rd right. What is what should I do with the other side of the Rd? Other side of the Rd should be grounded because again Vdd right.

So, this grounds from here I go at the drain what do I have? I have a capacitor an infinite capacitor an infinite capacitor in a incremental sense is a is a short circuit right. So, the capacitor shorts then what we end up with we end up with let me use a different color for Rd because that is how I have sketched it in the figure on the top ok. So, what will be the value of this gm? It will be gm times Vgs right in this case hence it will be gm times Vg ok and from across which node am I interested in taking the output? Clearly I am interested in taking the output across RL right. So, this is my V0 this is V0 ok. So, if that is the case what is the incremental V0? So, note that in this case RL and Rd are in parallel to each other right.

Since RL and Rd in parallel to each other all the incremental current gm gm Vg is flowing out of the parallel combination of Rd and RL and I am taking by taking the voltage across RL I am essentially taking the voltage across RL and R parallel combination of RL and Rd for the purpose of this analysis right.



So, V0 becomes equal to minus gm times Vg Rd parallel RL ok and if you bias your input side properly this becomes minus gm times Vi times Rd parallel RL ok which means the incremental gain V0 over Vi becomes minus gm times Rd parallel ok. So, this is so this is clearly this is not as good as minus gm times RL which we could have gotten if we had plugged RL in instead of Rd if we had the option of having access to both terminals of RL and I could have plugged RL in between the drain and the and Vdd, but we could not do so and because and what was the replacement? The replacement the alternate architecture was to put Rd between Vdd and in between Vdd and the drain and RL is grounded right. So, and because now the current is getting shared incremental current is getting shared between note that this incremental current this incremental current is getting shared between RL and Rd right earlier all the incremental current was going into RL because the incremental current is getting shared between RL and Rd we are getting a lower gain ok. So, one final thing let me ask you before we stop again we assumed C2 to be we assume C2 to be infinitely large right.

What do you think I mean clearly you cannot again have an infinite capacitor right what do you think will be the value of C2 or what will be the constraint on the value of C2 right when if we have to choose a value so as to pass a waveform of frequency omega naught right. So, essentially what I am asking is we can you figure out what will be the constraint on what will be the what will be the limit of C2 or what will be the constraint on C2 just like we figured out the constraint on C2 at the beginning of this on this page right. So, I hope you can do it yourself I will see you in the next lecture. Thank you.