Course name- Analog VLSI Design (108104193)
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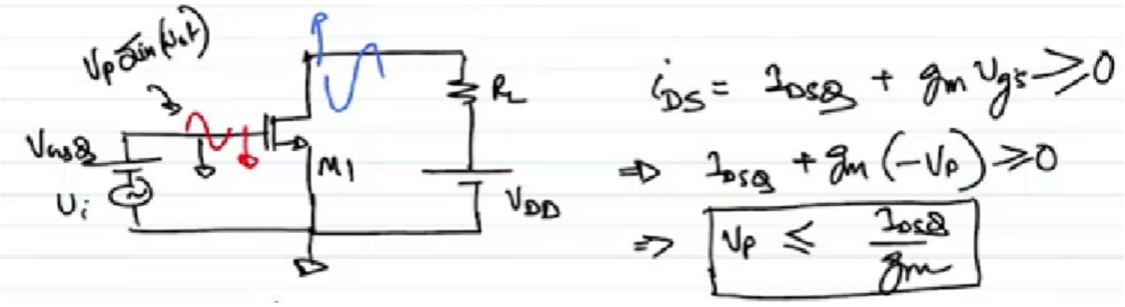
Week- 5
Lecture- 14, Module-1

Welcome back, this is lecture 14. So, in the previous lecture, we saw some constraints on the common source amplifier with respect to the amount of signal that you can hope to apply at its input while keeping the transistor in proper operating region that is it should be in saturation and obviously away from get cut off a cross the entire range of the signals right. So, while we were finishing of the lecture, we arrived at two constraints, one was obviously when the signal was going high right, one was if you recall. So, what we saw was if the signal swings in a sinusoidal, the signal incremental signal is sinusoidal, this signal will swing between the gate and the source on top of a quiescent VgsQ and while it does so, the drain voltage swings in a anti-symmetric manner right and if there is a gain the drain voltage will swing, the amplitude of the swing of the drain voltage will be higher than the amplitude of the swing at the gate right. Now, what happens when the input when the gate voltage increases and the drain voltage decreases, what happens? The transistor is going towards linear region right. So, you will have to be careful while choosing the input swing or in other words, if you are designing a transistor, you will have to choose the quiescent drain voltage in such a way that for the entire range of signal swing the transistor remains in saturation right.

This is as far as the condition of signal swinging high is concerned at the gate. Now, what is happening when the signal is going low? When the signal is going low at the gate at the drain it is going high right. So, saturation is no longer a problem, but what is the problem? The problem is the transistor, the current in the transistor is decreasing right and we said that while the current was going low the condition that we imposed was total Ids was the quiescent Ids that is IdsQ plus gm times Vi this is the total current and this we have to ensure that this never goes to 0. If this goes to 0 then we are in trouble.

Now, what is happening or rather in this case Vgs right, if you have to make it generic it should be Vgs as it turns out in case of a common source amplifier or in the configuration that we are looking at Vgs happens to be equal to Vi, but you have to be careful you do not you should not write gm times Vi all the time it is mind you it is always gm times Vgs. If Vgs is equal to Vi well and good, but it need not necessarily be the case all the time right ok. So, Ids is equal to IdsQ plus gm times Vgs and you have to ensure that this always remains greater than 0 and what happens at the negative cycle? At the negative cycle if this is a sinusoid on the positive cycle it goes to the input Vgs goes to plus Vp

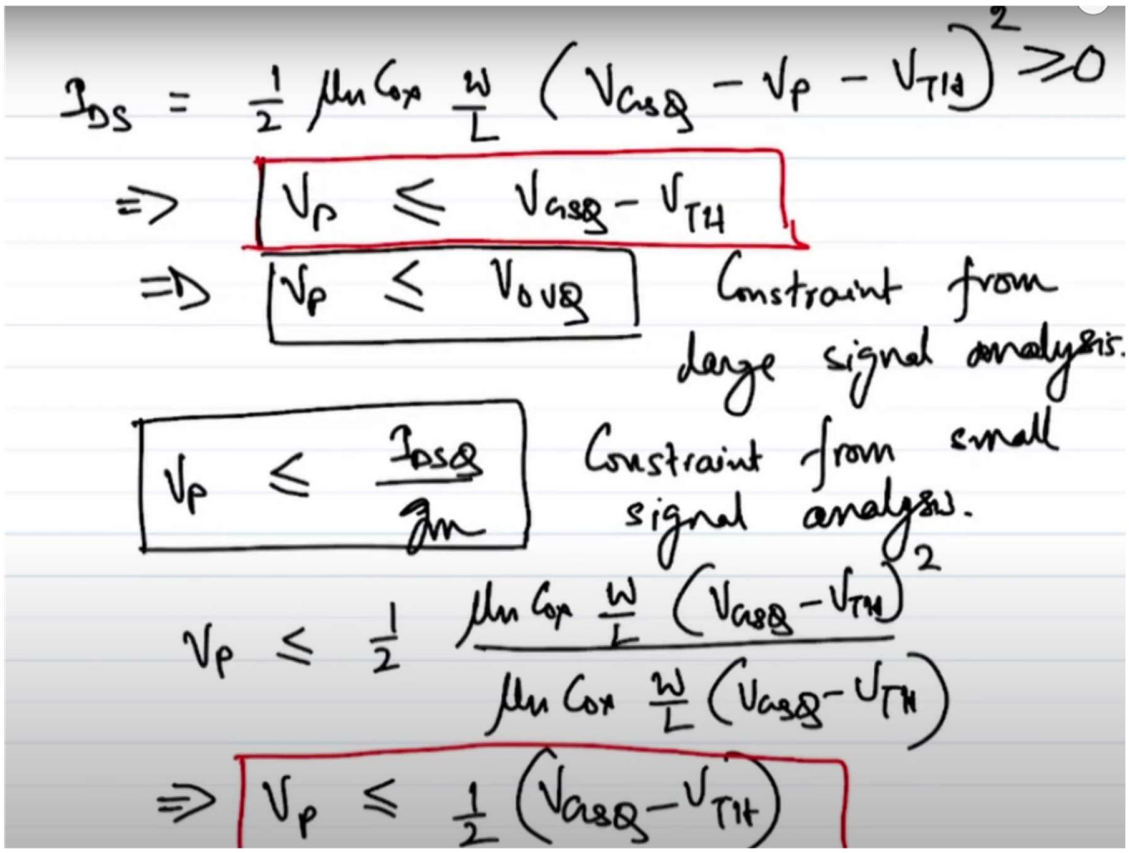
right with the sinusoid if this sinusoid is Vp sin omega naught t on the positive half cycle this goes to the input goes to plus Vp and the negative half cycle the input goes to minus Vp right. So, what is the constraint that will limit our condition that the transistor should is away from cut off the condition that will limit us will be IdsQ plus gm times minus Vp will be greater than 0 which means Vp should be less than IdsQ over gm right. So, this was the condition that we derived as we were finishing off the previous lecture.



Now some of you might have the question that this probably does not seem right because my current voltage equation for this transistor right the current voltage equation for this transistor is Ids is mu n Cox W/ 2 L Vgs minus threshold voltage whole squared right and on top of that if I apply a sinusoid right what does VgsQ lead to what does Vgs leads to. So, now I knew Vgs is VgsQ plus Vp sin omega naught t right and what will happen when I am in the negative half cycle or in other words when I am at peak negative cycle Vgs will be VgsQ minus Vp right. So, which means at sin omega naught t is equal to minus 1 what is going to happen Ids will be half mu n Cox W/L VgsQ minus Vp minus threshold voltage whole squared and in order to ensure that the transistor is away from cut off all we have to ensure is that this remains greater than 0 which means what which means we have to ensure that Vp is less than equal to VgsQ minus threshold voltage right or in other words we have to ensure that Vp is less than V overdrive quiescent right. So, this condition and these condition right this condition and this condition are they same. So, let us see so the condition that we got from so this is constraint from large signal analysis.

So, why do I say large signal because I have not taken any small signal approximation I took the total current voltage equation and I simply figured out when the current goes to 0 right. However, the condition that we got here is from quiescent plus small signal analysis right quiescent plus small signal incremental. So, in other words the condition that we got was Vp is less than IdsQ over gm this is constraint from small signal analysis. Now are they same let us see. So, if I replace if I replace this IdsQ and gm with their expanded version so what do I get so Vp should be less than half mu n Cox W/L VgsQ minus threshold voltage whole squared divided by gm, gm is again mu n Cox W over L

VgsQ minus threshold voltage right which means that Vp should be less than half VgsQ minus threshold voltage correct.



So, this full blown analysis the large signal analysis was giving me this constraint and the small signal analysis is giving me this constraint. Note that they are off by a factor of mu right. Now the question might that we might ask is that why are they different right there are two question to be asked like why are they different and are you comfortable with the fact that they are different and the second question is that if we are comfortable what is this factor of half what does what is the implication of this factor of half. Now coming back to the first question why are they different we should not be surprised here because what is small signal analysis in a small signal analysis we do not consider the entire current voltage equation right. We only consider the linear term while saying that the higher order terms even though they exist we will neglect them because it is difficult to deal with higher order terms.

So, we have purposefully, we purposefully omit some accuracy right we give away some accuracy in search of mathematical ease right. So, which essentially means that when you do a small signal analysis and you do a corresponding large signal analysis you are bound

to get a different result ok. So, that is as far as why are we getting a different result the answer to that question is concerned. However, now the question is what is this half what is this half doing here and should we be bothered about this or should we be ok with this limit that we got from the small signal analysis of Vp or should we stick to the one that we are getting from large signal analysis right. So, let us spend few minutes investigating that ok.

So, let us say let me just sketch one transistor without sketching the whole biasing network and everything. Let me say that this is V G S, V D S and the current through this is IDS. What is this IDS, VGS characteristics what does it look like? Note that this Ids, Vgs characteristics is nothing, but the plot of the equation half mu n C ox W/L Vgs minus threshold voltage whole square right. So, what does this look like? This looks like I mean if we assume that Ids is equal to 0 for a threshold voltage less than 0 voltage. So, till sorry Ids equal to 0 for voltages lesser than threshold So, till threshold voltage I do not have any current above threshold voltage I should see a I should see a parabola right ok.

Let me draw a clean parabola if I can ok. And let us say threshold voltage is equal to 1 volt right a nd let us say I am trying to figure out I have b ias my circuit in such a way that Vgs is equal to 2 volt right. So, let us mark off a value of 2 volt here. So, what is that IdsQ? The IdsQ will be that value which corresponds to Vds of 2 volt right. So, I will have some IdsQ which corresponds to Vgs of 2 volt ok.

So, what does now if I say that using small signal incremental analysis small signal plus quiescent incremental analysis I got Ids that is a total Ids which is equal to IdsQ plus gm times Vgs. What am I saying? What is gm? What is g m? What is the definition of g m? gm is nothing, but the slope of slope of I D VGS characteristics Ids Vgs characteristics at the operating point VgsQ. will be 2 volt right. So, if I sketch a slope right. So, this slope is yes is a gm right.

So, this is the slope right. So, this is the y axis correct. So, I can say that this is if you recall the equation of a straight line. So, this seems ideally similar to the equation of a straight line right. So, what is the equation of a straight line in x y plot? If I jog your memory y is equal to m x plus c is the equation of a straight line.

What is the corresponding to y here? Ids corresponds to y. what corresponds to x? in this case? Your Vgs right your Vgs corresponds to x. So, this is what is corresponds to m gm corresponds to m and what corresponds to c? Ids Q corresponds to c. So, this become Ids Q. Note that this is constant right ok.

However, there is a there is a slight difference. The slight difference is that here we are

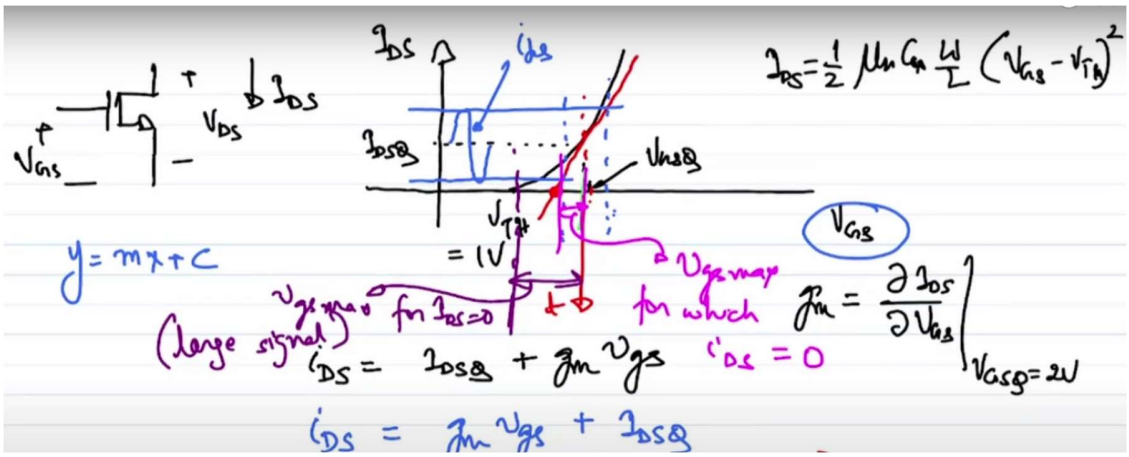
bothered with we are taking into account the total Vgs, but in this equation we are only taking into account the incremental Vgs which means that the plot would have shifted along the x axis, but that is a matter of detail right. So, that should not bother us too much here. Now, the question that we are asking the question that we are asking is that when we set Ids to be is equal to 0 right. When we are setting this Ids to be equal to 0 what are we essentially doing? We are essentially extrapolating this plot this Ids to be equal to 0 what are we essentially doing? We are essentially extrapolating this plot you are extrapolating this plot and seeing where it touches 0.

So, I had I think I did not sketch the plot properly. So, if I extrapolate this plot, so it will touch the it will touch the y axis x axis somewhere. So, the value of Vgs right the value of Vgs what is Vgs? I am sorry I mean I am making a mess out of this plot let me try to be a bit more clear ok. So, this is the equation of the straight line when we say that when we say that our signal swings in a sinusoidal fashion what are we essentially switch saying? We are saying that my Vgs is equal to Vpsin omega naught t and Vgs is swinging on top of what? Vgs is swinging on top of the quiescent point and what is the quiescent point? The quiescent point is VgsQ right. So, if I say that , if I say this is the time axis right.

So, this is Vgs. So, when I have, when the signal is sinusoidal what is happening essentially what is happening is the signal is swinging like this right and when the signal swings like this on the voltage domain what is happening in the current domain? the current is swinging between this point and this point right. So, the current is swinging between this point and this point right. So, this will be your this will be your IDS Q sorry this will be your delta IDS correct. So, this will be your small ids ok. So, when we say that the total IDS goes to 0 what are we essentially saying? We are saying that we are trying to figure out this point we are trying to figure out this point where the straight line needs the X axis or the voltage axis ok and what is this value of Vgs? In this plot what is this value of Vgs? The value of Vgs is nothing, but the deviation from let me use a different color the value of Vgs is nothing, but the deviation from the quiescent point right at which Vgs max this is not visible this is , this is Vgs max for which IDS goes to 0 ok.

So, this becomes this essentially becomes your this becomes the pictorial definition of where IDS goes to 0 using the small signal plus quiescent quiescent plus small signal picture. However, if you stick to the if you stick to the large signal picture large signal picture what is, it that you will get? You will get that you will get this to be your Vgs, right. So, using large signal picture this is the Vgs max for IDS equal to 0 using large signal picture correct. Now, clearly in the pictorial definition you see that there is a difference between the small signal and the large signal picture simply because I have a

parabola it is basically the current, the current voltage relationship of a MOSFET is that of a parabola and the fact that that half the factor of half comes into picture is basically the property of the slope of the parabola right. Now, note that if I if you if you again go back to the previous lecture what we established the stuff that we established was in order to ensure our small signal models are valid we have to ensure a certain condition right.



What was the condition? The condition was the condition was that the incremental Vgs has to be much much less than the overdrive right. The incremental Vgs should be much much less than VgsQ minus threshold voltage. Now, if you allow the signal to swing as high as the overdrive voltage right. So, if you allow the signal to swing as high as overdrive voltage you are definitely not honoring the constraint on small signal and if you do not honor the constraint of small signal what is going to happen? Your circuit will become terribly non-linear right. You will have higher order terms you will have if you input a sign input if your input is V P sine omega T you will you are going to get output at omega naught and also but you are also suppose you also be getting outputs at 2 omega naught because you have the squared terms that will come into picture and why will they start dominating? They will start dominating because your signal is swinging so much that your small signal validity approximation is no longer no longer valid right.

So, given that constraint that we have to stay away from the signal swing of as high as the threshold volt as I have the overdrive voltage right. So, we cannot ever apply a signal which is equivalent to we cannot ever apply a signal between the gate and the source of a transistor which is equivalent to its overdrive voltage right which means we have to apply a lower signal and a lower value of the signal and the constraint on and analysis of incremental plus plus small signal is enabling us right. The result that we are getting by using incremental plus that the result that we are getting by enabling the quiescent plus

small signal approximations is giving us the is giving us the a better perspective of how to handle how to handle small signal models and the results that we are getting out of a small signal by setting this total current to 0 also honors the small signal approximation right. So, going forward hence going forward we will be using this constraint right we will be using this constraint of for setting the current to find out the maximum current or the maximum swing that we can have right at the input in order to keep the transistor away from cut off we will be using this constraint that is the quiescent plus incremental and we will not be using will not be using the large signal constraint of setting the IDS to be equal to 0 right. So, this is again a very important a very important outcome of this of this discussion.

So, we will be having a few assignments on small signal model on swing limits what is the maximum swing that you can apply from an input while keeping while keeping the transistor in saturation and away from cut off. So, I hope you will be you will be able to hone your skills and become comfortable with dealing with is this quiescent plus small signal models right. .