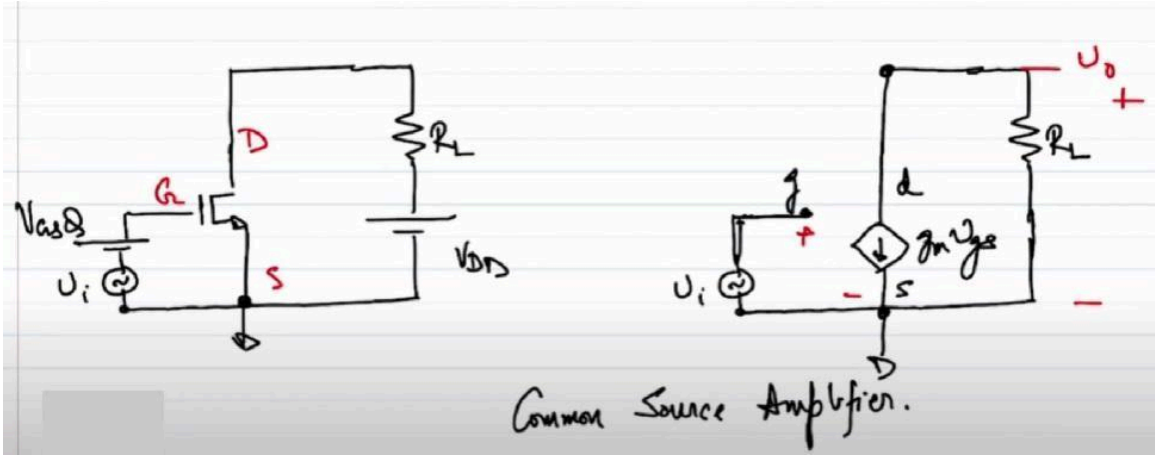
Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 5
Lecture- 13, Module-2

Now, welcome back. So, let us take, let us use the framework that we just talked about and see how we can use it in our common source amplifier. Mind you this is again a repetition of what we have done in the previous lecture, but in this lecture the aim is to formalize the treatment of using the quiescent condition and the incremental condition separately and combining them, right. So, because this is important because we will be using this framework for the rest of the course, ok. So, this is the standard common source amplifier topology that we started off with even before we knew that this was a common source amplifier. So, what should we do? First step is to find out the Q points.

So, this is let me mark this as Q point analysis. So, what should we do? We should get rid of the incremental or any incremental stuff. So, this is what we will do, right. From there, from here what we will find? We will find Vgs, we will find Vds, we will find Ids, right.



$$v_{DS} = V_{DSQ} + v_{ds} = V_{DSQ} - g_m R_L U_i$$

$$v_{GS} = V_{GS} + v_{gs} = V_{GSQ} + U_i$$

$$v_D \geq v_G - V_{TH}$$

$$\Rightarrow V_{DSQ} - g_m R_L U_i \geq V_{GSQ} + U_i - V_{TH}$$

$$\Rightarrow (1 + g_m R_L) U_i \leq V_{GSQ} - V_{TH} - V_{DSQ}$$

So, then what is the second step? The second step is to do small signal analysis or incremental analysis. So, what will you do? You will essentially replace all the non-linear elements with the incremental equivalent, right. So, the incremental equivalent of our, for MOSFET is the incremental equivalent of the two-port network, right. So, and we know that given the current voltage equations of the MOSFET in saturation, we will know that the incremental equivalent is this. We get rid of all the constant sources and how should we get rid of the constant sources? Since we have a Vdd, since we have voltage source, we can short it.

If we had a current source, we would have had to open it, right. So, this is Rs. So, this is gm times is voltage Vg minus Vs or Vgs, ok. So, if we do this analysis, what do we get? We get this voltage to be equal to Vi, correct. So, if which means Vgs is equal to Vi which means this current becomes gm times Vgs.

This current is the same as this current which means this voltage here is what? What is the drop across RL? The drop across RL is gm times Vgs, but in which direction? In this direction. Since the bottom side is bottom, bottom side of RL is grounded, so this voltage will be minus gm times Vgs times RL, correct or in other words which is equal o minus gm times Vi times RL, right. So, what is the total? What is the Vgs? So, when we have to find out total, so we have to add up. Now, in order to find out total, so we have to find, let me not go into a different page that will make it complicated. So, let us say total I and V.

So, what you have to do? You have to find out, you have to get the Vgs, Ids, Vds, you have to find out Vgs, Ids, Vds and you total them, right. So, you have to find out, you total them as in Vgs becomes Vgs plus small vgs, Ids becomes Vgs plus small ids. Similarly, Vds becomes Vds plus small vds. Let me ensure that we have used the same terminologies, yes, right. So, two step, three step process.

First step, you find out only quiescent. Second step, you linearize the network, find out its incremental equivalent and solve it to find out incremental. Third step, add them together to get the total correlation voltages. And why is total essential? Total is essential because you need to ensure that the circuit, the transistor still operates in saturation even when there is a signal swing. It is not sufficient to only ensure that the transistor remains in saturation only under quiescent condition.

The transistor needs to be under appropriate quiescent regime even in the presence signal swing. And how will you ensure that? In order to ensure that we have to find out the total currents and voltages, correct, ok, great. So, now, let us take the example of this common

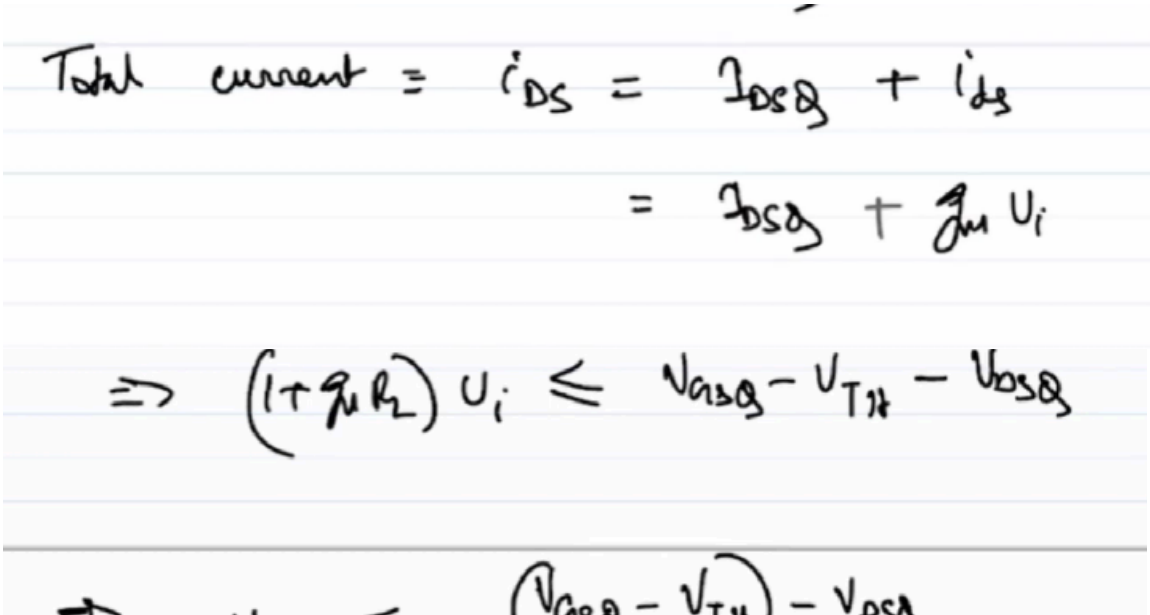
source amplifier and see where that leads us. So, what did we see? We saw that, now let me just, I will assume that we know what the common source amplifier currents and voltages are.

Right. So, what should we see? We should find out what is the maximum swing if I have to find out, right and I mean to find out the maximum or minimum Vi for which M1 always remains sufficiently into, remains in saturation. What should we do? Firstly, we need to establish what are the total currents and voltages. So, what is the total? The total, so total current total, I mean let us do the saturation first, saturation condition first. So, Vd which is equal to Vds, right, Vds which had been found from quiescent conditions plus Vds. What is Vds? Vds is, small vds is again, small vds is minus gm times Vi times RL, right.

So, this is a small vds or incremental vds. So, this becomes Vds minus gm times RL times Vi, okay. So, this is Vds, right, okay. Similarly, what is small v, small v or total Vgs? Total Vgs is VGS plus Vgs which is equal to Vgsq, the one that we have applied plus Vi, right, okay. Let me use q here, otherwise it will not be consistent, okay.

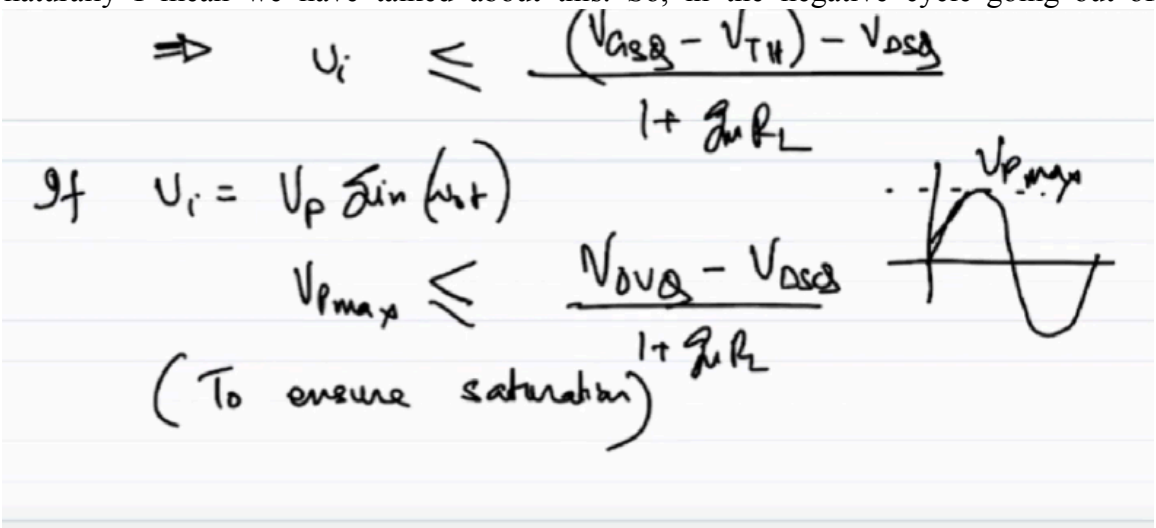
So, now what is the condition for saturation? The condition for saturation is Vd should be greater than equal to Vg minus threshold voltage, right. So, since this is the case, I need not even bother about source, but in our, in this example the source is grounded, so

it does not really matter whether I am expressing in terms of Vds, Vgs or only Vd or Vg which essentially, this essentially gives us the condition that V dsq minus gm times RL times Vi should be greater than Vgsq plus Vi minus the threshold voltage, right which means 1 plus gm RL times Vi should be less than equal to Vgsq minus threshold voltage which is a DC overdrive, right minus Vdsq which essentially boils down to Vi should be less than Vgsq minus threshold voltage minus Vdsq by 1 plus, right and if Vi is Vp sine omega0 t, right, if Vi is less than sine, Vp sine omega naught t, what does this, what does that condition impose? The condition essentially is telling us that in order to always



ensure the transistor is always in saturation even when I have applied a sinusoidal input your Vp max should be less than this is V overdrive minus Vdsq by 1 plus gm RL. Let me say V overdrive quiescent q because we are dealing with quiescent conditions there, ok. So, this is to ensure saturation. So, this is when the signal when Vi is here, right.

So, this is the max we are talking about. We are not talking about the bottom cycle, right. We are not talking of the negative cycle, we are only talking about the positive cycle because the transistor can go out of saturation only the positive cycle of in case of a common source amplifier, ok. So, now naturally what happens if in the negative cycle naturally I mean we have talked about this. So, in the negative cycle going out of



saturation is not no longer a problem because the gate voltage is going down, drain voltage is going up.

So, the transistor is comfortable in saturation, but what is the problem? The problem is my current is decreasing, right. So, what is the problem? So, what is the other condition? The other condition is what is my total current? Total current is equal to Ids is Idsq plus small Ids. So, Idsq we have found out from our quiescent conditions, right. So, mu n Cox w/2 L Vgs minus Vd whole square, right. So, we have found out Idsq.

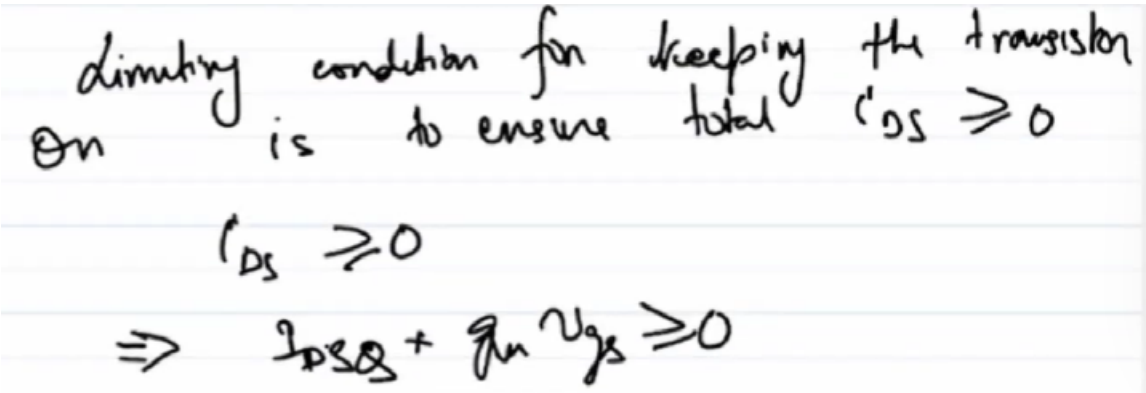
What about small Ids? What about incremental Ids? What is the incremental Ids? Incremental Ids is gm times Vgs, right. So, incremental Ids is gm times Vgs and Vgs is equal to Vi in this case. So, this becomes plus gm times Vi, right. So, what do you want this to be? What is the inequality that we are bothered about in this case? So, let me sketch inequality that we are bothered about in this case.

Let us say this is Idsq. This is with respect to time, ok. So, let me sketch it in the next page, ok. And let us say this is Vi, this is Vi, ok. So, what is going to happen? So, let us say this is Idsq. If this is and that and the Vi is also sinusoidal, what is the sinusoidal

voltage lead to? So, it will lead to also a proportional current which is gm times Vi, right.

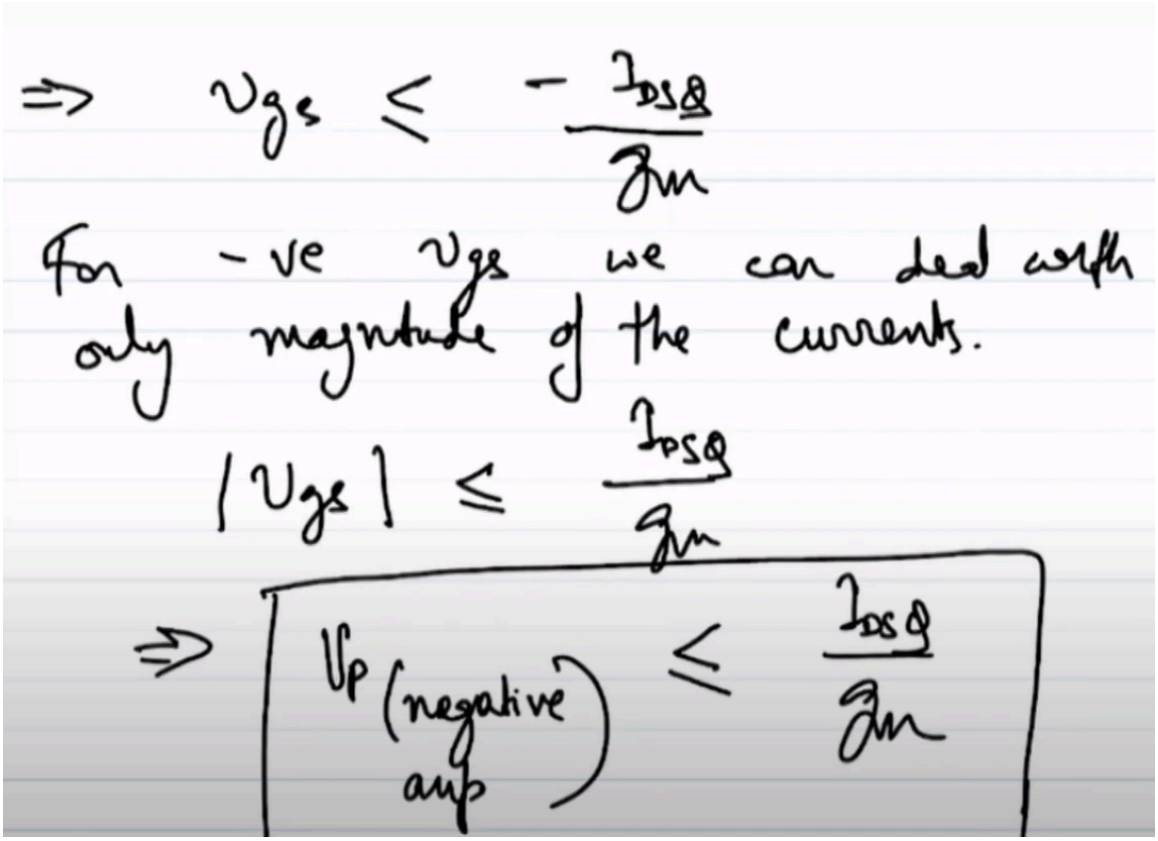
So, and you have to essentially add those two up and you will get, you will get a corresponding sinusoidal current on top of quiescent, right. So, this will be gm times Vgs or gm times Vi in this case. Similarly, this will be gm times Vgs, the magnitude of that will be gm times Vgs or gm times Vi. Now, what do you think? Do you see a problematic situation arising, right? You must be, I mean just look at this margin that I have when the current is going towards the negative cycle. What is that margin that you are have? The margin that you started off with was Idsq, but the margin is shrinking as the current islowering, right.

As the, in the negative half cycle of Vi that margin is shrinking. And how much can that margin shrink? The margin can shrink to the level of Idsq, right. So, the max which essentially means that if you keep on increasing Vgs, you run into the trouble of shorting the transistor down, right. So, what is the problem? The problem is if you increase, if Vgs increases, total Ids decreases, right. If Vgs increases, total Ids decreases and how much total Ids can decrease? It can at max go to 0, right or rather at min it can go to 0, which means what is the other condition? What is the limiting condition on the negative side for Vi? So, the other condition is Ids.



So, limiting condition then becomes, limiting condition for Ids greater than equal to 0 becomes Idsq, sorry, let me just say the limiting condition for keeping the transistor on is to ensure total Ids is greater than equal to 0, right. So, in this case, so Ids if I say this has to be greater than equal to 0, what does this mean? This means Idsq plus gm times Vgs should be greater than equal to 0, right, which means what? Vgs should be less than equal to minus Idsq over gm, right. So, and in our case Vgs is essentially Vi, correct. So, this is Vi should be less than equal to minus Idsq by gm, correct, ok, but note that here, you have to be careful with the sign, signage because of what? Because what is it, what is it that is, that is changing when Vgs is decreasing, right. So, when Vgs is decreasing, right,

the current is also decreasing.



So, essentially we are talking about negative quantities or in other words, if I have to get rid of that, of those negative signage, we can only deal with the magnitude, right. So, if we have to deal with the magnitude, I can simply say that, in other words for negative Vgs, we have to ensure that we can deal with only magnitude of the currents and say that mod of Vgs should be less than Idsq over gm or in other words, we can say that while going negative in this case, Vp negative amplitude, right, negative magnitude should be less than Idsq over gm, right. So, what is this essentially telling us? This is essentially telling us that if this height, let me sketch it in a different page. So, this is the input voltage Vi, this is the total current.

So, this is Idsq. The current, total current becomes, the total current becomes actually 0, it touches 0, total current touches 0 when this input sinusoid or let me just say Vgs in this case, this Vgs becomes Idsq over gm, right. So, note that this everything came from quiescent plus incremental analysis. So, we found out what is the quiescent drain current and we found out what will be the change in the drain current in the presence of a swinging Vgs and we notice that if Vgs goes down, the total drain current will also go down and how far it can go down? It can go down to at max 0. So, this is becomes a limiting condition of the transistor current going to 0 under the, when we have done the

analysis using the framework that we have developed, right. S o, now essentially you would have seen that we have gotten two constraints.

So, so we get, so to summarize, so we get two constraints on Vgs or Vi in this case for the, to keep M1 in saturation and away from the top, correct. Those two constraints came from two different conditions. One is to keep the transistor away from saturation and other is to keep the transistor away from cut-off. So, after you do this, so what are these constraints? The constraint was Vgs or in this the constraint that we got was Vi should be less than V overdrive Q minus threshold voltage by 1 plus gmRL and another constraint was Vi could be less than equal to IdsQ over Vm, right. So, this is the saturation constraint, this is the cut-off constraint, right.

And these two and the values that you will get by analyzing these two constraints will not be same, did not necessarily be the same. So, which value will you choose? Let us say after doing the saturation constraint I got 100 millivolt, right. I got the constraint of Vi should be less than 100 millivolt and after doing the cut-off constraint I got Vi should be less than 50 millivolt. Which one should you choose? Obviously, you should choose that one for which both the constraints are met which means we will choose Vi to be less than equal to 50 millivolt. Because if you choose Vi to be less than 50 millivolt you not only satisfy the cut-off constraint but also satisfy the saturation region constraint, right.

Okay, so we will stop here for this lecture and I request you to pay particular attention to this lecture because this will form the backbone of many of the analysis that we will be doing for almost all the architectures that will be that will follow, right.