Course name- Analog VLSI Design (108104193)
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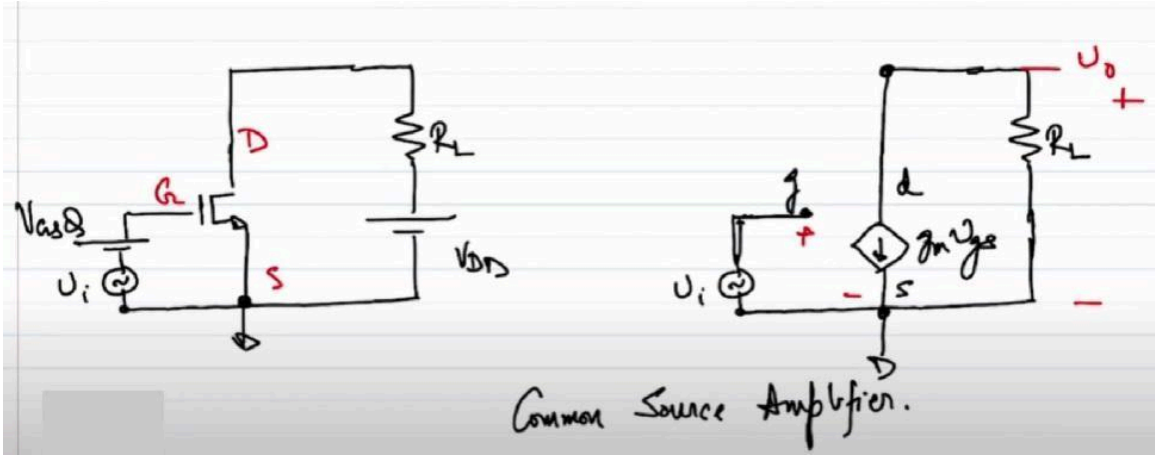
Week- 5
Lecture- 13, Module-1

Now, welcome back, this is lecture 13. So, in the previous lecture we were looking into what happens to a to the condition of a common source amplifier right, when the signal at its input swings right. So, by the way let me take a moment to emphasize the fact that, so what is the configuration of the amplifier, potential amplifier that we were interested in. So, this is the gate, this is the drain and this is the source. So, the input is incrementally, what is the incremental equivalent of this, incremental equivalent of this structure is. So, you have the gate right.

So, what I will do is, I will sketch the MOSFET, I will sketch this entire structure and then show you the incremental equivalent. So, what should you do in order to get the incremental equivalent. So, you should first replace the non-linear device with its linearized equivalent and what is the linearized equivalent of this MOSFET M1. So, the linearized equivalent of this MOSFET is nothing but.

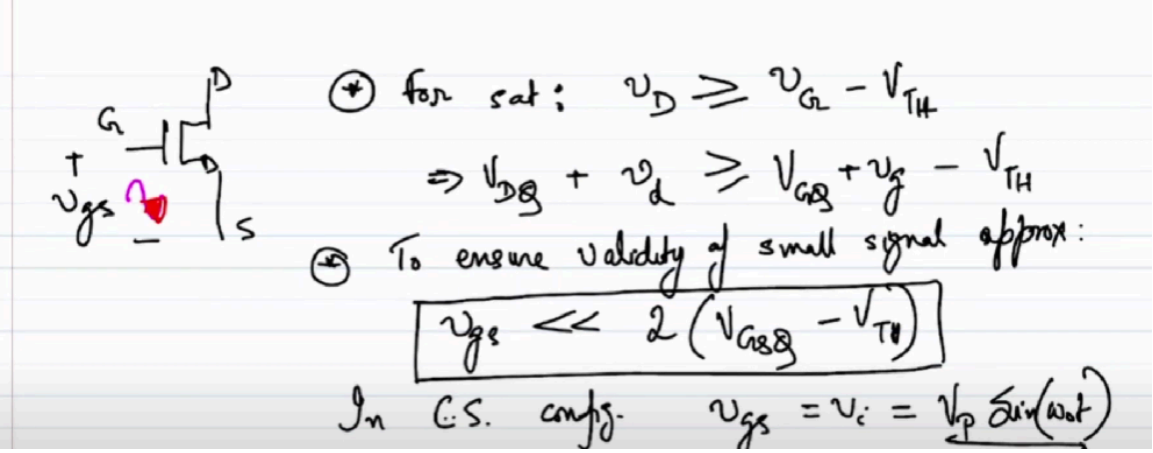


A control source, a current control source whose controlling terminal are the gate and the source correct. The constant voltage sources go to 0, so this shorts. We leave the incremental voltage source as is on the output side the constant voltage source goes to 0 right. And what is the other terminal, this is the drain terminal and this connects to RL. What is the value of this control source? The value of this control source is gm times Vgs right ok.

So, what so, incrementally if you see the input is applied between the gate and the source right and the output where are you taking the output, the output is taken between another terminal which is drain in this case and the source right. So, the common terminal between the input and the output is a source terminal and since the common terminal in the incremental model is a source terminal, it is called a common source configuration right. So, this is also called common source amplifier right. So, another way of thinking another way to think of it is the fact that whenever we say whenever we say common right, you will see several configurations which that we will be dealing with in the upcoming lectures. This common term will come you will see common source, common gate, common drain and so on.

So, this common essentially in your mind at the back of your mind you can you can replace common as grounded source right. You can say that this is almost equivalent to saying you have a grounded source configuration ok. I find this terminology a bit more useful because it, yeah it is much more general while dealing with other configurations as well right. So, however, in the literature common source amplifier is the it is a generic term. So, we will refer to this configuration as common source amplifier, but at the back of your mind you should have the understanding that whenever we are saying common source amplifier, we essentially pointing to the fact that the source is incrementally grounded ok.

Great and also it is not only the source is incrementally grounded the it should be common with the input should have been applied between the wherever we between the gate and the and the, and the incrementally grounded source and the drain the output is also between some other terminal and the grounded source ok fine. So, now so now in the previous lecture we were delving into what happens when the signal actually swings right. So, it is one it is one matter to just apply the voltages the quiescent voltages and set up the quiescent currents in order to keep the transistor in saturation, but it is a different volume altogether when we say the transistor should be in saturation even when I apply an incremental even when I apply an incremental input right. And when we saw that and we saw that in case of this particular configuration or if we saw that if incrementally my input if Vi is or even if I say that incrementally if this is the Vgs and assuming the transistor is in saturation right. So, subtext is transistor is in saturation we saw that there were two conditions that we needed to maintain right what were the two conditions.



So, this is gate this is drain this is source the primary condition that we had to maintain was for saturation the total drain voltage Vd had to be greater than equal to the total gate voltage Vg minus the threshold voltage right ok. In other words if I have to break it down what is total drain voltage? Total drain voltage is nothing, but the quiescent drain voltage Vdq or capital V capital D right plus the incremental drain voltage should be greater than the total gate voltage right minus the threshold voltage. So, this was the saturation region and this was this condition we had to ensure in order to keep in order to make sure that the transistor always remains in saturation. What was the second condition? The second condition was to ensure the transistor is sufficiently on right. So, when we say the transistor is sufficiently on what are we implying? We are implying that we know that the Vgs when the Vgs swings it can go up or it can go down.

When Vgs goes up right when Vgs goes up I run into a potential problem of the transistor going out of saturation because the drain voltage can because I am closing the gap between the gate and the and the drain right. However, when the when the Vgs goes down when the Vgs goes in this half cycle when the Vgs goes down what is what is the likely cause of problem? The likely potential problematic cause is the transistor can get into cut off right and we did the analysis and we saw that we had to ensure that the incremental Vgs right had to be much, much less than had to be much much less than what the over twice the overdrive of the transistor right twice the quiescent overdrive of the transistor. Correct? And if we in a common source configuration in a common source configuration if I go to this common source configuration what is this incremental Vgs? Incremental Vgs is so in in common source configuration this incremental Vgs is the input that has been applied directly and if I say that the input is sinusoid right if the input is sinusoid then Vgs essentially becomes Vp sin omega naught t right. So, what is the condition on Vp? What is the condition on Vp? To ensure that the transistor or the small signal approximation always holds so I let me let me take a step back and I think I

should rephrase I should rephrase this this this statement. So, if we go back to the previous lecture we saw that this condition was required in order to ensure in order to ensure the validity of the small signal approximation regardless of whether whether the signal is swinging on top or you swinging to the positive cycle or in the negative cycle right.

So, so let me let me correct myself here. So, the condition that I am referring to here is to ensure to ensure validity of small signal approximation we have to ensure this Vgs is much less than the twice the overdrive right. We will come to we will come to what is the what is the necessary condition what is the minimum Vgs that we can apply shortly, but again I mean this is a correction right from the statement that I had made two minutes back that this condition is to ensure the validity of the small signal approximation. So, in a common source amplifier Vgs essentially is equal to Vi which is equal to Vp sine omega naught t right. Since this is since this is that case so what is the maximum Vp that you can apply in order to ensure in order to ensure the small signal validity right.

The small signal approximation is still valid note that when you have the sinusoid Vp sine omega t the sinusoid goes on either direction and this peak to peak is twice Vp right which means which means Vgs max is twice Vp which means you have to ensure Vp is less than 1 overdrive. So, in a common source configuration right a common source configuration you have to ensure that the sinusoid that you have applied is much less than the overdrive of the other transistor and if you are not particularly bothered about whether it is a common source configuration or not right then the question arises how should I let us say I have a network which has a transistor where whole bunch of stuffs are connected to the source, whole bunch of stuffs are connected to the gate and whole bunch of stuffs are connected to the drain right. Then how do I know, how do I know what is the constraint what is the constraint for small signal approximation that is a quite a valid question to have because it is not necessary that we will be using our transistor in a small signal configuration all the time right. So, in that case what you have to do is you have to find out what is the gate voltage you have to find out what is the source voltage right and then you will have to ensure Vgs whatever that Vgs might be after solving KVL and KCL is much less than twice overdrive and if Vgs is supposed to be a sinusoid right if incremental Vgs is equal to some sinusoid let us say some a sin omega naught t, ags sin omega naught t right. We will have to ensure to ensure that ags is much less than overdrive right this is for validity of small signal approximation.

Now, one might say that what is this much much less whether I mean 10 times less is much much less 100 times less is much less that depends on the application right. So, the whatever you will be designing a circuit for certain application right that application will have a specification what is this much, much less and for you will have to you will have

to design your circuit based on the requirement of that particular application ok. Ok, so let us move on, let us move on. So, in or now if I ask you if I give you if I give you a, let us say a common source amplifier like the way we derived the way we went about finding out the total currents and voltages in the common source amplifier in the previous lecture was to combine the incremental and the combine the incremental and the quiescent conditions in the same figure right and we I walked you through the steps, but that can be a bit of a hassle when the circuit becomes a bit more involved when you have multiple transistors when you have multiple elements right it might not be so easy to draw or to sketch all the incremental and the total currents in the same figure right. So, what we generally do is we break the problem into two parts and then combine them in order to come up with a solution.

Let me let me demonstrate that with the same example that we have been taken till now. So, let us take what I am asking, what I am basically trying to motivate here is that in the next part of this lecture what we will do is we will see how to we will see how can we combine the incremental and quiescent conditions to get to total currents and voltages in the network right. So, this is what we will be focusing on in the next next few minutes ok. So, so let us take the same example.

Ok. So, what is step 1? Step 1 will be, step 1 will be find quiescent currents and voltages right. So, how will you find quiescent currents and voltages? You get rid of inputs get rid of incremental inputs in this case the incremental input was only one voltage source we get rid of them when I say get rid of them I mean I desensitize them right. Voltage source desensitizing means it gets shorted if I had a current source I would have had to open circuit them right ok. So, now from this what will I do? I will solve the full blown non-linear equation right. So, how do you do that? Solve for I and V using KCL and KVL using the non-linear IV current equations of M1 right.

So, what you will be getting from this you will be getting VgsQ you will be getting with all the parameters right you will be getting Vgs Q you will be getting Vds Q you will be getting Ids Q right. So, we will combine them what is the next step? The next step next step is make the incremental model of the non-linear network. What is the incremental model of the common source amplifier? We know that we have done it sufficient number of times now the incremental model of the common source amplifier is this where there is no we do not have any constant voltage or current sources we only have incremental quantities and the MOSFET has been replaced with its incremental equivalent V I this gate this source, this is drain this is gm, Vgs right. So, what will you do now? Now note that this is the completely linear network right. So, what will you do? We will find so here we will be solving.

Solve for I and V in the incremental network linear network and what will be step 3? Step 3 will be combine the currents and the voltages that you have gotten from step 1 and step 2. To get total current and voltage combine the currents and voltages with me also mark the figures that would be helpful. This is figure 1, this is figure 2, combine the currents and the voltages obtained from the quiescent analysis. So, this is figure 2 figure 1 and incremental analysis this figure 2 right. So, what will you get after at the end of this? So, from figure 1 we will get VgsQ, IdsQ, VdsQ right and from figure 2 we get small vgs small Ids small vds.

So, what will be the total? Small v capital G S will be V G S Q plus small v g s similarly I D S will be I D S Q plus small I D S similarly V D S will be V D S Q plus small v g s ok. So, once we have this framework we can use this for any network right. We can essentially close our eyes find out I mean find out the quiescent conditions convert the quiescent transistor circuit into its incremental equivalent find out the incremental conditions and combine those two. Now, note that the incremental equivalent is related to the quiescent equivalent quiescent network because in order to figure out the incremental equivalent you need the values of gm right and what does gm depend on? gm depend on depends on the quiescent condition of the primary network right. So, the value of the gm will change if you change if you change the quiescent condition, but the analysis procedure or the steps that we that we go through does not really change ok.