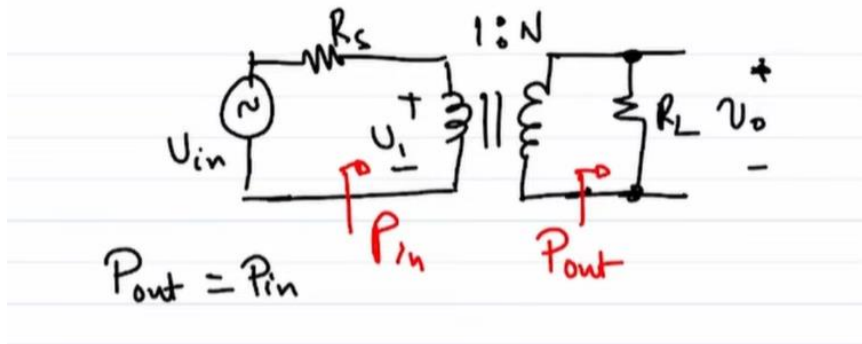


Course name- Analog VLSI Design (108104193)
Professor – Dr. Imon Mondal
Department – Electrical Engineering
Institute – Indian Institute of Technology Kanpur
Week- 1
Lecture- 1, module-02

Welcome to Analog VLSI design. ok, I hope you had the chance to go through the problem to figure out whether P_{out} will be greater than P_{in} less than P_{in} or equal to P_{in} and what did you find? I am sure that you have seen this before. So, what did you find? You found that P_{out} was exactly is equal to P_{in} right? What was P_{out} ? P_{out} was a power delivered to R_L and what was P_{in} ? The P_{in} was the power that was going inside the transformer right and should it make sense? It should make sense right? Why should it make sense? Because this transformer is a lossless device at least an ideal transformer is a lossless device.



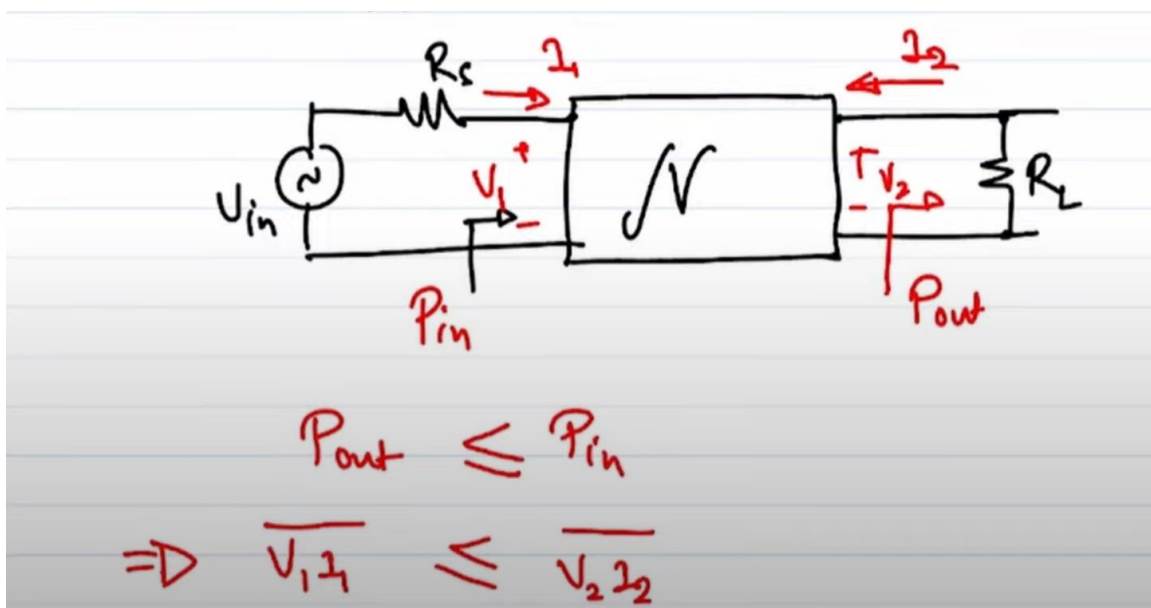
So, whatever power goes in inside the transformer none of it can get dissipated in the transformer and the transformer cannot generate any power on its own which means the power that is going into the transformer only has one place to go and that is into the load resistance which gets dissipated, but which consumes the entire power that went inside the transformer.

Hence, P_{out} was equal to P_{in} right. So, in a sense, in a sense, this is one of the fundamental laws of our universe which essentially guides energy conservation right? which essentially means that if we have a network N right which has a net which has a passive network N without any sources any voltage sources or current sources inside if you have a passive network N then the power that goes in it is P_{in} and if you observe the power that comes out that is P_{out} . So, P_{out} will always be less than equal to P_{in} right. In other words, if this is input voltage is V_1 output voltage is V_2 the current that goes in is I_1 that currents, that comes out let me put the direction the other way because that is generally the convention.

So, what this is essentially saying is average of $V_1 I_1$ will always be less than average of $V_2 I_2$ ok? So, this is basically power conservation said in a different way ok. So, this should not be surprising if N if the network N is lossless which was the case in our ideal

transformer case then P_{out} will be equal to P_{in} , ok great. So, what have we what have we seen till now? We have seen that it is not sufficient to just say that we will have a voltage amplifier. Also similarly it is not sufficient to say that we will have a current amplifier even though I did not prove or even I did not show an example of current amplifier you can you can flip the transformer on its head and make that case as well.

However, it you can say that we want to build an amplifier in this course where the output power is more than the power that I am extracting from the source. However, note that it is not sufficient yet it is not it does not really guarantee that the output voltage is more than the input voltage or the output voltage is less than the input voltage. Thus note that we are talking about power, the power is the product of voltage times current. It is quite possible that the voltage does not change and the current increases and hence the power at the output is higher than the power that you are extracting from the source. It's, it's quite possible that the current at the output is smaller than the current at the input, how the voltage is higher right.



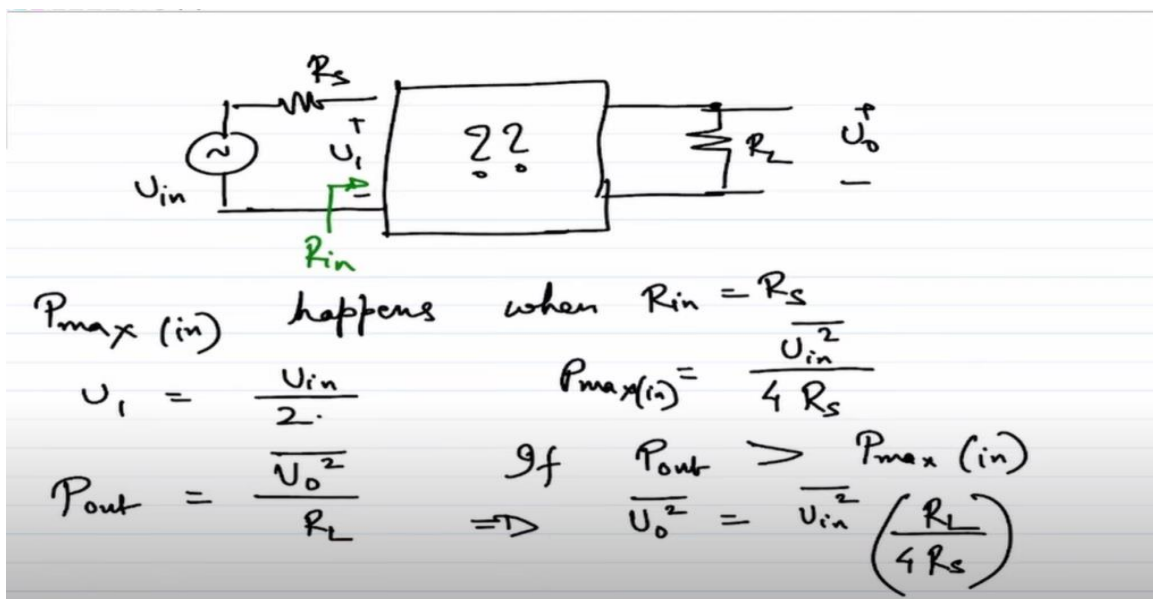
So, all these sorts of combinations are possible. All you need to ensure is that if you can ensure that your output power is greater than the input power then you might have a configuration in which you might have that configuration behave like a voltage or a current amplifier depending on the values of loads and source resistances. Let me elaborate. Let us say I have a voltage source V_{in} in which again has a internal resistance R_s and like before we have put in a block between the input and the output right and we are trying to figure out what this block should be right and we said that we are looking for a device which can get us power amplification or we are looking for a network which can give us amplification of power. So, it makes sense to first figure out what is the maximum power that I can

extract from the source right?

So, what do you think if I only concentrate on this piece right if I only concentrate on this piece and then further say that the stuff inside the box stuff inside the box gives me some resistance R_{in} right? Let us say it gives it gives me some resistance R_{in} what is the maximum power that I can extract from V_{in} right. What is the maximum power that I can extract from V_{in} ? So, P_{max} from the input side will be V_{in} square average right. Oh let me, let me, let me take a step back and point out the point and recall the fact that recall the fact that the maximum power transfer happens when R_{in} is equal to R_s right. So, $P_{max}(in)$ happens when R_{in} is equal to R_s right.

If that is the case what is P_{max} ? So, if that is the case my V_1 will be equal to V_{in} by 2 right? So, what will be P_{max} ? P_{max} will be V_{in} square over 4 right and what is V_{not} or rather what is P_{out} ? P_{out} in this case is V_{not} square average over for R_L right? If the voltage sources in question are sinusoidal then you can replace V_{in} square with the amplitude square by fact by 2. Similarly, you know that V_{out} will be also some sinusoid. So, you can replace it with the amplitude square by 2 right instead of V_{not} square average.

So, if a power amplification has to happen right? if P_{out} is greater than P_{max} that has been extracted from the input then what do I get? We get V_{out} square is equal to V_{in} square times R_L over 4 R_s ok. Which essentially means that if you have power amplification and you also want to ensure voltage amplification then you have to ensure that R_L is greater than 4 R_s right? If you can do that right, if you can do that then obviously, you will be able to ensure that there is a power amplification. Note that it is a function of the resistances associated in the network right because power is a function of the resistances associated with the network.



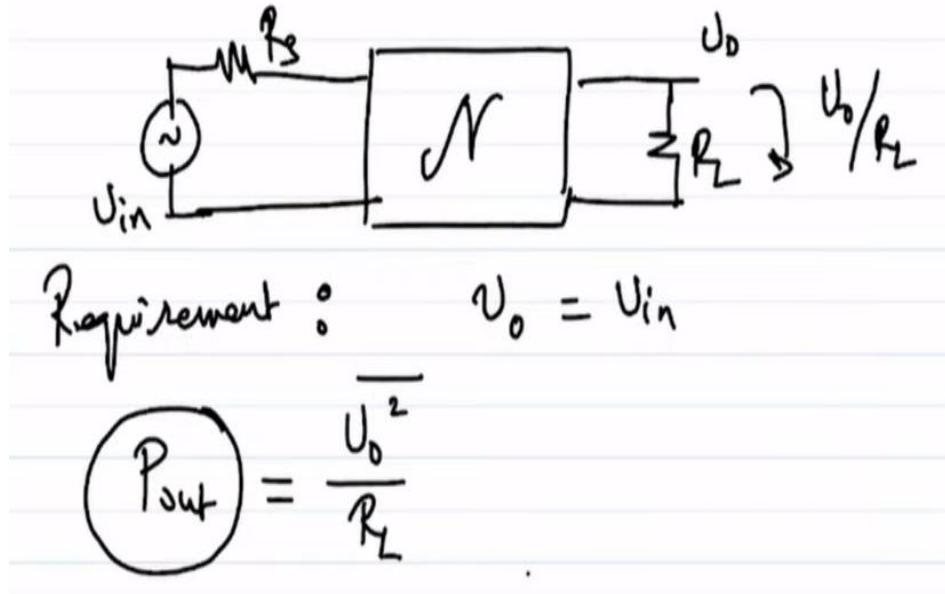
If I look deeper into this situation and ask you the following question that let's say I have requirement where I have a requirement where my output voltage V_{out} across a resistance R_L right.

So, my requirement is the requirement is the following. Let's say we requirement is V_{out} has to be equal to V_{in} . Can you comment on whether you comment on whether this block needs to be capable of doing performing power amplification or any voltage amplifier or even a short circuit between the input and the output will suffice? Note that I am sure you already have figured this out, but note that if V_{out} has to be equal to V_{in} you need to ask one more question. Now, what is the question? The question is, hey!! if V_{out} has to be equal to V_{in} can you tell me across what load should I be maintaining V_{out} and why is that question important? That question is important because if you have a some load R_L , what is the current that you are drawing through R_L ? You are drawing V_{out} over R_L right and if this is the case which means you need to be able to supply a power of V_{out}^2 over R_L to the output right?

So, this will be P_{out} . If you have not asked what is the value of R_L which essentially means that you do not know what is the P_{out} that you are supposed to supply. If R_L increases the amount of P_{out} the amount of power that the network N has to supply will be smaller. If R_L decreases then the amount of output, a power output that the network N has to supply will be larger right? So, essentially even in order to maintain the same voltage as the input even in order to maintain the same voltage as the input you at times will require a network which can perform power amplification ok.

Now, there are applications there are certain applications in which you need to maintain this voltage V_{out} right whatever be whatever be that voltage might be you need to maintain that voltage V_{out} regardless of the value of R_L . If the R_L changes from very small value to a very large value then you then also output voltage has to be constant. One very important example of that is a voltage regulator right. You must have heard that the cell phones that we use or that or many of the mobile devices that we use they operate under certain supply voltages right and their performance might get degraded if the voltages fluctuate which essentially means that it is a job of certain block or certain analog device analogs network whose job will be to give a constant output voltage to regardless of whatever is happening in the network which means that your load R_L might change the temperature might change you might go from Kashmir to the deserts of Thar right everything around it might change however the output voltage has to be constant right and as we saw an example right now that having a constant output voltage also will require a device or also will require a network which can give you power amplification otherwise

you cannot really guarantee that the voltage will be constant because in order to hold a constant voltage across a variable load you should be able to supply variable power correct.

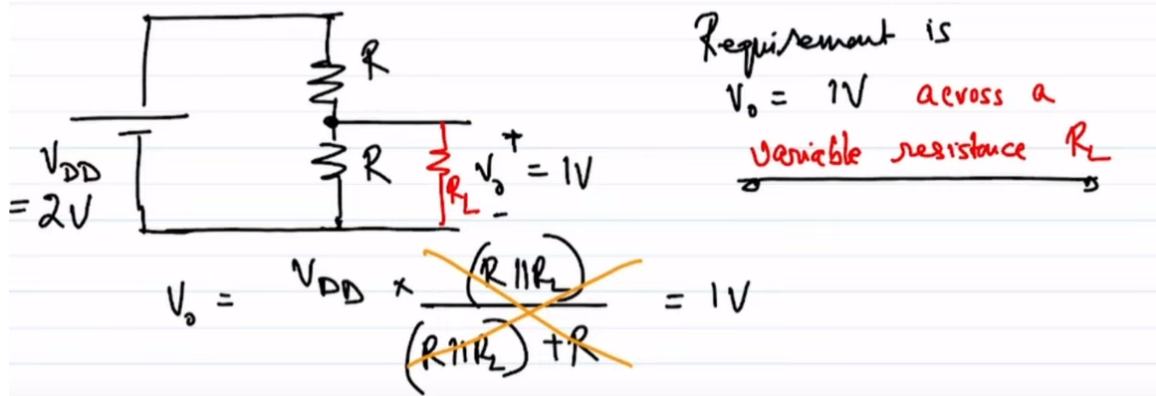


So, that that essentially is one of the main motivations of this course as to how do I design this network N which can give me the required amount of power regardless of whatever the load might be so that I am able to hold certain voltage across it or if the application requires I am able to supply certain current through it ok?

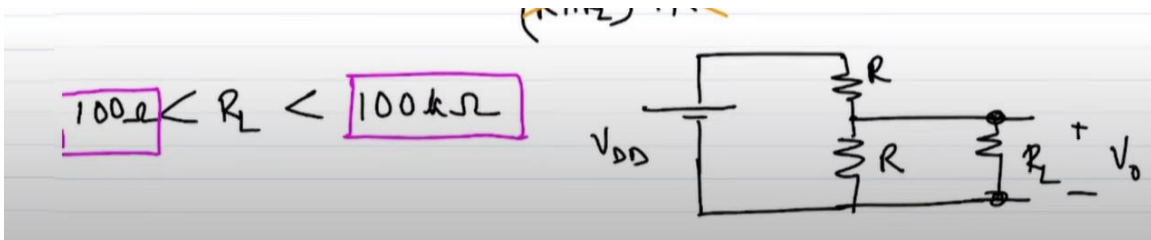
Now, let me give you another example of something that is not an amplifier, but hopefully will help you motivate hopefully will help you to understand the directions we will take in this course going forward. Take, for example, the case of a simple resistor divider. So, let's say I have a let's say I have a voltage source I have a battery let me call this VDD and I take a simple resistor divider. Let's say this VDD is of 2 volt say I have a 2-volt battery ok and I am interested in observing this voltage V not ok. And my requirement is so, what is the requirement? My requirement is let's say my requirement is V not should be equal to 1 volt ok. So, if V not is should be equal to 1 volt what is the how should I choose those values of the resistances? One might say hey how does it matter I can choose any two equal resistances let me call this R we call this R it really does not matter whatever the values of R is as long as the ratio of those of this resistor divider is 1 over 2 right then V not will be equal to 1 volt right simple enough.

Now, let's let me modify the requirement a bit and I say that hey, this is, this is not exactly what I wanted I want to supply 1 volt across a resistance R_L right? So, requirement is V not equal to 1 volt across a variable resistance R_L which means that I need to figure out right

I need to figure out what these values of R will be such that if I connect if I connect a resistance RL here I still get a value of 1 volt. How can I get that can you give me an example or can you solve this and tell me this is quite straightforward we can say that if I solve, if I solve Vnot over solve for the value of Vnot, what will I get I will get Vnot, Vnot will be VDD times R parallel RL by R parallel RL plus R and I will set this combinations of R and RL in such a way that this is equal to 1 volt right we can do that, but note that what is the requirement, requirement is RL is variable right. So, you cannot do this you cannot you cannot do this because RL is variable you might be able to satisfy this condition for a particular value of RL, but you will not be able to satisfy for a range of RL right? So, let's take some values now right?



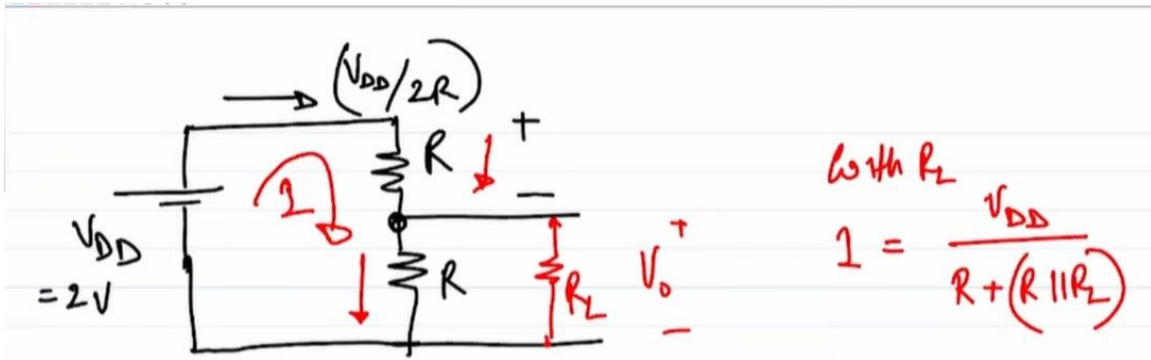
So, let's say, let's say RL, let's say RL varies between 100 ohms to 100 kilo ohms, right? let's say RL varies between 100 ohms to 100 kilo ohms and I would like to maintain 1 volt across it I have a 2 volt battery and I can choose whatever is the divider I want. So, what should I do? What is the what is the simplest solution that comes to mind? I am sure I am sure you have you have already figured it out the simplest solution that comes to mind is that I will choose this value of Rs such that the voltage Vnot such that the voltage Vnot is approximately equal to is equal to 1 volt under the worst case condition right and what is the worst case condition that I am talking about here? How do I figure out what is the worst case in this case? Because I have two conditions I have the conditions of RL minimum which is 100 ohm and RL maximum which is 100 kilo ohm. So, what is the worst-case condition in this case? If I if I set the value of RL to be equal to 100 ohm do you think Vnot will change drastically or if I set the value of RL to be equal to 100 kilo ohm Vnot will change drastically. Now, note that I have not told you what is the value of R.



So, herein lies the designers choice right what should be the value of R in order to figure out or in order to make this circuit work in such a way that V_{not} is almost equal to almost equal to 1 volt regardless of this range of R_L . What do you think should happen? In order to figure out what what should happen we first need to see what is fundamentally happening to this circuit once I connect R_L right. So, let's let's see what is happening to this circuit one once we connected R_L . So, let's say I have V_{DD} , you have R , you have R Let's say I did not connect R_L right? So, what was the current? So, this is 2 volt.

What was the current that was getting drawn from the battery? The current that was getting drawn from the battery was V_{DD} over $2R$, the current that was flowing through this R and the current that was flowing through this R were identical and hence you are getting a voltage of 1 volt across, across V , V_{not} ok. So, now, what happened once I once I connected R_L ? Two things happened one is the effective resistance changed right right. So, what is the current that you that you are now drawing in the presence of R_L changed right, right? So, what is the current that you that you are now drawing in the presence of R_L ? So, in the presence of R_L with R_L the current that I am now drawing is current that I am now drawing is V_{DD} over R plus R parallel ok. So, firstly this is different and since this is different right since this is different the drop across the drop across the top R changed right.

Since the drop across the top R changed the voltage V_{not} also changed correct. So, in a nutshell what happened after I connected R_L ? After I connected R_L the amount of current that I am drawing from this from the supply voltage V_{DD} changed and since that current change the drop across the resistance R changed and because of that the voltage V_{not} also changed. Now, obviously, we cannot do anything to this to ensure that V_{not} never changes, but can we do something in order to mitigate the effect of change of V_{not} after the application of R_L ?



In other words what we are asking what we are asking is how can we mitigate how can we reduce the extra drop across R once we connected RL right. So, in other words what we are asking is how can we reduce the extra drop across R when RL is connected? So, this is the question that we are asking. So, in order to answer this question we need to figure out which value of RL causes the most problem.

The lower value of RL causes the significant problem or the higher value of RL causes the significant problem right. Note that if I again go back to this to this case what does this tell us? This tells us that I have this condition of R parallel parallel RL in the denominator. So, clearly if RL is small if RL is small it will dominate and my current will be V_{DD} by R plus RL. If RL is much larger than R right if RL is much larger than R then the current will be almost V_{DD} by 2 R right. So, essentially the problem is for lower values of RL.

So, smaller values of RL causes the change in the effective resistance of the circuit right. So, smaller so, smaller values of RL causes change in effective resistance that V_{DD} sees and hence causes change in currents and change in V_{not} right. So, in other words there is the technical term for this in other words we say that RL loads the network ok. It is because RL loads the network it changes changes the output voltage. Now, you cannot wish away the effect of loading, but can we minimize its effect? Yes we can what can we do to minimize its effect? We can ensure that for all conditions of RL the value of RL is much greater than something.

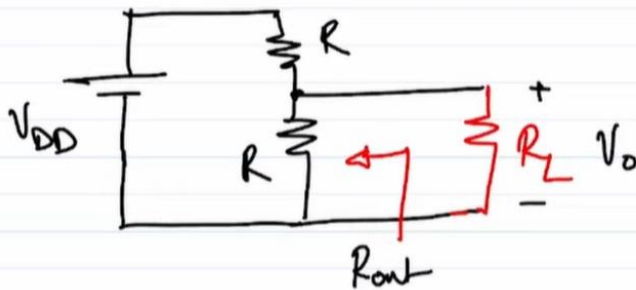
What values of R will minimize the drop across R when R_L is connected?

Smaller values of R_L causes change in effective resistance that V_{DD} "sees" and hence causes change in currents and change in V_o .

R_L loads the network.

What should it be much greater than? It should be much greater than. The value of RL should be much greater than the impedance that that RL sees looking into the network right. So, if I say that this is R_{out} , if RL is much much greater than R_{out} then what will be V_{not} ? What will be V_{not} ? V_{not} will be or rather than I can say that then RL does not load the network correct. And what is R_{out} ? What is the effective R_{out} in this case? So, effective R_{out} in this case is equal to how do you figure out what is the effective R_{out} of any network? You desensitize the input right. So, you redraw the essentially you redraw your network, you redraw your network R and you figure out from which port you are trying to from which port you are trying to find the effective output output resistance.

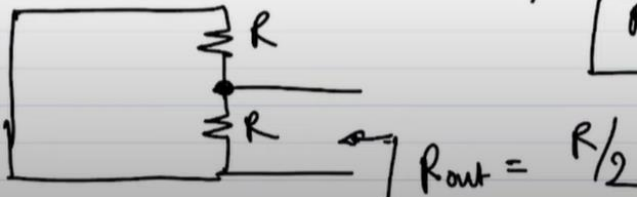
You desensitize your supplies that is if it is a voltage source you set it to 0 which means you short circuit the voltage source. And once you look into this network whatever resistance you see effective is the output resistance and what is the R_{out} that you see? This R_{out} is equal to R by 2. So, if you ensure that if we ensure R_L to be much much greater than R by 2 or R , Let me, let me, put it in other way if we ensure that R by 2 is much much less than R_L then you will be able to ensure that V_{not} is approximately equal to V_{DD} for the all for all V_{not} is approximately equal to V_{DD} over 2 for all ranges of R_L . And for that which is the constraint on R_L that you need to check this should be the constraint on R_L mean right. If you can ensure that then we will be able to we will be able to ensure that V_{not} is approximately equal to V_{DD} over 2 and that is what we wanted ok.



If $R_L \gg R_{out}$ then R_L does not load the network.

If we ensure

$$R/2 \ll R_L(\min)$$



Now, the problem here is the problem here is the following ok. Let me take a step back and ask you request you to solve this question using brute force method. Let us say that we do not know how to figure out the output resistance we just want to we just know that this equation is valid and we know that V_{not} is equal to V_{DD} minus this I times R and I need to figure out what will be the constraint on R what will be the constraint on R in order to ensure that V_{not} is approximately equal to V_{DD} by 2 for all ranges of R_L and R . So, what should be the constraint on R in order to ensure that? So, I would like to request you to pause the video here and do it yourself without resorting to whatever we just did that is finding out the output resistance and trying to figure out what will be the constraint from there ok.