**Course name- Analog VLSI Design (108104193)**
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Lecture- 12, module-1

Now, welcome back this is lecture 12. So, in the previous lecture we were trying to build an amplifier which was supposed to give us some amplification of power using a MOSFET and we and we noticed that in order to come from in order to arrive from the small signal incremental model of our MOSFET to a full blown MOSFET architecture with all the biases in place we had to make some we had to make some adjustments in order to accommodate for the required quiescent conditions right. And we were halfway through because what we said was under the given conditions that we want a gain of let us say 10 across a resistance RL of 1 kilo ohm we know we saw that we required a we required a gm or a Y21 or a gm of the transistor to be 10 millisiemens from that we back calculated we back calculated the required overdrive that is the VgsQ minus the threshold voltage from there we need we got the value of Vgs in order to get a in order to get a gm of 10 millisiemens right. And that Vgs came out to be 6 volts then we had to ensure that that 6 volt Vgs remains applied right I mean the incremental signal that I am trying to the incremental signal that we are trying to amplify should be riding on top of the Vgs right. We cannot just simply apply the incremental signal to the gate of the transistor because the transistor will will not be on ok. And then we came up with came up with the architecture of the input loop right.

And then we saw that if we do this not only we will have a current a quiescent current of 25 milliamps. So, this is quiescent this is IDSQ, but also we will have incremental current ids and the total current will be the quiescent with the quiescent plus the small signal incremental. And note that if we go back to lecture 11 you would have seen that the way we came up with this incremental topology or the mathematics behind this was we used the full blown equation of the MOSFET assuming that MOSFET is in saturation. And then in the full blown equation we neglected the higher order terms right.

So, that in essence is the that in essence is the approximation a small signal approximations we have not yet we have not yet seen under what condition of Vi that small signal approximation holds, but we have assumed that let us assume that the Vi is small enough for the small signal approximation to hold. So, we will go back later and see under what condition in a MOSFET the small signal approximation holds good right. For the time being we will assume that the small signal approximation holds and we will simply say

that the total current is the total current flowing between the drain and the source is the quiescent current plus the small signal current the incremental small signal current that is gm times Vi ok. Great. Then we turned our attention to the output side what is the output? Now output is across RL.

Lecture 12

$$\mu_n C_{ox} = 0.2\,mA/V^2, \quad V_{TH} = 1V$$
$$W/L = 10, \quad R_L = 1k\Omega$$
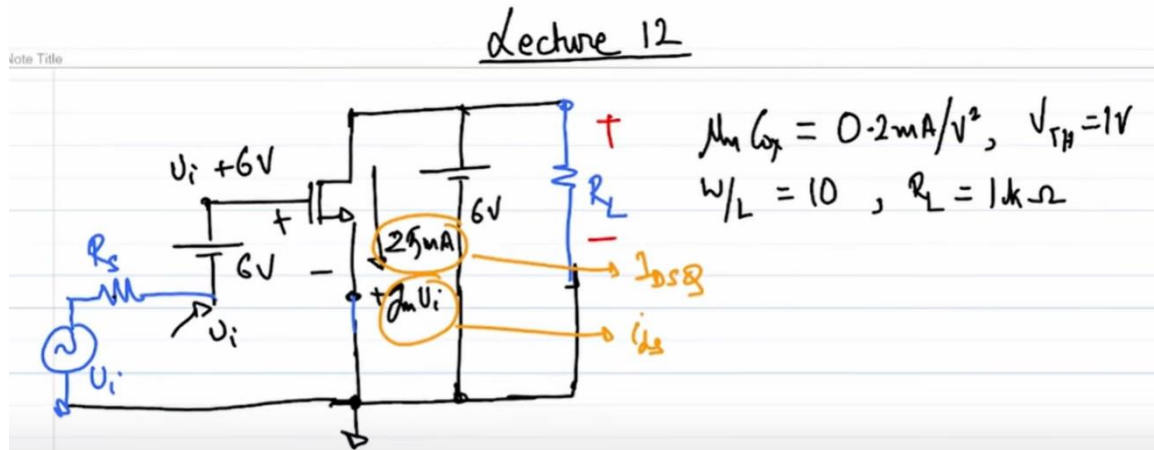
 Now what do we see? At the output what is the voltage across RL? Clearly the voltage across RL is 6 volt because I have a battery clamped across RL. So, whatever regardless of whatever incremental or changing current that flows to the MOSFET it will not be able to change the voltage across across RL right. So, what is the solution? So, putting RL in parallel with the battery does not seem to be a solution I mean if not in parallel what is the other thing that we can do? We can try putting RL in series with the battery. So, let us do that. So, if we put RL in series with the battery let me get rid of these details.

 So, let us put RL in series with the battery same battery 6 volt in series with RL right. So, what do you think will change or I mean the first thing we need to satisfy see moment to change anything in the circuit the moment to change anything in the circuit which can potentially change the quiescent conditions you need to go back and check whether the quiescent conditions under which the transistor is supposed to work still holds true right. For example, in this case what do we want? We want the transistor to remain in saturation right regardless of whatever happens ok. Unless the transistor is in saturation we are not going to get any amplification. So, it is imperative to always ensure that the transistor remains in saturation if we are looking to get gain out of out of the amplifier.

 So, since we have moved the battery we now need to check whether the transistor remains in saturation under quiescent condition right. So, basically first thing is check operating point right. So, how do I check operating point there are there are three operating regions one is cut off right one is off transistor is off one is it is in linear region which is also by the way called triode region and another is saturation. So, what we will do is we will not

try to assume will not try to derive whether the transistor is in saturation or a triode or whatever we will assume a region of operation and then try to see whether the assumption holds true or not ok. So, this will be the recurrent theme through the course.

So, we will assume that the transistor I mean whatever we are trying to achieve is going to work and then we will back test our idea and see whether the assumption holds true or not ok. So, let us assume that the transistor in saturation is in saturation right. So, we will assume MOSFET is in saturation ok. So, if the MOSFET is in saturation what is the current that what is the quiescent current that is that is supposed to flow. Note I am not talking about incremental current which means I am assuming that Vi is 0 right.

So, we can as well put Vi to be equal to 0 right because we are doing quiescent analysis. So, when we are doing quiescent analysis this is regardless of whether you have applied a signal or not right. So, in case of a in case of a voltage source we need to desensitize the voltage source and desensitizing the voltage source means we have to short circuit the voltage source ok great. So, now if we assume MOSFET is in saturation what will be IDSQ? So, you can look back in your in your notes of the last previous lecture your IDSQ assuming saturation condition will be half u n C ox W over L, VGSQ that is 6 volt minus threshold voltage that is 1 volt whole square and if we do this calculation what did we get we got 25 milliamps. So, this is supposed to be 25 milliamps assuming saturation condition.

Now, we need to go back and check whether the saturation condition is indeed true or not right. So, what do we need to check what is the test for saturation? The test for saturation is we need to check the drain voltage we need to check the gate voltage and we need to see whether the drain has gone down one threshold voltage below gate or not that is the only thing right. Note that we need not bother about the source right saturation condition the saturation condition is VDS should be greater than VGS minus threshold voltage source is common on both sides of the non-inequality source goes off. So, essentially we need to satisfy check if VD is greater than equal to VG minus threshold voltage. Again note that you need not bother about the source voltage right source can be anything in this case is trivial in this case source is grounded, but you will see later on we will have topologies where source is not grounded, but you do not I mean when you are trying to figure out whether the transistor is in actually is in saturation or not you need not bother about the source.

What do you need to bother about? You need to bother about the drain voltage and the gate voltage right the absolute drain voltage and the absolute gate voltage and see if the condition of VD greater than equal to VG minus threshold voltage holds on right. So, let us assume let us see whether it holds or not. So, this is 25 milliamps right. So, what should I do if we assume IDSQ is 25 milliamps and you have a battery of 6 volts what is the what

is the drain voltage what is the drain voltage VD now. So, you have this is this voltage is 6 volt minus RL times IDSQ which is how much RL is 1 kilo ohm IDSQ is 25 milliamps essentially 6 volt minus 25 milliamps 6 volt minus 25 volt that is minus 19 volts.

 So, clearly this is not in saturation not only the not only that this is not in saturation this is telling us that the drain is below ground right which clearly is not possible right because if you have a circuit where the minimum voltage is ground it cannot go beyond that right. And I mean if you have an LTI circuit right where you are not purposefully trying to get a voltage lower than the ground or higher than the VDD you will not get a condition where under DC under DC operating point a voltage is minus 19 volt ok. So, which means that assumption is wrong right. So, in this case VD is equal to minus 19 volt which implies as a saturation assumption is wrong is incorrect ok. So, if it is not in saturation obviously it must be linear and we need not go about and figure out how deeply linear region it is because we are not bothered about linear region at all.

 So, all we need to care about is what should we do in order to bring the transistor back into saturation ok. So, next thing will be modify biasing point to get MOSFET back in saturation region ok. So, what should we do? How can we get it back to saturation region? What do you think needs to be done? So, clearly in a saturation region I need the only thing that is that is sacrosanct is IDSQ has to be equal to 25 milliamps right. So, if I only concentrate on if I only concentrate on that part of the circuit ok. What should I see? I should essentially see that I want an IDSQ of 25 milliamps correct.

 This is we want right if it is in saturation this is what it is supposed to be and since what

is the transistor? A transistor is a current source is a voltage control current source, but it is a current source nonetheless right. So, we were we can essentially replace the transistor with a current source of 25 milliamps if it is in saturation. Then what? This is supposed to go through a resistance of 1 kilo ohm and we are supposed to have a battery here. Let us call this battery beginning. Now what all things are negotiable here? What all things you can change and what are the things we cannot? Clearly this cannot be changed.

When I mean it cannot be changed what I essentially mean is that this has been fixed by a specification right. We came to this IDSQ not just by Fluke it was a requirement of the it came from a top level requirement right. We started off with a gain of 10 across a volt across a resistance of RL. We know the gain is gm times RL which means if RL is 1 kilo ohm gm has to be 10 milli siemens from the value of gm of 10 milli siemens we figured out what the Vgs needed to be assuming certain value of W by L we figured out what the gm needed to be or rather we figured out what the Vgs needed to be. From that Vgs we back calculated the required IDSQ which means we need this much IDSQ right.

So we do not want to change IDSQ because if we change IDSQ our gm will get affected which in turn will affect our gain. RL can we change RL? We cannot change RL because RL has been given by a specification that we need to get a gain of 10 across RL so RL we cannot change. So what else can we change? Obviously we can change VDD right. So now the question boils down to what is the minimum VDD right. Find VDD minimum for which let me call this MOSFET M1 instead of repeatedly writing MOSFET M1 is in saturation right.

Why do I say minimum? Because clearly 6 volt is not sufficient which means I need higher and higher VDD right. So the hope is that if I raise the VDD the transistor will go closer and closer to saturation and then we will reach that magic VDD value for which the transistor is actually in saturation right. So what am I looking for? I am looking for the transistor to be in saturation then what is the required voltage at the drain for the transistor to be in saturation? So required what am I asking is what is this is VD what is the required VD? So clearly the required VD that is the drain voltage is required VD is required VD has to be greater than or equal to the gate voltage the gate voltage which is 6 volt minus let me write it in this form VG minus threshold voltage which is 5 volt. So now clearly if VD is greater than 5 volt I am good but what is the minimum VD in order to keep the transistor in saturation? So VD min is 5 volt right. So what is the corresponding node what is the corresponding node on the circuit on the right that corresponds to VD clearly this is VD.

So that has to be equal to 5 volt if this has to be equal to 5 volt then what should VDD be? So VDD has to be 5 volt plus 25 milliamps times RL, RL is 1 kilo ohm which means it has to be 30 volt and so this is essentially VDD min right. If you increase VDD beyond 30

volts fine your transistor will be in saturation more comfortably but this is under the condition that the transistor is barely at the edge of saturation. Saturation okay. So now the question is what happens when I put the input back right. What am I asking is do you see an issue what I am essentially asking is this do you see an issue if I put the VI back in the network.

So now what is VDD? VDD is equal to 30 volt right. VDD is equal to 30 volt what is the drain voltage the drain voltage is 5 volt right. So now do you see an issue if I put VI back in the network. Let us assume VI equal to a VI is a sinusoid. VI is some sinusoid Vp sin omega naught t where let us say Vp is equal to 100 milli volt.

So it is a 0.1 volt. Small signal I mean I just applied a 100 milli volt signal I mean even though we have not really established what is small signal what value is small signal let us

assume for the time being that this is small signal again kindly bear with me we will see whether this can be characterized as small signal or not sometime later okay. So what do you think do you see an issue with this architecture if I now apply a sinusoid of amplitude 0.14. I request you to think about it for a second and we will meet after that okay. So let us stop here and see you in the next class. Thank you.