

Course name- Analog VLSI Design (108104193)
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Week- 4
Lecture- 11, Module-1

Welcome back, this is lecture 11. A few lectures back, we saw that in order to make a non-linear in order to make a good amplifier which can indeed amplify power, we needed a device or we needed a network that had the following small signal characteristics, right. So, if our two port network were like this, if the two port network model for the incremental network were like this, where this conductance is y_{11} , this conductance is y_{22} , the transconductance in the input side is y_{12} times v_2 , where v_2 is the voltage at the output port and the transconductance at the output side was modeled as y_{21} v_1 , where v_1 was the voltage at the input port, right. And if we were to connect we were to connect an input with a finite source resistance R_s at the input port and if we were to take the output across another resistance R_L across the output port, then we saw that and wish list for our ideal. So, wish list for an ideal amplifier would have been y_{11} should be 0, y_{12} should be 0, y_{22} would be 0 and y_{21} should be as large as large as possible, right. Then in our quest for finding such a device, we landed up with one such device, which was a MOSFET and n MOSFET in particular which is a three terminal device, right which is a three terminal device.

Under saturation condition i.e. $V_G - V_S \geq V_{TH}$

$$V_D - V_S \geq V_G - V_S - V_{TH}$$

$$\Rightarrow V_D \geq V_G - V_{TH}$$

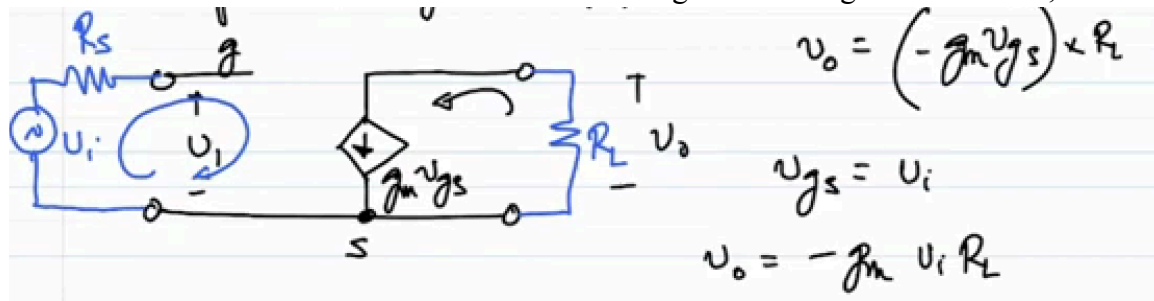
$$\Rightarrow V_G - V_D \leq V_{TH}$$

$$y_{11} = 0, \quad y_{12} = 0, \quad y_{22} (g_{ds}) = 0$$

$$y_{21} = g_m = \mu_n C_{ox} \left(\frac{W}{L} \right) \underbrace{(V_{GS} - V_{TH})}_{V_{ov}}$$

The port 1 is connected between the gate is v_1 , the port 1 is connected between the gate and the source and the port 2 is connected between the between the drain and the source.

And then we saw that if the MOSFET is in saturation, right. So, under saturation condition that is what is saturation condition? Saturation condition is firstly it has to be on, right the MOSFET has to be on which means voltage between the gate and the source has to be greater than some threshold voltage which is a characteristics of the MOSFET that the threshold voltage V_{th} will be given to us, right it is a characteristics of the MOSFET. And under saturation condition that is V_{gs} should be greater than V_{th} , another



we need to satisfy another condition that is V_{ds} , $V_d - V_s$ should be greater than $V_{gs} - V_{th}$ - threshold voltage, right, right.

In other words you see that source is common between both sides of this inequality. So, they go off which means that we just have to ensure that the drain voltage is greater than gate voltage $-V_{th}$ right. So, essentially if we can ensure these two conditions that is V_{gs} is greater than equal to the threshold voltage and the voltage at the drain or rather this voltage difference between the gate and the drain, is not less than a threshold voltage, right. So, what is this inequality telling us? This inequality can also be written in the form of $V_{gs} - V_d$, right. V_{gs} if I move it to the other side $V_{gs} - V_d$ should be less than equal to threshold voltage, right.

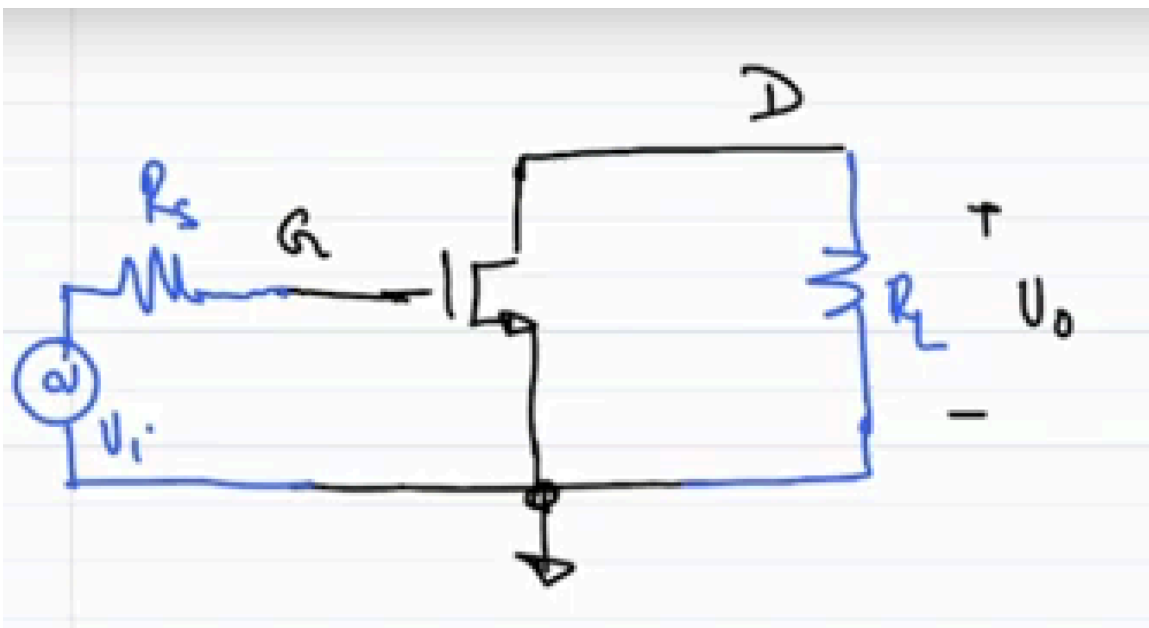
So, in other words what is it saying? It is saying that the gate voltage, the voltage at the gate can be even higher than the drain voltage, but by a maximum of one threshold voltage, right. So, if these two conditions are satisfied, that is V_{gs} is greater than a threshold voltage and drain is not lower than the gate by more than one threshold voltage, right. So, your saturation condition is met and under the condition of saturation, under the condition of saturation we get these conditions that is Y_{11} is equal to 0, Y_{12} is equal to 0, Y_{22} which we also call as the conductance between the drain and the source that is g_{ds} is also equal to 0 and Y_{21} which we call as g_m is equal to $\mu_n C_{ox} W/L (V_{gs} - V_{th})$. Now, note that this g_m , right, what we want Y_{21} to be? We want Y_{21} to be as high as possible and this seems to be doable since these factors W/L and $V_{gs} - V_{th}$ or in other words the overdrive is under the control of a designer, right. So, we can choose, we can pick and choose values of W over L and $V_{gs} - V_{th}$ or the overdrive of the MOSFET.

Since we can pick and choose these values we should be able to get a value of a value of Y_{21} which is sufficiently high, right. So, if this is possible, if this is possible what is the

next step? The next step is to see how can we use this MOSFET, how can we use this MOSFET to suit our purposes, right. So, in other words what we are asking is that, ok, it is well and good that it is well and good that does this MOSFET seems to MOSFET in saturation seems to satisfy the conditions that is required to get amplification of power, right. But I mean ultimately you have to put things together we cannot just simply say here is your MOSFET bias it in saturation and you will get amplification of power, right. We will have to ensure that we have to ensure that this is indeed achieved, right.

So, let us so next step of next obvious step is to see how can we achieve both, right. So, what is the thing what are we after? The next goal is to next goal is to bias the MOSFET in saturation and apply a small signal input or an incremental input to get amplification, ok. So, let us dive in. So, what is the incremental model of our MOSFET? The incremental model of our MOSFET lets us do both together. So, what is the incremental of the incremental picture of our MOSFET? The incremental picture of MOSFET is this.

So, this is g_m times V_1 what is the V_1 ? V_1 is this voltage this is V_1 , but note that this V_1 is between a gate and a source. So, g_m times V_1 we can also write it as g_m times V_{gs} , right g_m times V_{gs} , right. And where are the incrementally where are the inputs and outputs connected? Incrementally a source will be connected here I dot s and the load will be connected here, right. So, incrementally if this is if this is achieved what will be if this is V_{naught} what will be V_{naught} over V_i ? So, V_{naught} is nothing, but the current that is g_m times V_{gs} , right the current that is g_m times V_{gs} times R_L , but the sign will be flipped because of the way the voltage V_{naught} is marked, right. I am drawing current out I am drawing current out of the resistance R_L .



So, V_{naught} is that voltage difference across R_L is minus g_m times V_{gs} this is the current times R_L . What is V_{gs} ? What is V_{gs} ? How do I know what is V_{gs} ? If I do a KVL in this loop in the input loop. So, if I do a KVL in this input loop what do I get? Is there firstly is there any current in this input loop? No there is not because I have an open circuited at the input terminal, right. So, there is no current. Since there is no current what do I get? V_{gs} is equal to V_i .

So, if that is the case if I plug in this value in the top equation. So, V_{naught} becomes minus g_m times V_i times R_L and V_{naught} over V_i that is the small signal gain becomes minus g_m times R_L , ok. So, so is this is good or bad is this is good news or bad news? Clearly this is good news because now this gain, right. So, this gain this A_V is minus g_m times R_L , right. And can this be made as high as possible? Clearly yes because R_L is fixed because R_L has been given to us by some external specification, but this value of g_m , right this g_m is a designer control variable, right.

The g_m is a designer control variable we can tweak the g_m , right. We can design the g_m to suit our purposes by changing by changing the W over L the aspect ratio of our device, right or by changing the overdrive of the device, right or changing V_{ds} minus V_{th} or by changing the overdrive of the of the device, right. And note that this V_{gs} minus V_{th} or the overdrive are at the quiescent parameters, right. So, that is the these are the parameters at these are the quiescent voltages at which our MOSFET is has been biased, ok, ok. So, now now the question is this is I mean this still is an incremental incremental model, right.

I mean I do not see a MOSFET here I I see the incremental model of the MOSFET. So, we have to put a MOSFET in this case, right. So, what if what if or what is the next thing? So, so what we will see try to see is what if we replace this incremental model with its with a MOSFET, right. So, let us do that. So, how should we replace the incremental model with the MOSFET? Now, note that note that in a MOSFET the gate is one terminal, right.

So, if this I if this is V_1 , V_1 is the voltage between the gate and the source this is gate this becomes the source, right and V_2 is the voltage between the is voltage between the drain and the source, right. So, let me just mark it here. So, V_1 becomes the voltage between the gate and the source and V_2 is the voltage between the drain and the source, right. So, how should I connect the MOSFET? The MOSFET is connected like this, ok, right. So, let us redraw this.

Now, who decides again who decides which is the drain and the source terminal because

the MOSFET is physically symmetric device. Clearly the voltage that the terminal between drain and source which is a higher potential is a drain, right because pinch off happens. I mean you apply the voltage when you apply a higher voltage at the drain side the electrons in the channel get sucked out from the source and get dumped on the drain or drained out from the terminal that is why it is called a drain, fine. So, now we need to ensure that this is what is the first thing we need to ensure? If we ok let me do this experiment with you and if we if I say that if I directly connect these sources and these loads here what is going to happen, right. So, let us do this experiment. So, let us say I connect I connect the source B_i and the load R_L like this what is going to happen and for the sake of simplicity let me just say that this common terminal the source seems to be a common terminal between the input and the output, right.

The source seems to be a common terminal between the input and the output and we know that every reference circuit every circuit that we do has one common terminal with respect to which we define all the voltages, right because the absolute value of voltage does not have any meaning it is always a voltage difference between the two nodes that we are referring to and when we say that the voltage at this node is 2 volt or 5 volt or 3 volt we implicitly assume that there is one reference terminal from which we are the difference from which is 3 volt or 5 volt or 2 volt or whatever you are measuring and that reference terminal that common terminal we typically call it as ground. So, since in this particular configuration note that it is not true for all configurations in this particular configurations since the source seems to be the common terminal between the input and the output, right. So, we call this we call this let us call this ground, right. So, we call this as a, let me change the color. So, we call this ground, right.

Since so, since source is a common terminal we will we call it ground. So, what I have request you to do is to take a moment and tell me what will be what will be the V_o over V_i or what will be the what will be the procedure that we should follow in order to figure out what will be V_o over V_i , right. We will see you in the next class. Thank you.