An Introduction to Coding Theory
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Indian Institute of Technology, Kanpur
Module 04
Lecture Number 17
Convolutional Codes: Classification, Realization

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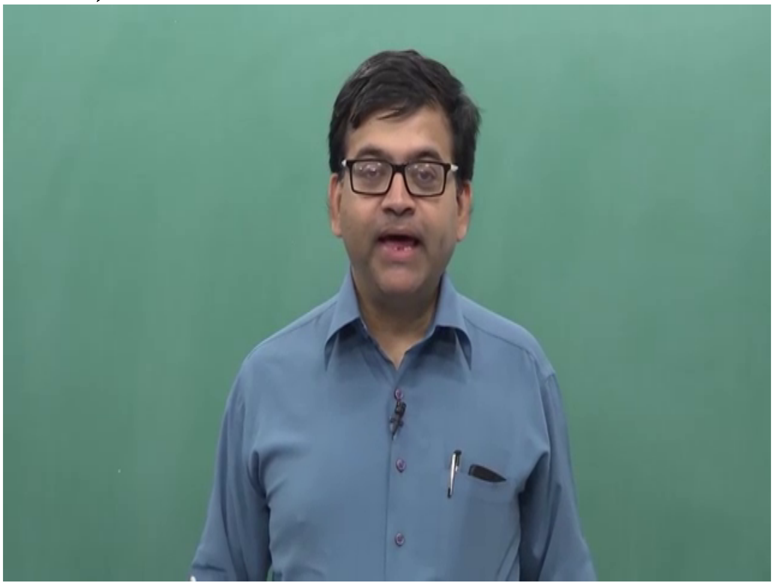

In this lecture today we are going to talk about

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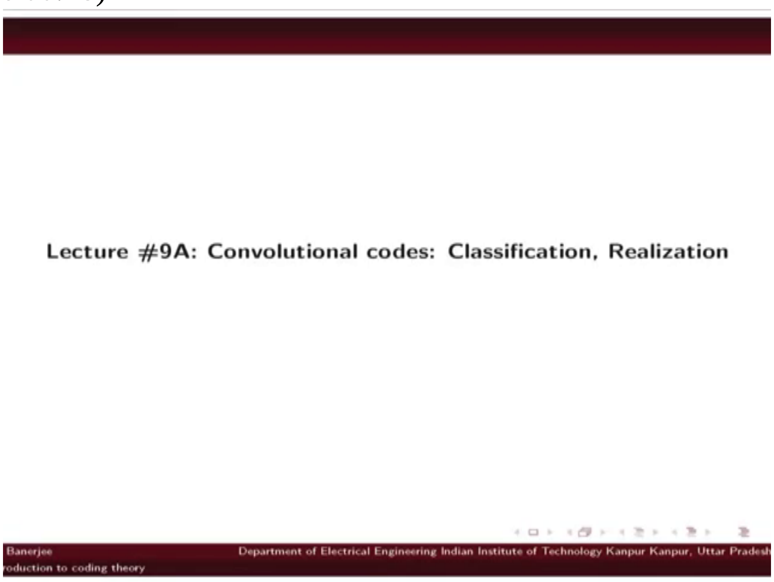

classification of convolutional codes based on

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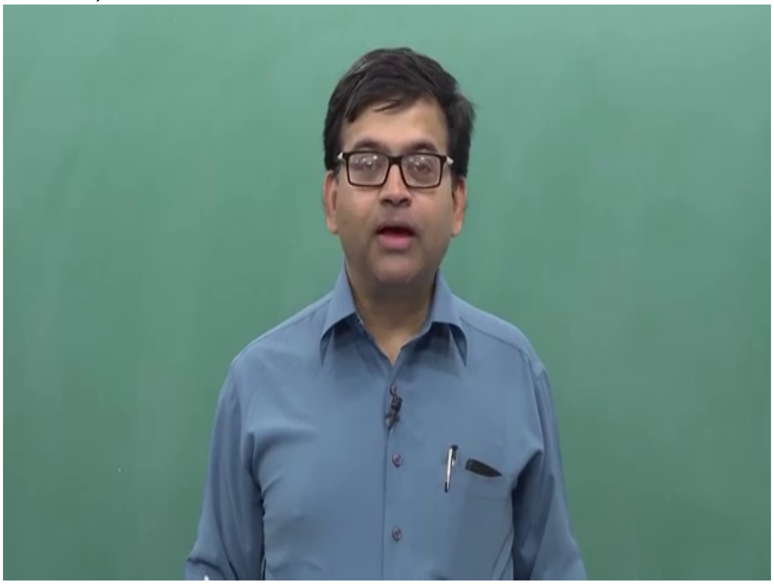

type of connections between the output and the input. Also based on what are our output bits, we will classify convolutional codes into systematic and non systematic codes. Then we are going to talk about how we can realize convolutional codes using shift registers. So

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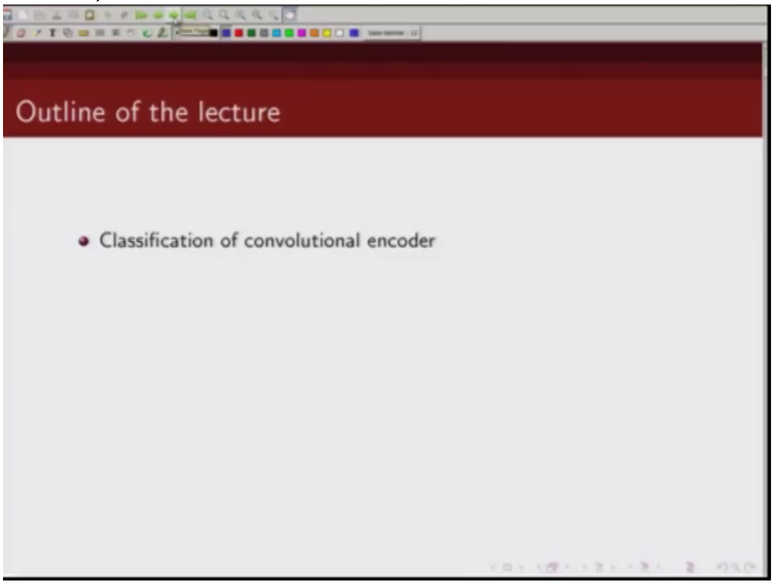

as I said first we will talk about convolutional codes

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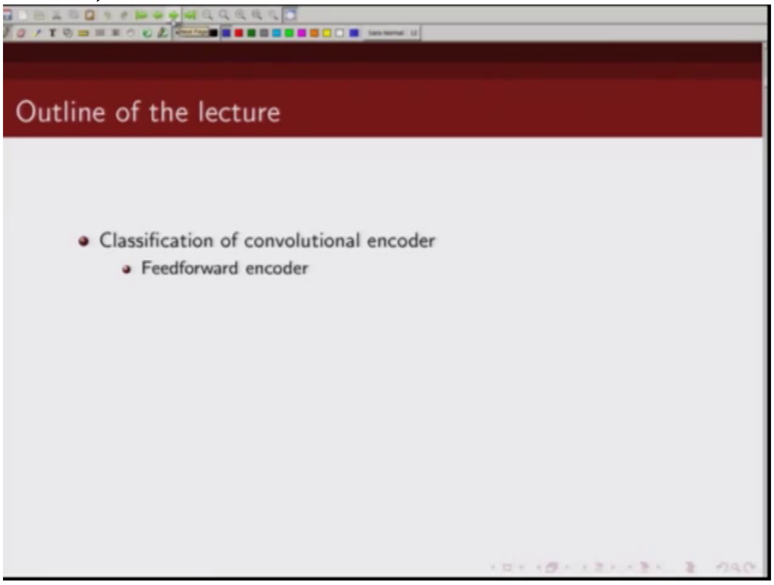

and in this we are going to

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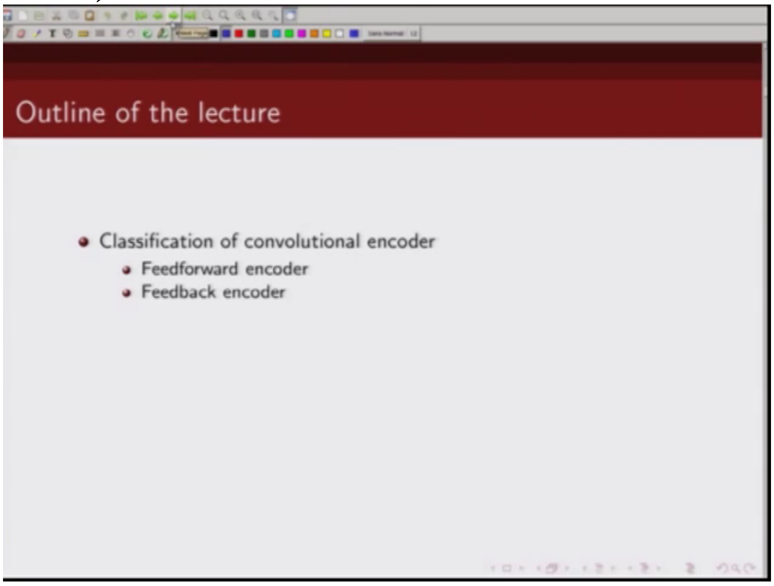

talk about classification based on types of connections between the input and the output of

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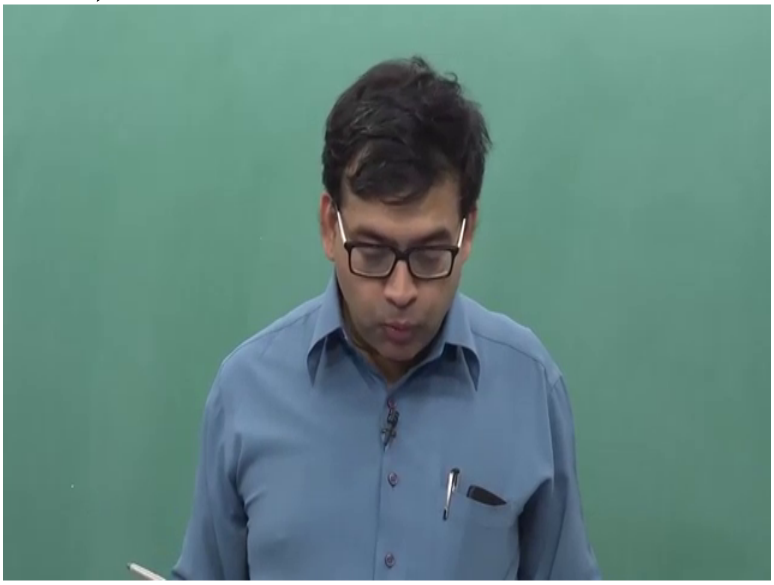

the convolutional encoder. In this regard we are going to talk about what do we mean by feed forward encoder and feedback encoder.

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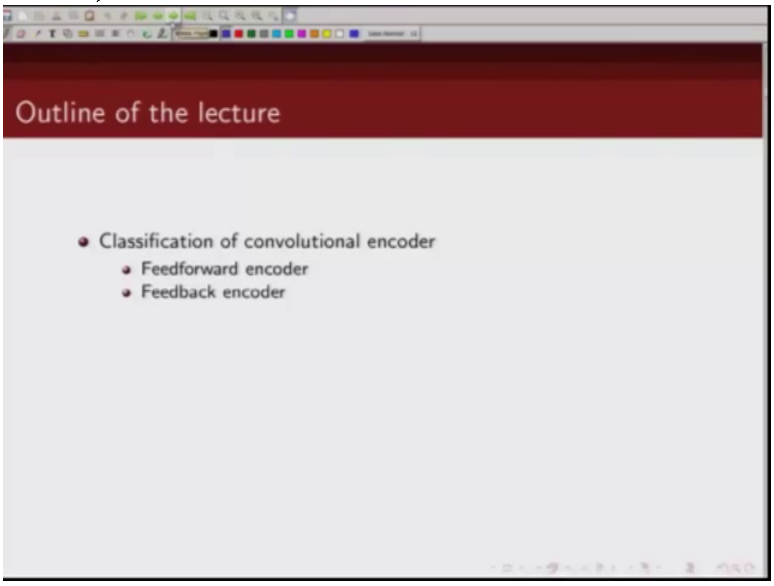

Then we are

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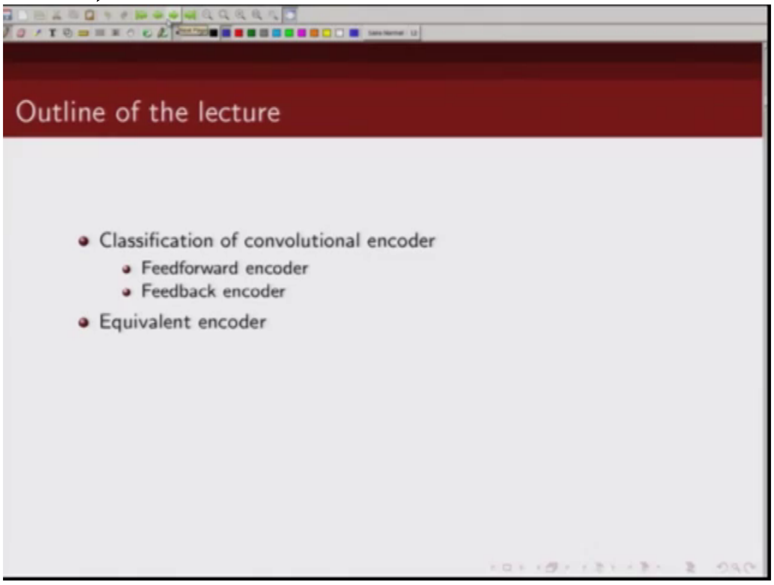

going to introduce a classification based on what are the output bits.

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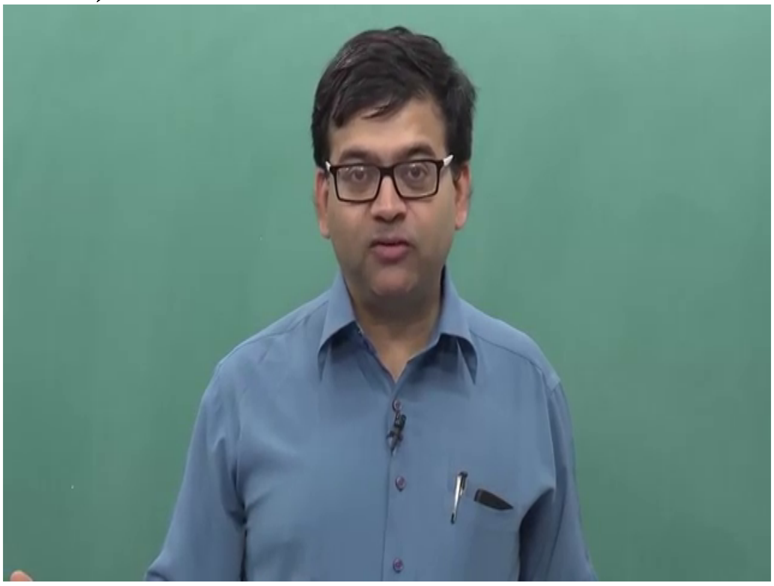

Whether the information bits directly appears in the output or not, based on that there will be a classification of convolutional code,

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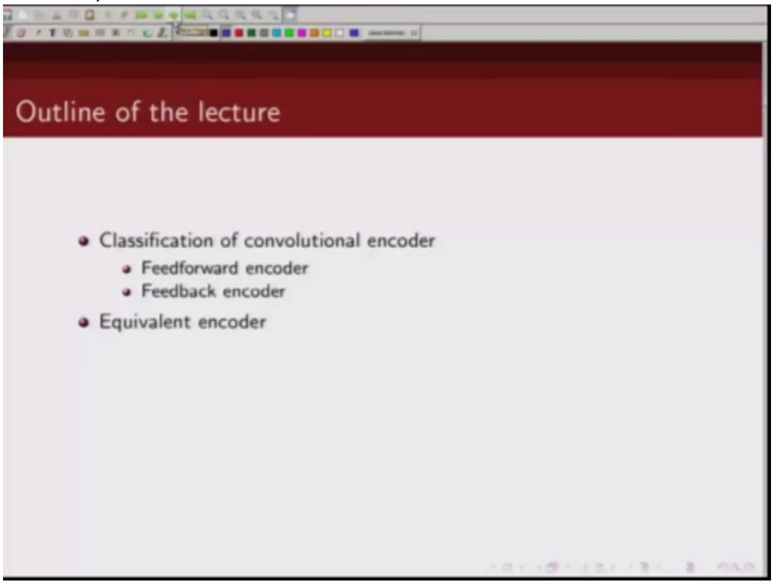

the encoder basically where information bits can be separated out is known as systematic encoder and in

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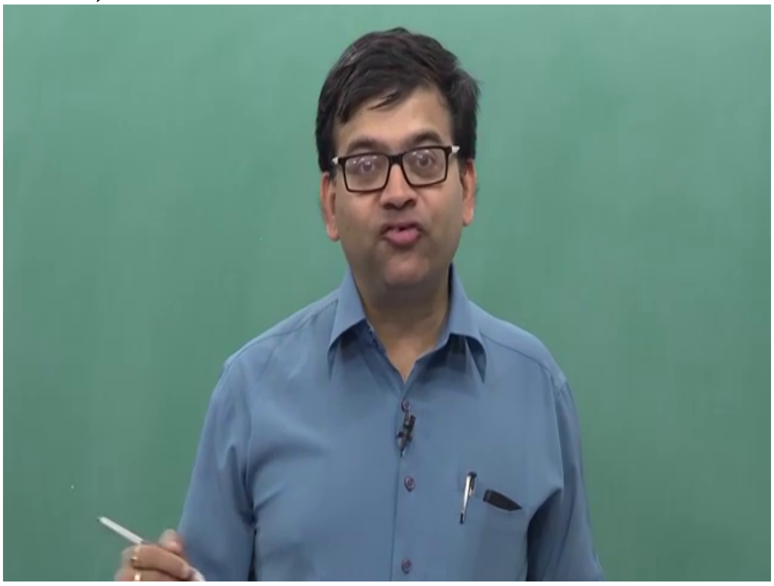

non systematic encoder we cannot separate out information bits directly from the parity bit. So we will talk about what do we mean by systematic encoder for convolutional code and non systematic encoder. And then we will introduce the concept of equivalent encoder.

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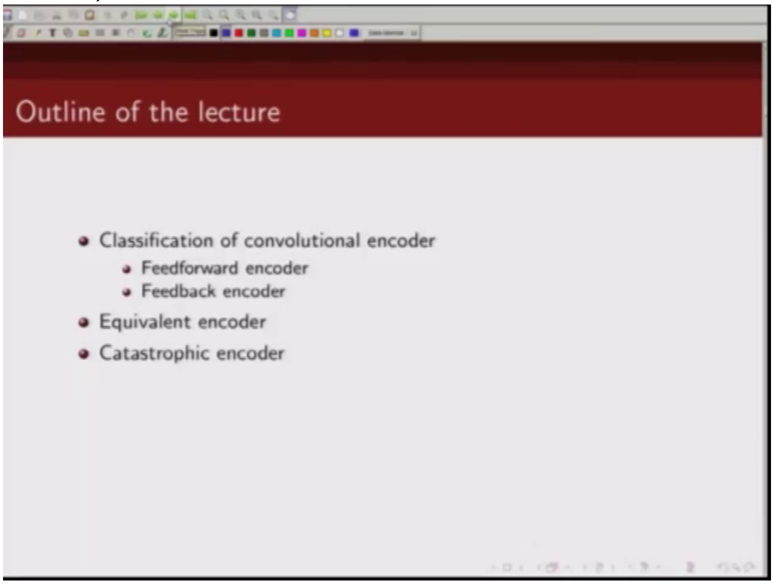

For every non-systematic encoder there is an equivalent systematic encoder and through an example we are going to illustrate how we can get its equivalent encoder. Then we are going to talk about a class of encoder where, if the input bits are very high

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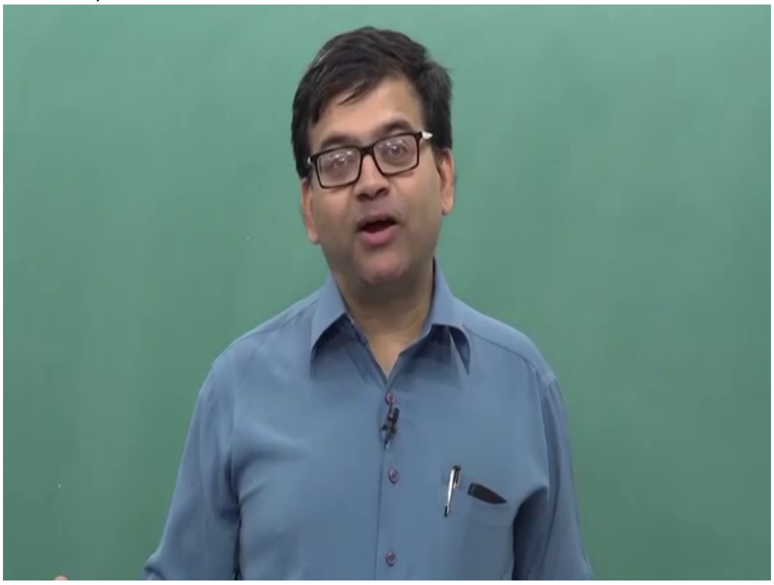

weight we can still get an output codeword of very low weight and these kinds of encoders are known as catastrophic encoders.

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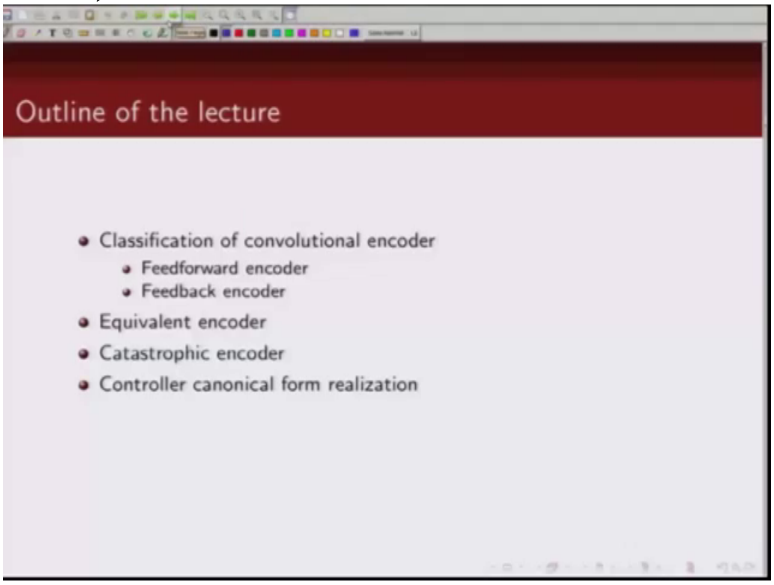

And finally we are going

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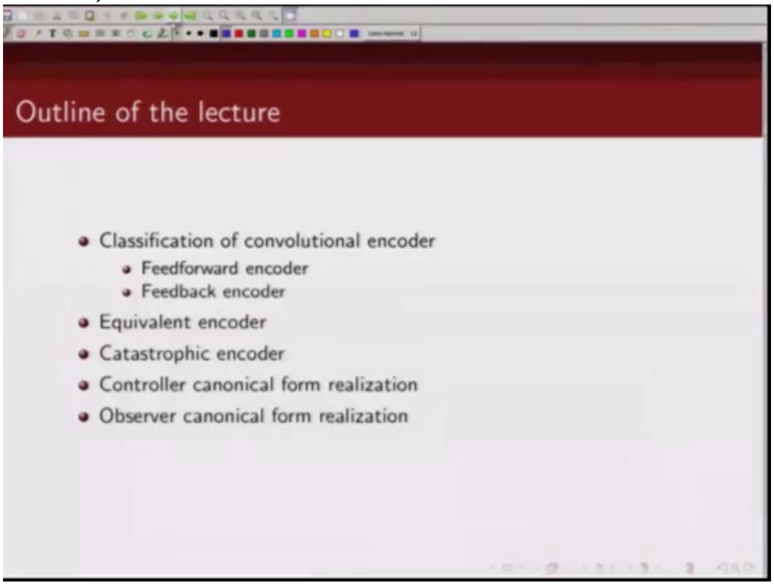

to talk about 2 different types of realization of convolutional codes using shift registers, the first one which is known as controller canonical form realization and the second one is known as observer canonical form realization. And

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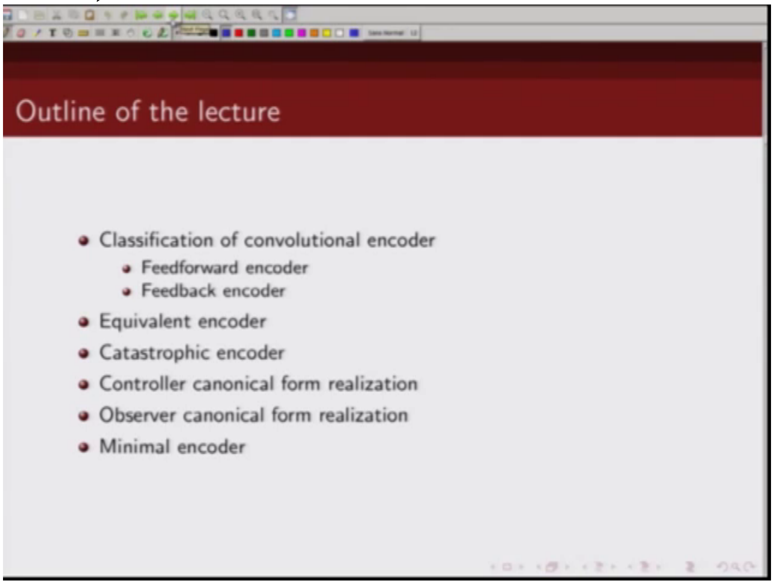

finally we are going to conclude this lecture with the concept of minimal encoder.

So let us

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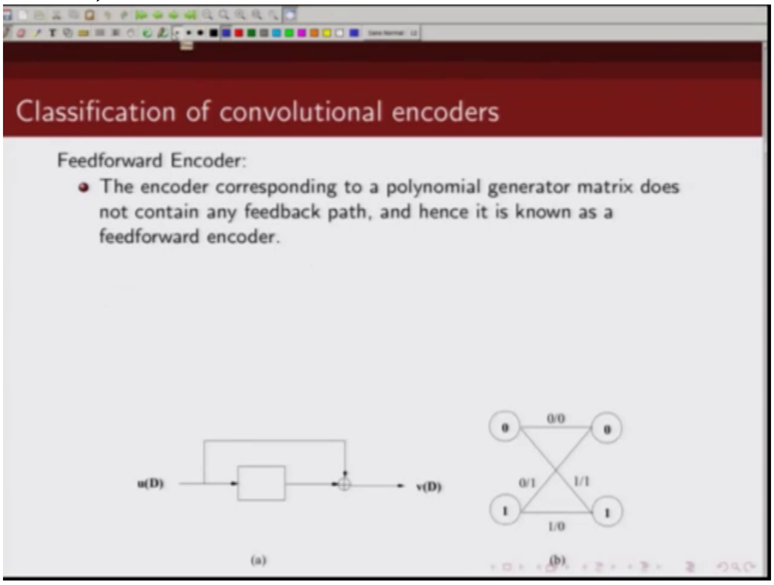

start our discussion on classification of

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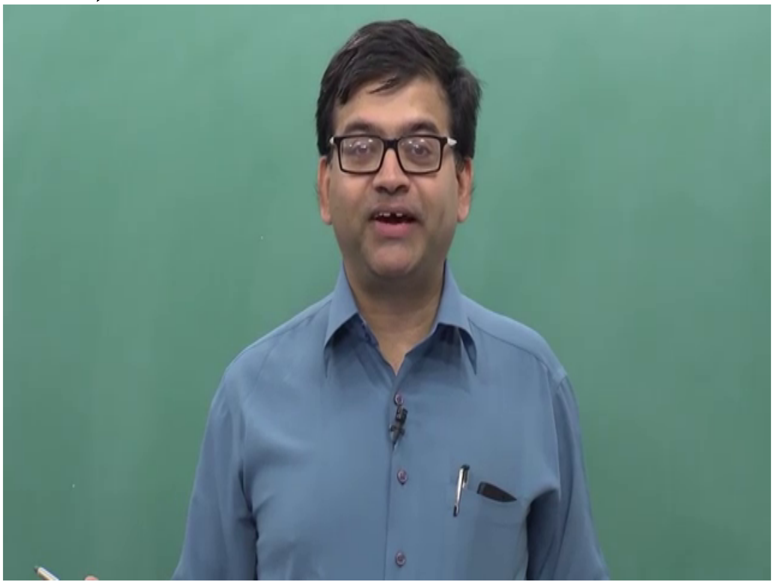

convolutional encoder. The first type of encoder that we are going to talk about is known as feed forward encoder. So what is a feed forward encoder?

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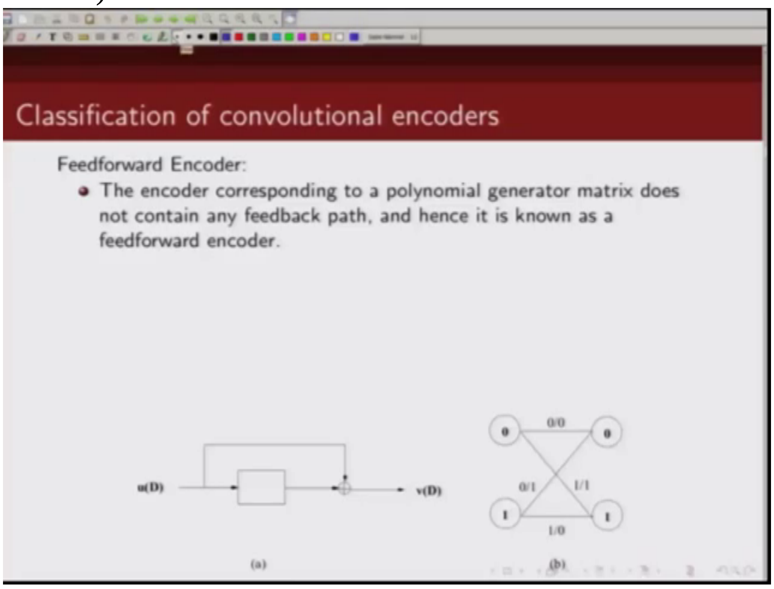

The encoder corresponding to a polynomial generator matrix which does not have any feedback from the output to the input is known as feed forward

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encoder. Let us

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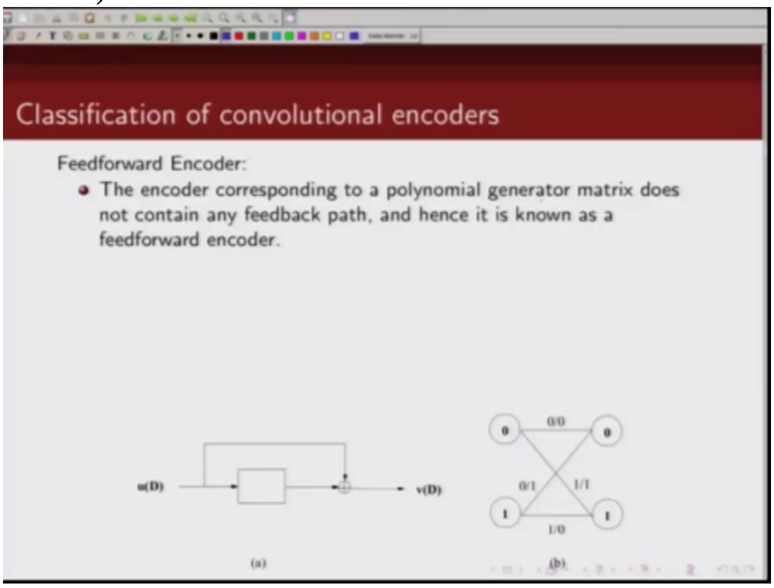

take this example. This is our information sequence. v d denotes our coded sequence. What is the generator matrix G of D, in this case it is given by 1 plus D. Note here

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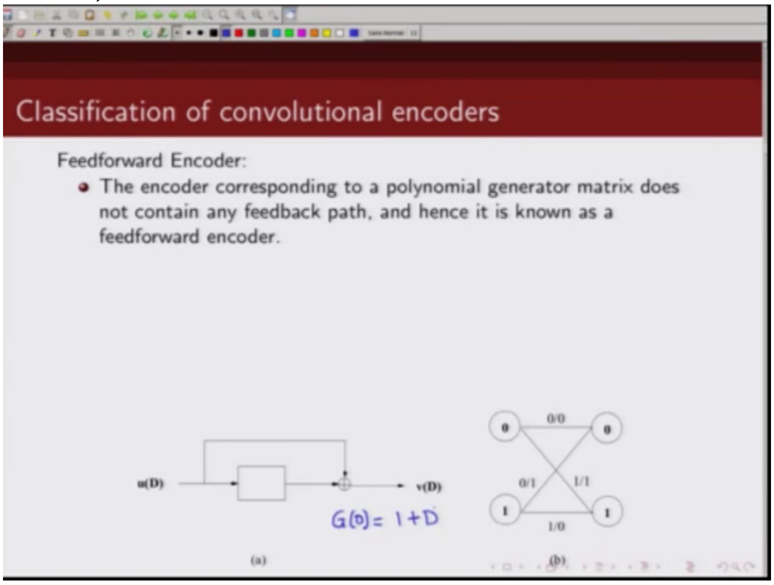

the generator matrix here is a polynomial generator matrix right, as opposed to a rational generator matrix and there is no feedback from the output to the input side. You can see basically the output depends on the current input as well as input one past time instance. So there is no feedback from the output to the encoder side. And this is an example of a feed forward encoder. Now we can

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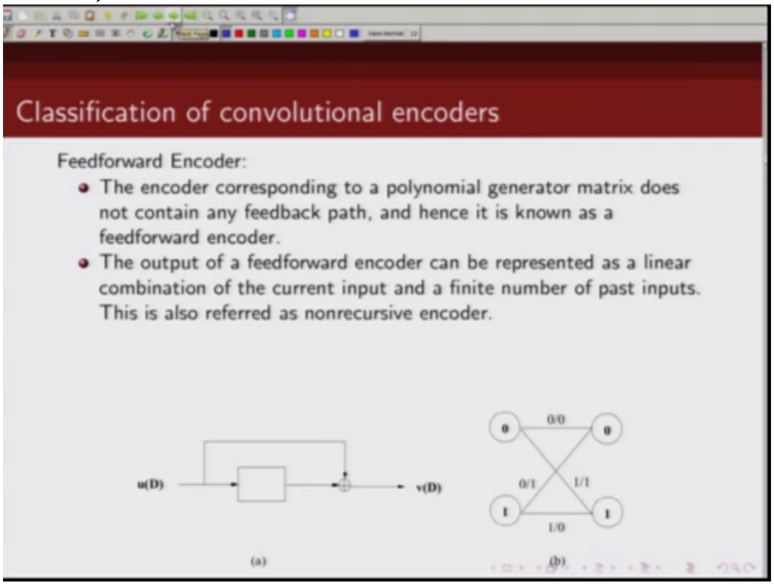

represent the output of feed forward encoder as linear combination of current input and finite number of past inputs. We also refer this type of encoder as non-recursive encoder. And as we said

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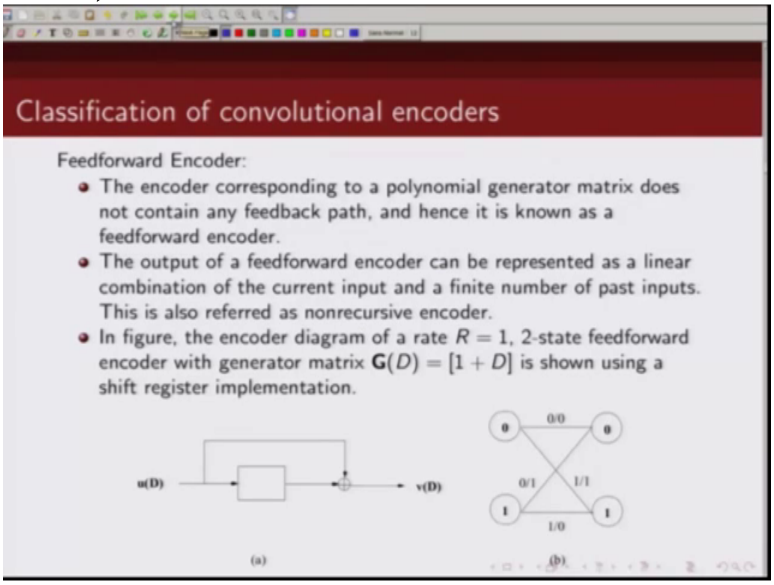

in this we have an example of rate one code, because input one bit, output is one bit coming out and the generator matrix of this rate one code is given by one plus D and you can see this is an example of the feed forward encoder whose generator matrix is a polynomial generator matrix and there is no feedback from the output to the input side. And this is its corresponding state diagram for this feed forward encoder.

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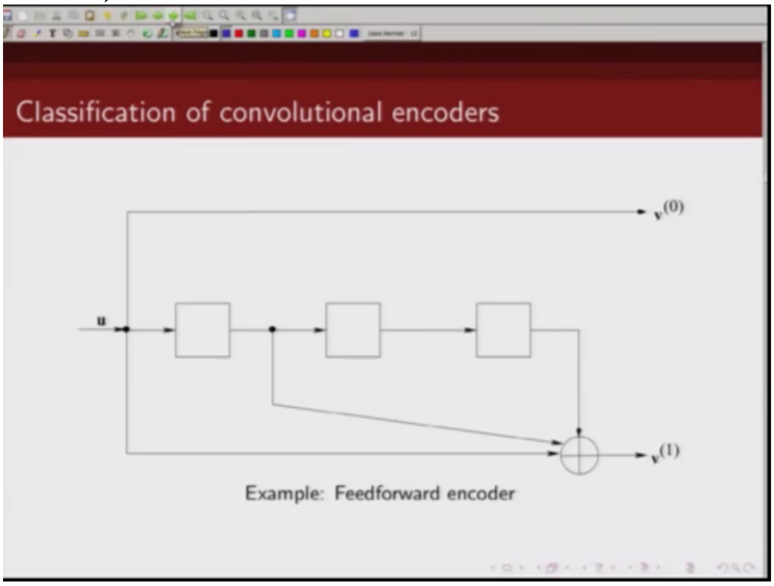

This is another example of feed forward encoder. You can write down the generator matrix of this G of D. v 0 is nothing but input bit so this first one is just 1. And what about the second parity bit? This is information bit so we have 1 plus one delayed version of this information bit plus D cube; this is 1, 2, 3

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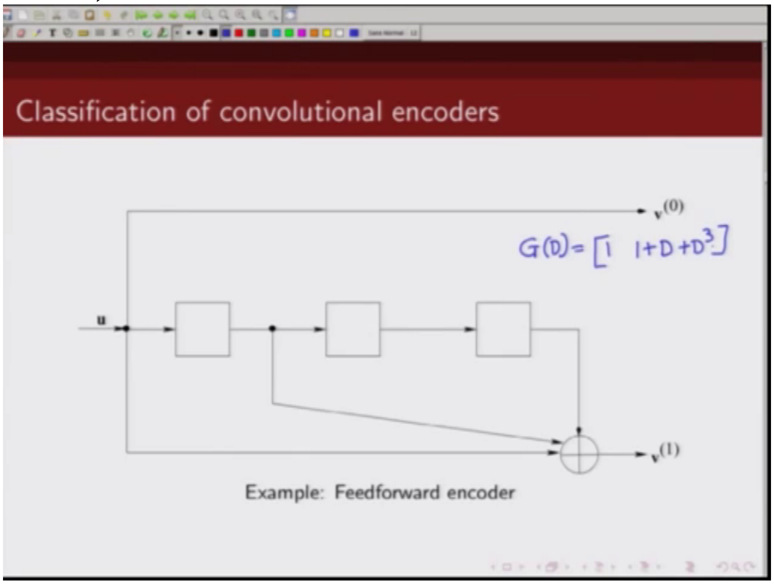

three times instance delayed version of u; so this is a generator matrix, this is also a polynomial generator matrix. There you can see there is no feedback from the output to the input side.

Now let

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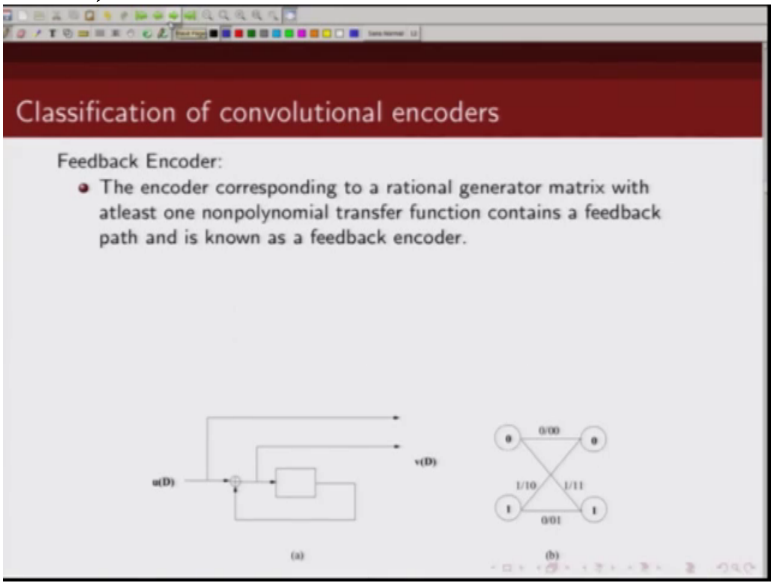

us look at what do we mean by feedback encoder. As opposed to a feed forward encoder, the encoder for a feedback encoder has a rational generator matrix. Please note here we had a

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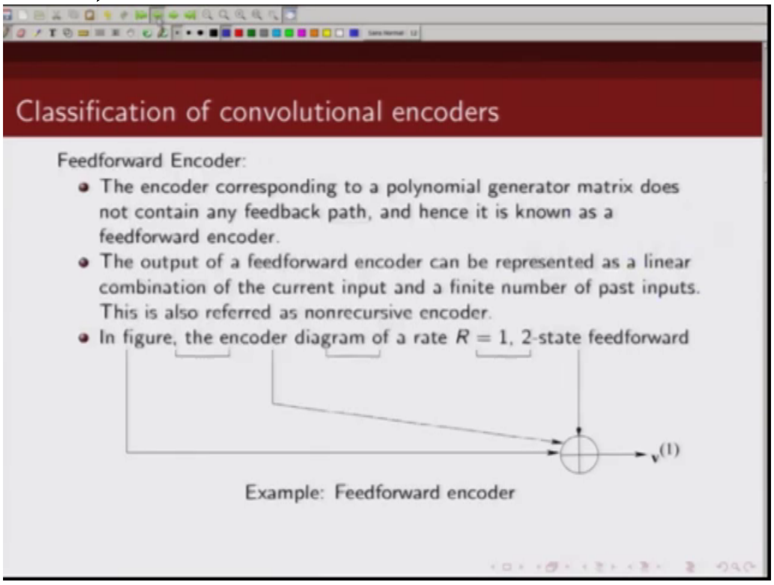

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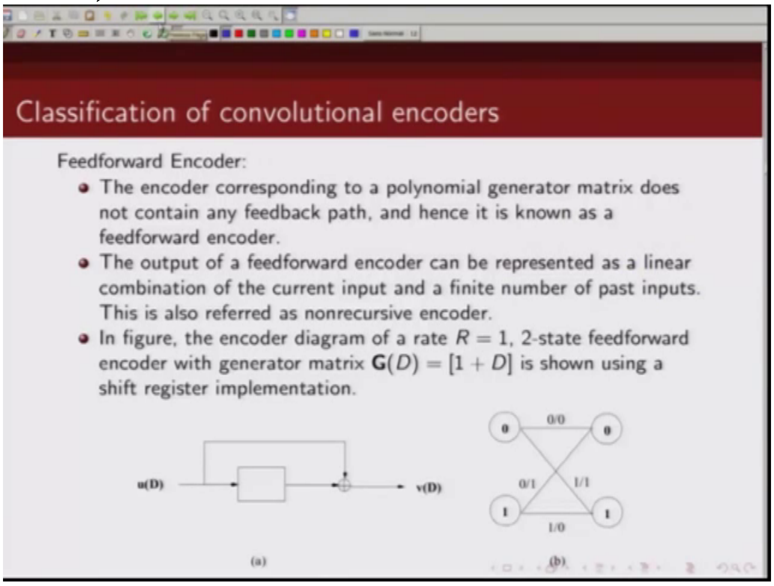

polynomial generator matrix; for a feed forward encoder we had a polynomial generator matrix where as for a

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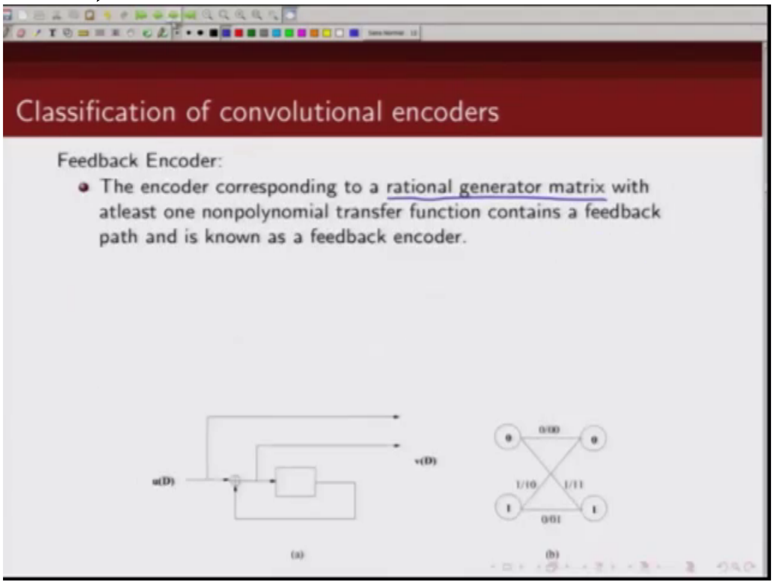

feedback encoder we have a rational generator matrix with at least one non polynomial transfer function containing a feedback path from the output to the input.

Look at this example. From the output we can see the feedback going into the input side. And the generator matrix for this is basically, so first coded bit is nothing but information bit, so that's 1. And this is basically 1, 1 plus D.

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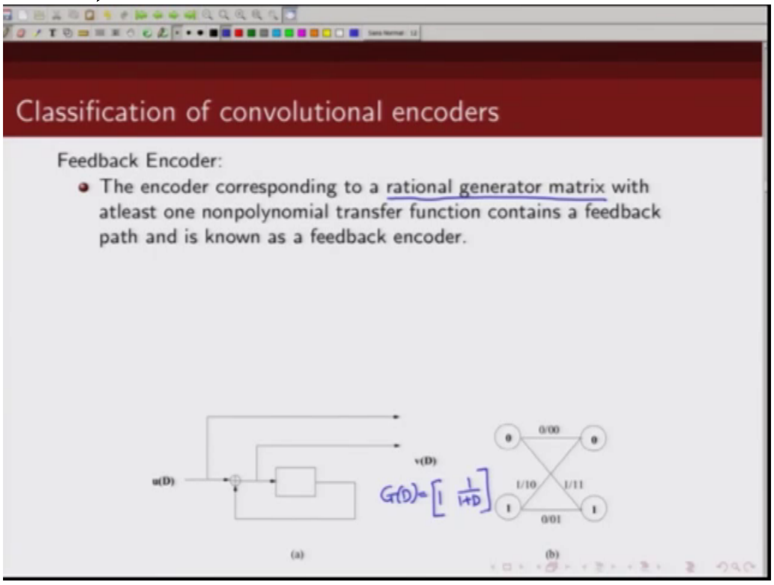

So

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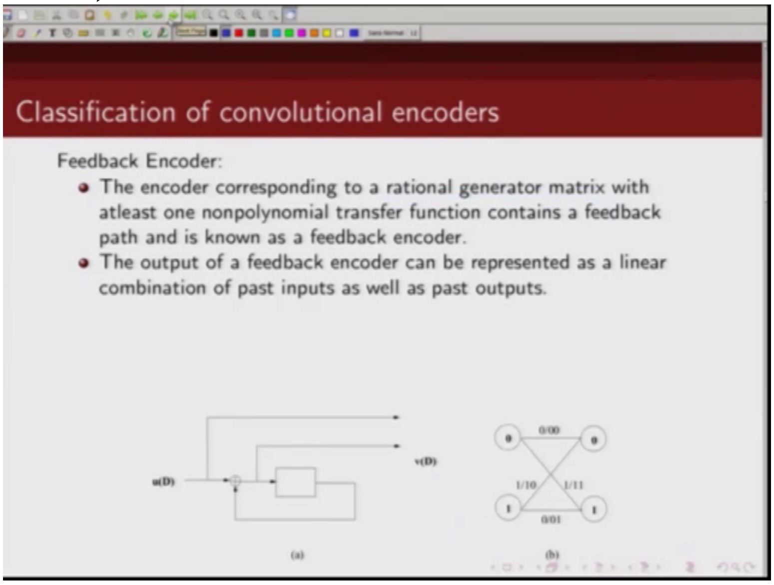

because there is a feedback from the output to the input side, the output of the feedback encoder can be written as a combination of past input as well as past output.

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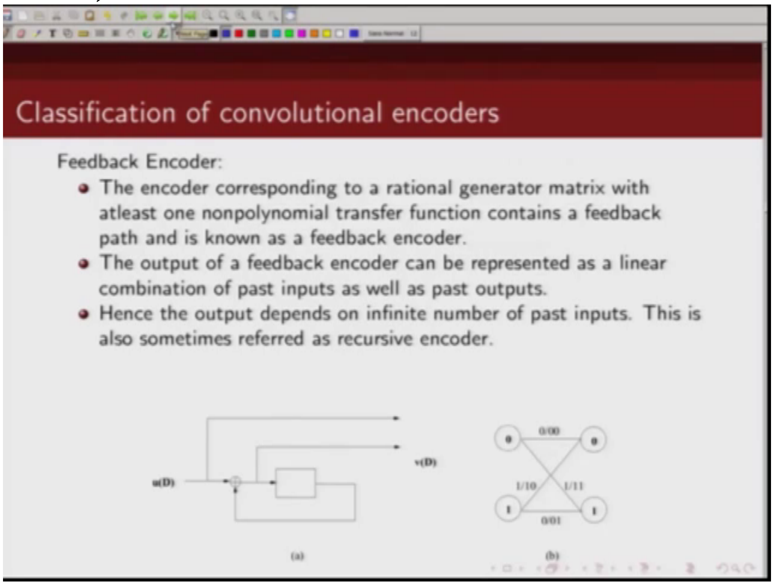

Hence the output depends on infinite number of past input because the current output depends also on past output and past output also depends on past input and past output. So the output will basically depend upon infinite number of past inputs. Now feedback encoder is also known as recursive encoder. And we just now mentioned one example

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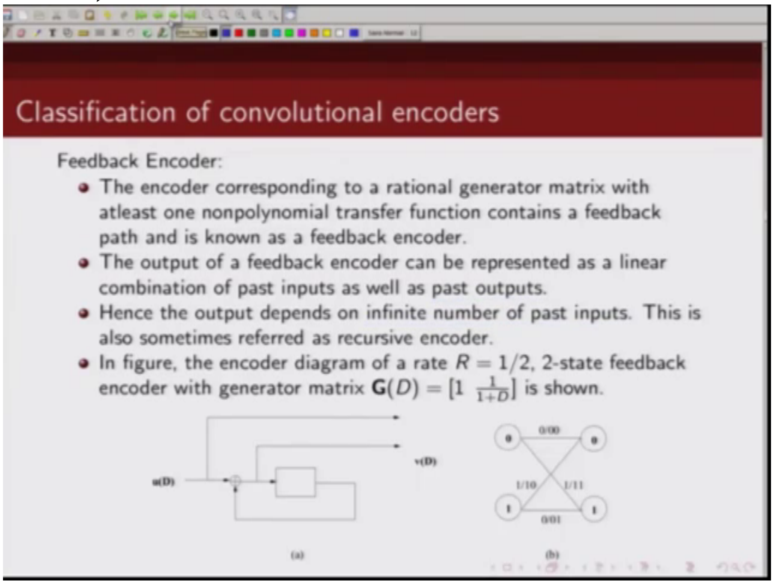

of this feedback encoder is given in this (()). This is a rate one half code. You can see for 1 input we have 2 outputs and its generator matrix is given by this. This is its corresponding state diagram for this feedback encoder. This is another example

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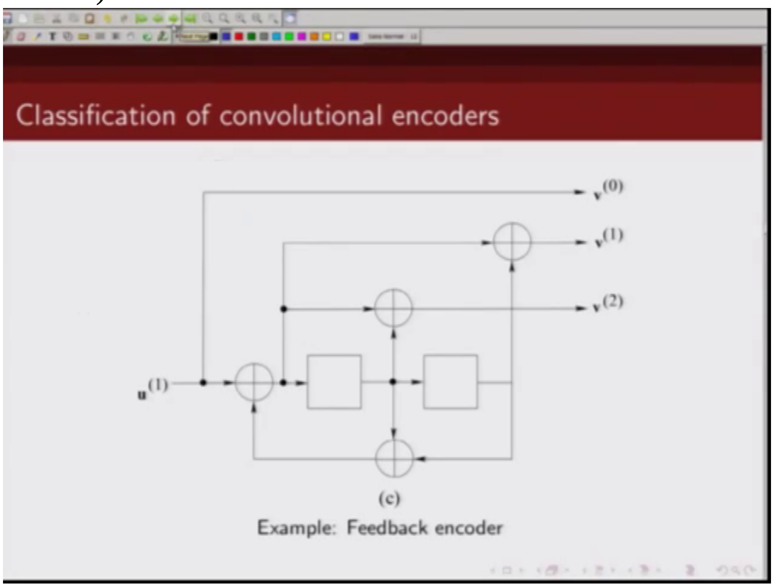

of a feedback encoder. So there is 1 input and there are 3 outputs. We can write the generator matrix G D, the first output is nothing but information bits that's 1. Now what are the feed forward terms in v 1? So v 1 depends on this bit and this bit. So this is 1 plus D square and what's the denominator term, we have basically 1 plus D plus D square term. Similarly v 2 is basically given by 1 plus D and this is 1 plus D plus D square. So this is a generator matrix

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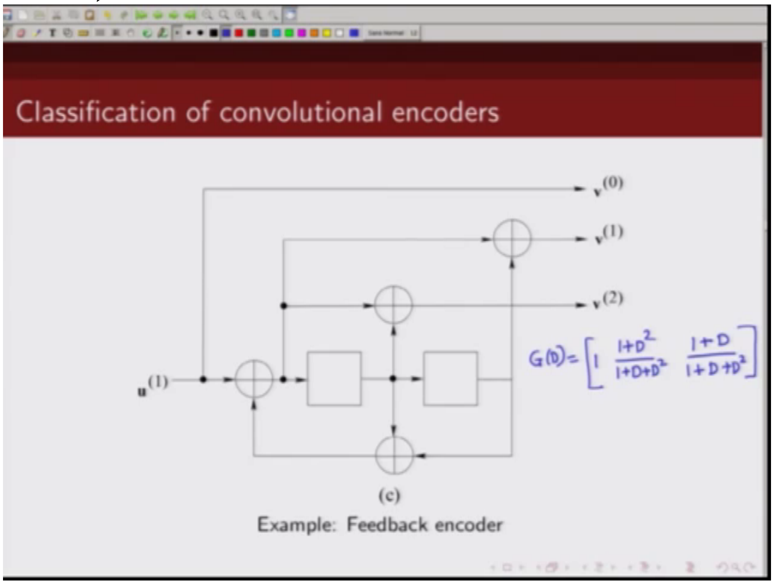

for this feedback encoder.

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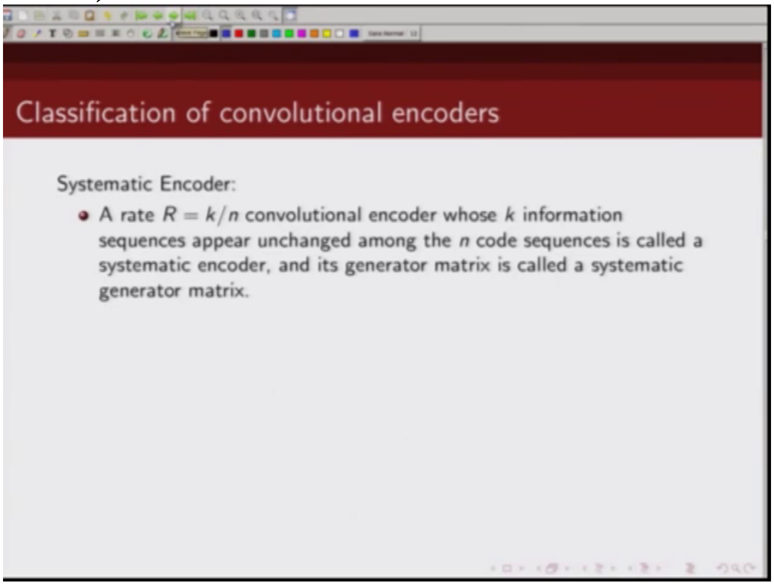

The next classification that we are going to talk about is based

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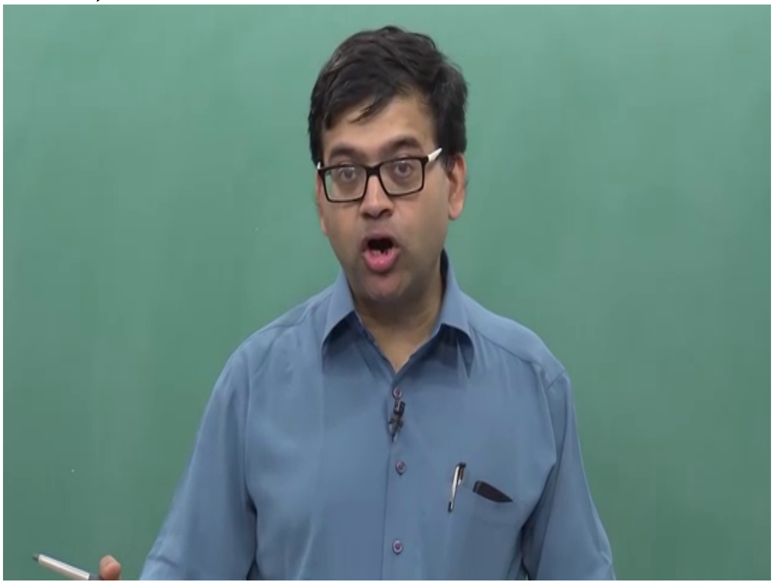

on output bits, whether we can separate out information bits from the coded bits. So in a systematic encoder;

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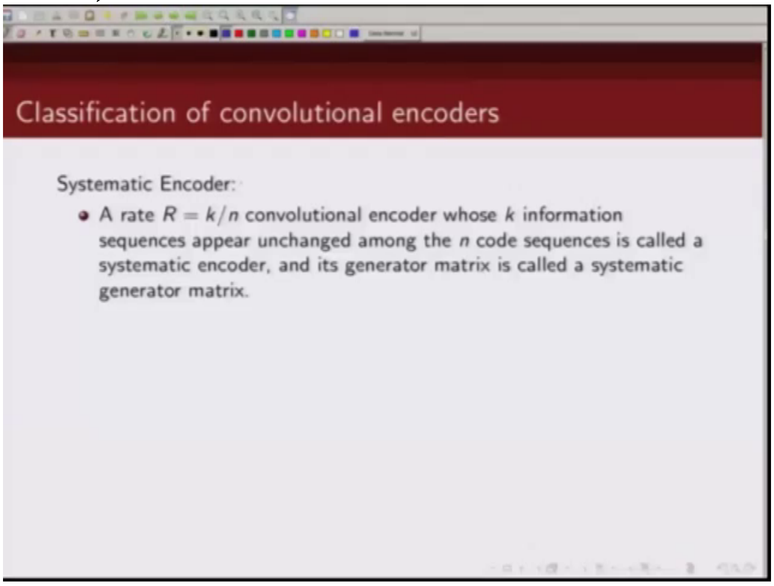

a rate k by n systematic encoder the k information bits appear unchanged in the output. So out of those n coded bits

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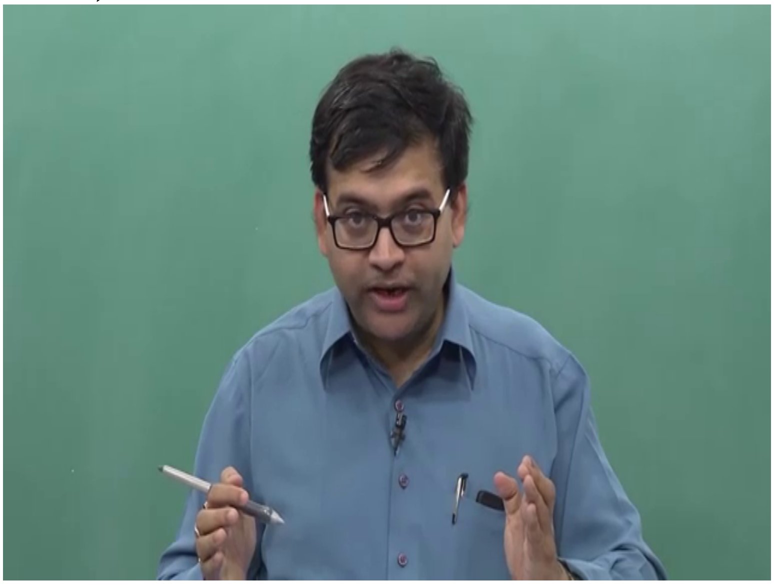

you can directly see the k information bits and rest n minus k bits are your parity bits.

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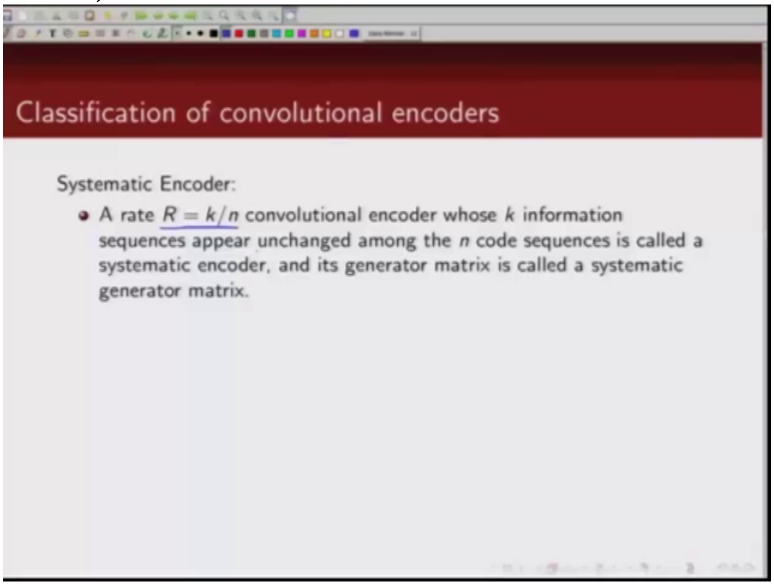

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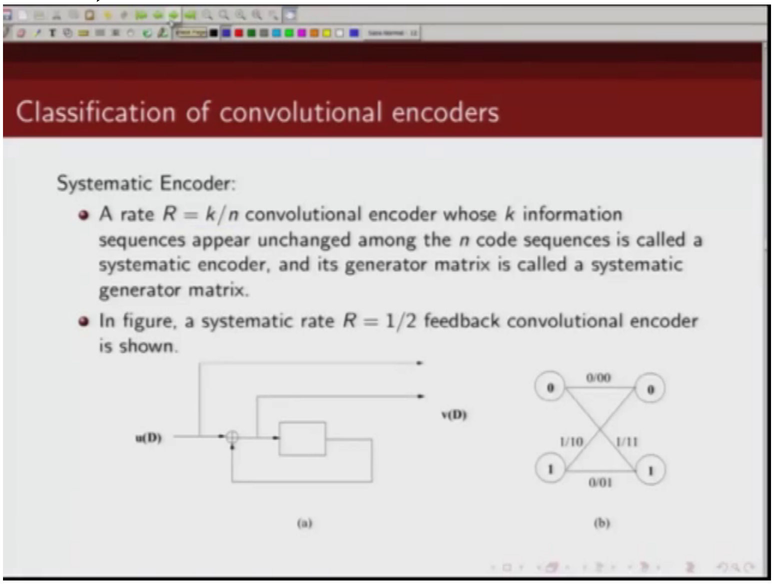

And the generator matrix corresponding to a systematic encoder is known as systematic generator matrix. Take example of this rate one half feedback encoder. You can see there is one input and there are two outputs. So it's rate one half. And it is a feedback encoder. There is a feedback from the output to the input side. You can see here the first coded bit is nothing but the information bit and the second coded bit is parity bit basically coming out from this convolutional encoder. So from these two coded bits, we can easily find out what the information bit was from this bit. So we can separate out the information bit from the coded bit. And this is example of a systematic encoder.

As opposed

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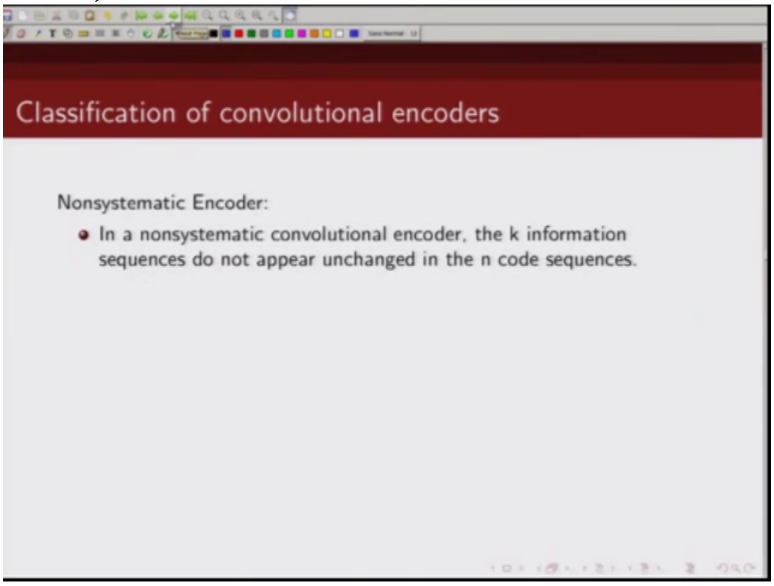

to a systematic encoder, in

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a non-systematic encoder

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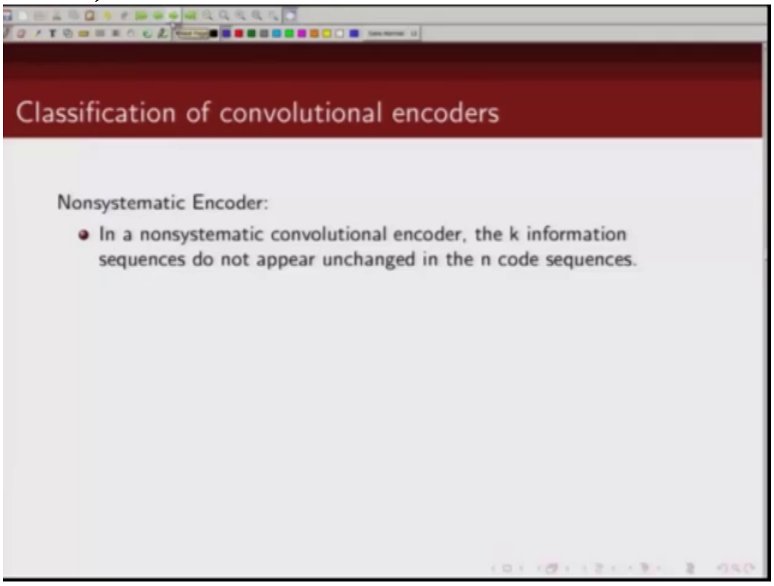

we cannot separate out the k information bits from the n coded bits. This is an example

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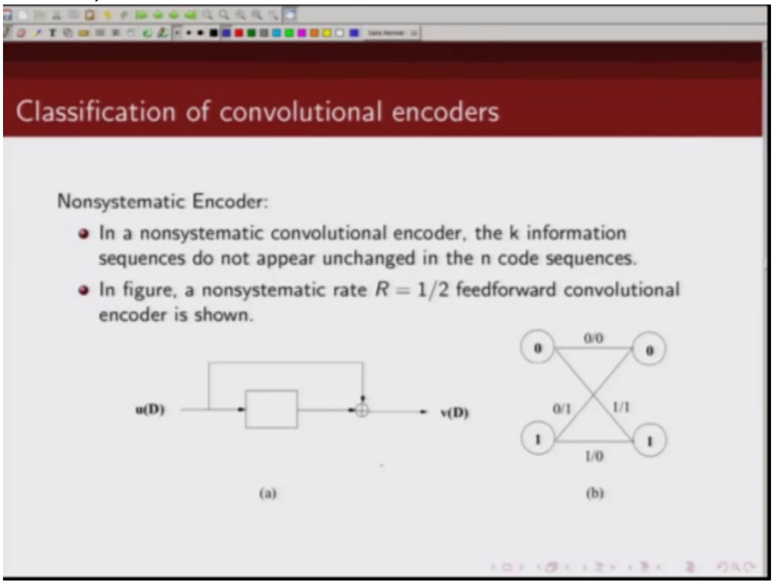

of a, one second I want to make it rate one, this is actually rate, this is a typo, this is rate 1 code

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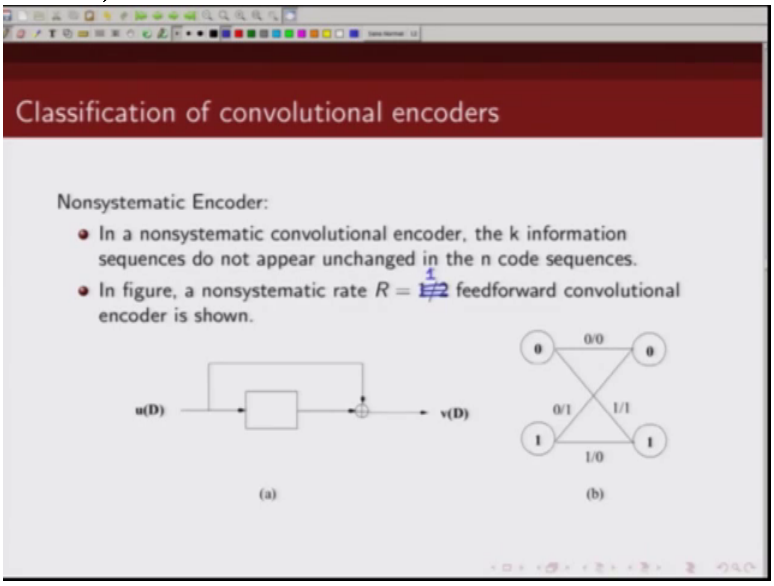

because there is 1 input and there is 1 output this is the rate 1 and this is the feedback, feed forward encoder you can see there is no feedback from the output to the input side; so it is rate 1 feed forward encoder and you can see the output bit

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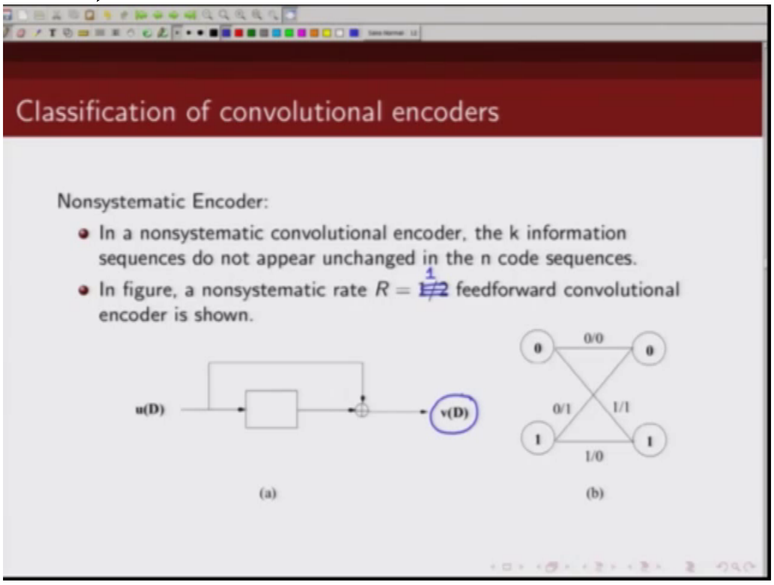

is given by this current input bit and this past input bit. So you cannot directly take out the information bits from this coded bit. So this is an example of a non systematic encoder. We could also define

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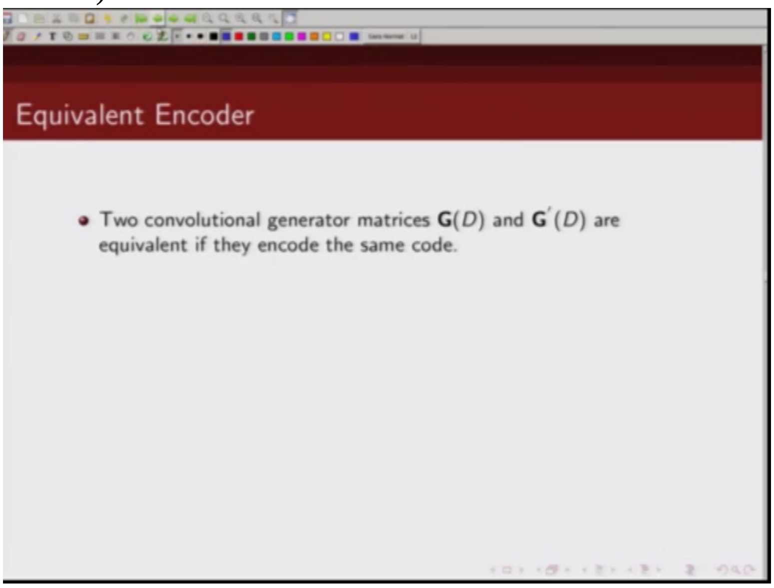

a class

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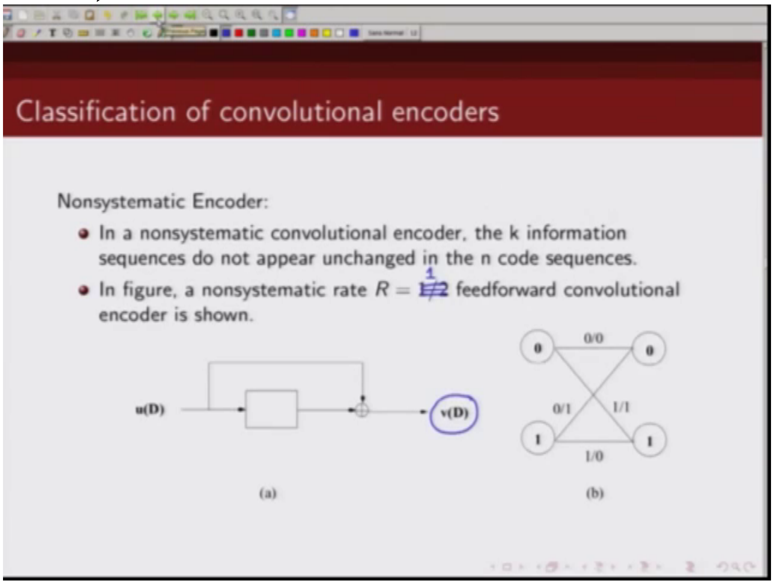

which is called

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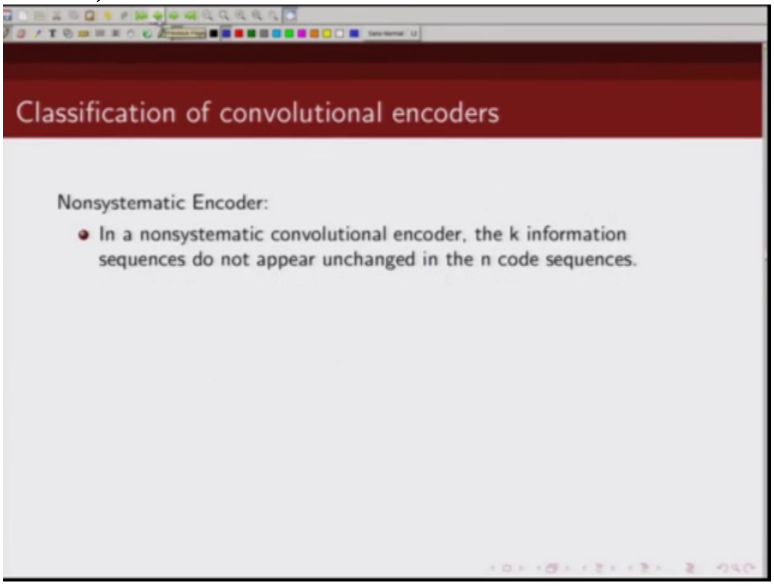

partially systematic

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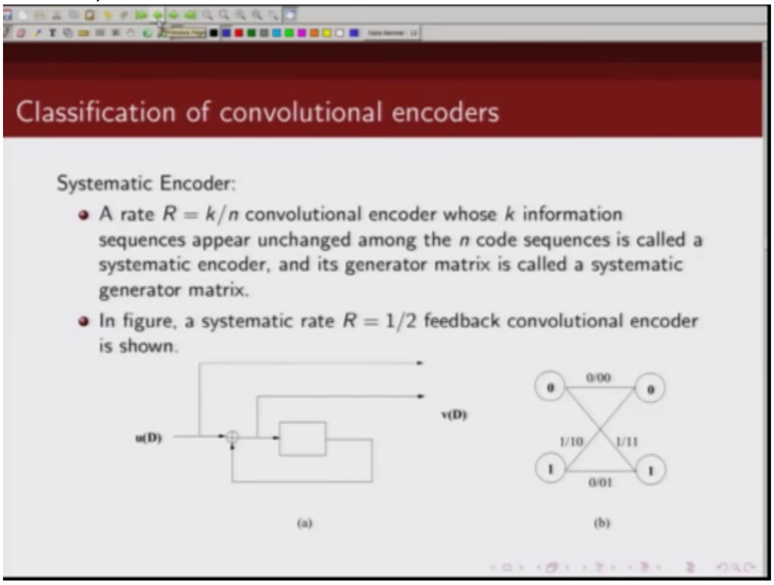

encoder. In a partially systematic encoder,

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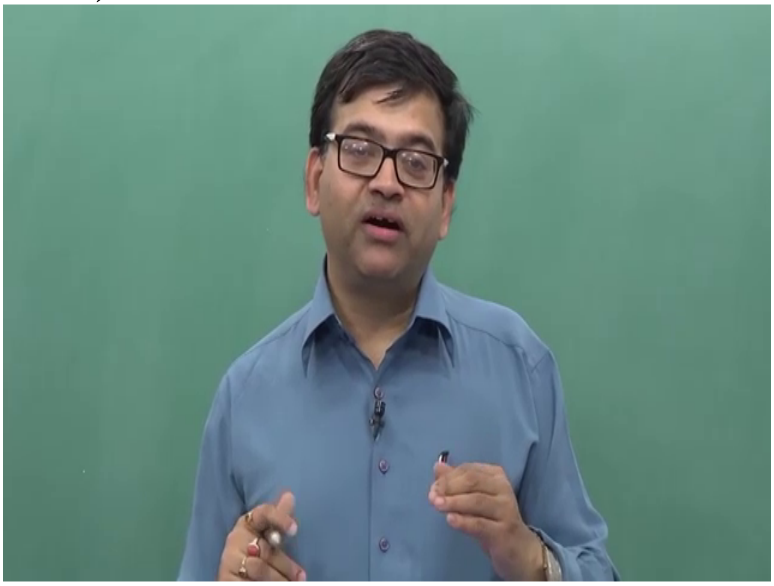

so if you have a rate k by n partially systematic encoder, out of those k information bits some of them appear unchanged in the output while some of the information bits do not appear unchanged in the coded bit. So in a systematic rate k by n encoder we can see directly the k information bits. In a partially systematic encoder we can see a fraction of these k information bits, may be a few bits like 1 to k minus 1 and in a non systematic encoder we cannot see any systematic bit direct, any information bit directly in the output. So all

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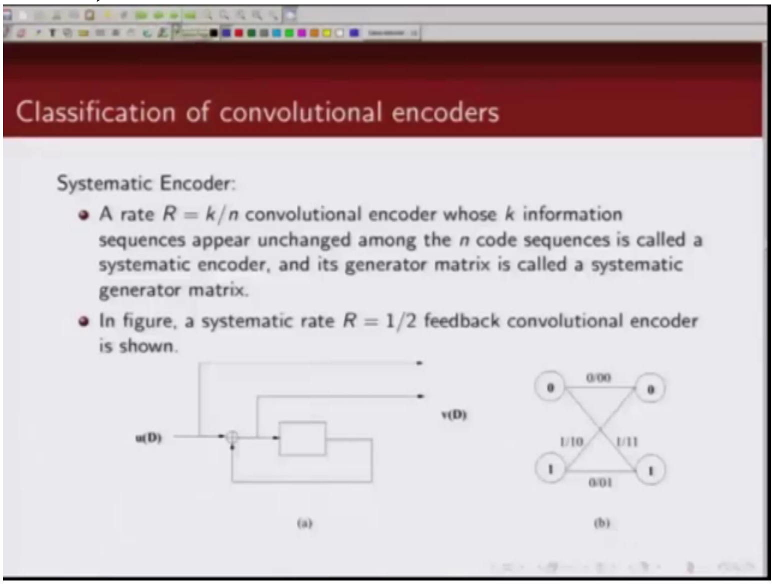

the parity bits are essentially linear combinations of current and past inputs and outputs. Now

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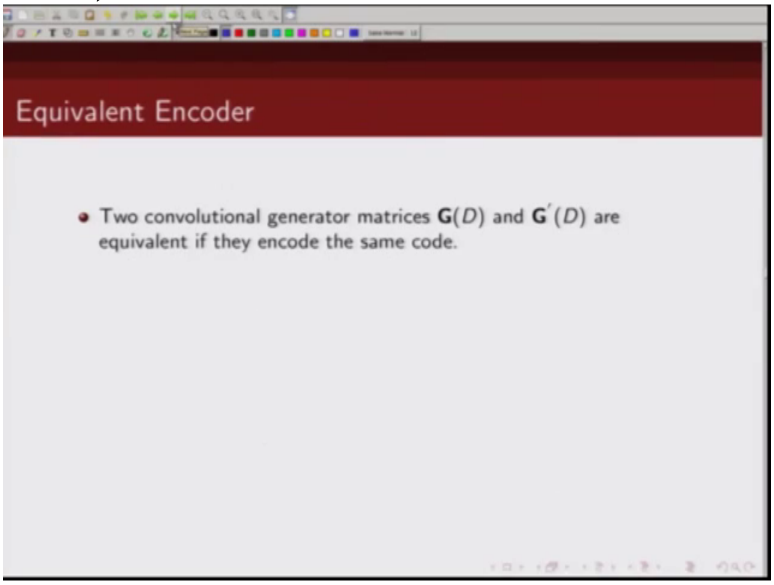

that brings us to our next

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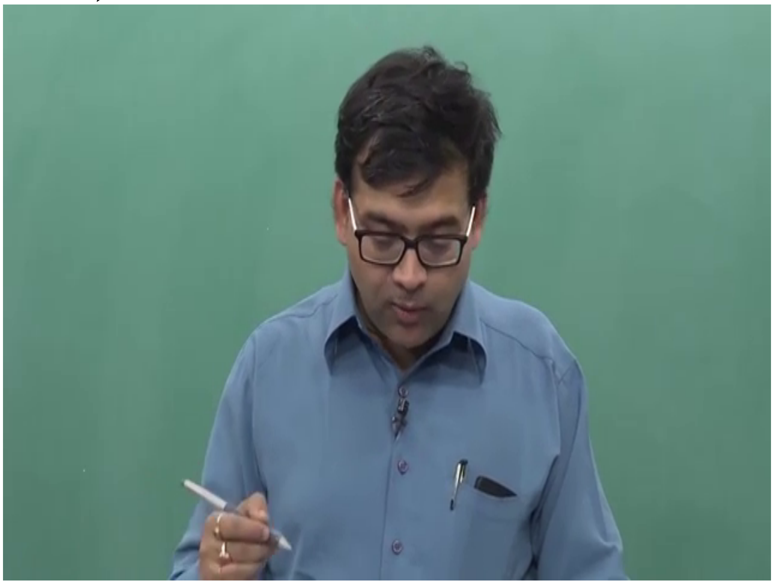

topic of discussion which is concept of equivalent encoders. So before we define

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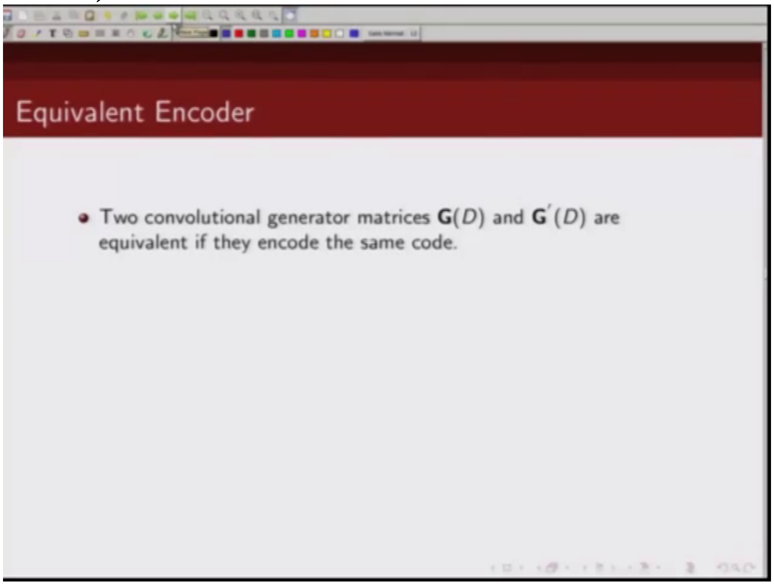

what is an equivalent encoder, we will define what do we mean by equivalent generator matrix. So we, two convolutional matrix let us call it G D and G prime D are equivalent if they encode the same code. Now what do we mean by encode the same code? So the set of codewords generated by this and this, if they are same, then these generator matrix are equivalent. Now the set of codewords generated by these generator matrix are same but the mapping between the input and the output is different in this encoder from what the mapping between inputs and output

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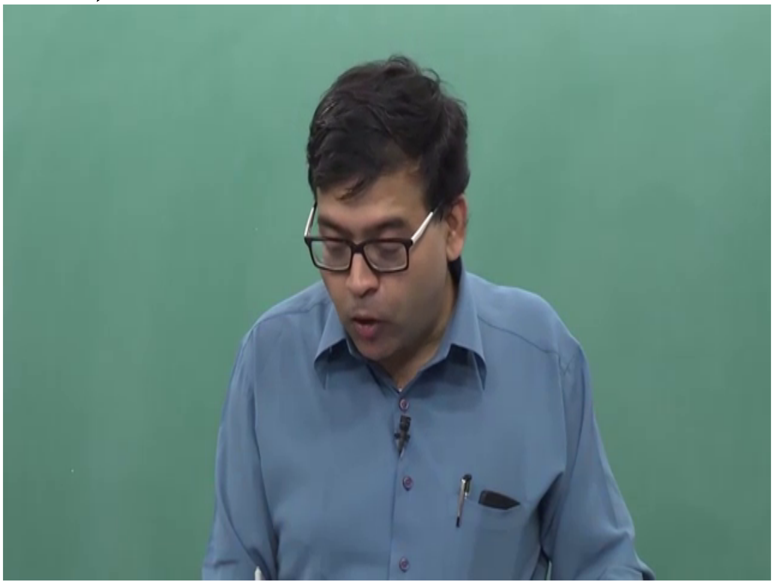

is for this generator matrix.

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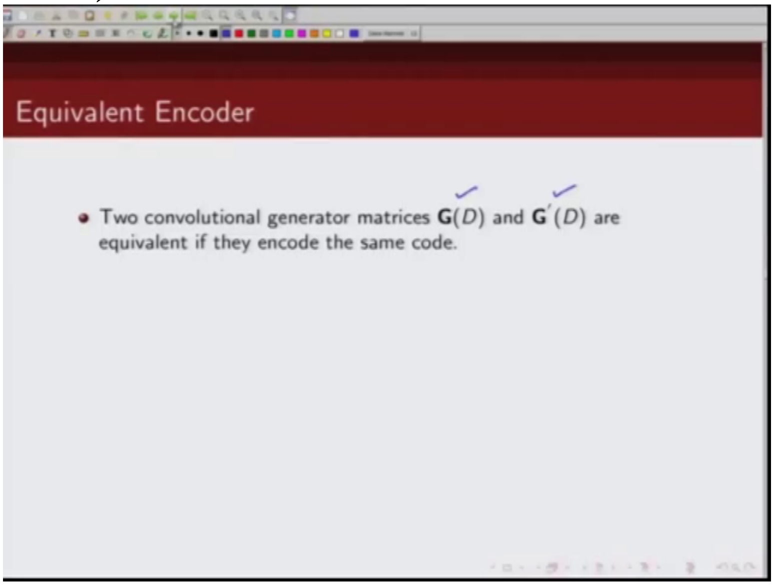

Now we say

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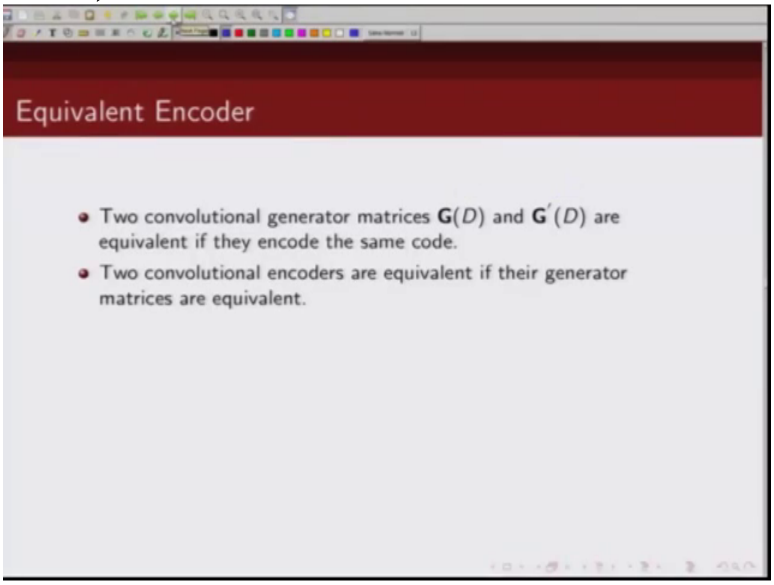

two convolutional encoders are equivalent if their generator matrix are also equivalent. In other words if their generator matrix encode the same

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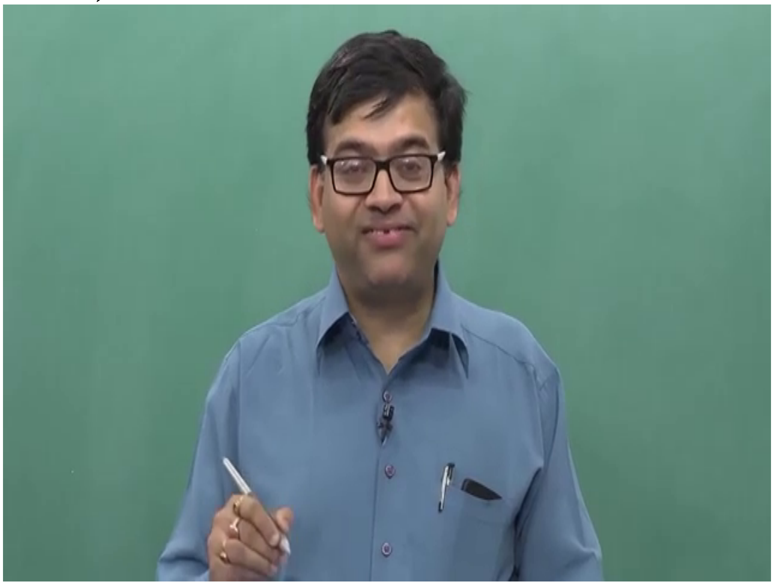

code then we say 2 convolutional encoders are equivalent. So if

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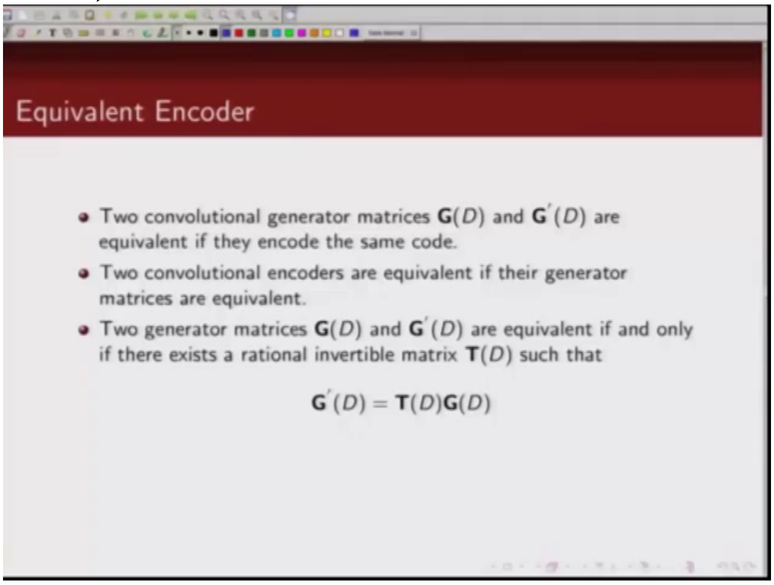

G D and G prime D are equivalent then this condition should hold. So two generator matrixes are equivalent if and only if there exists a rational invertible matrix T of D such that we can obtain G dash G by T D multiplied by G D, Ok and we can see basically so let's say set of codewords generated by G dash D. So that would be v D, u D times G dash D. Now this we can write

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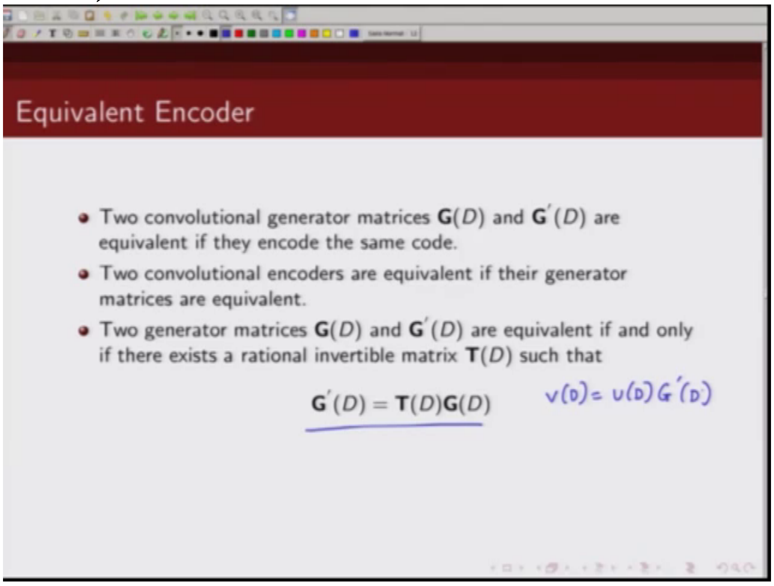

as u D T D times G of D and let us call

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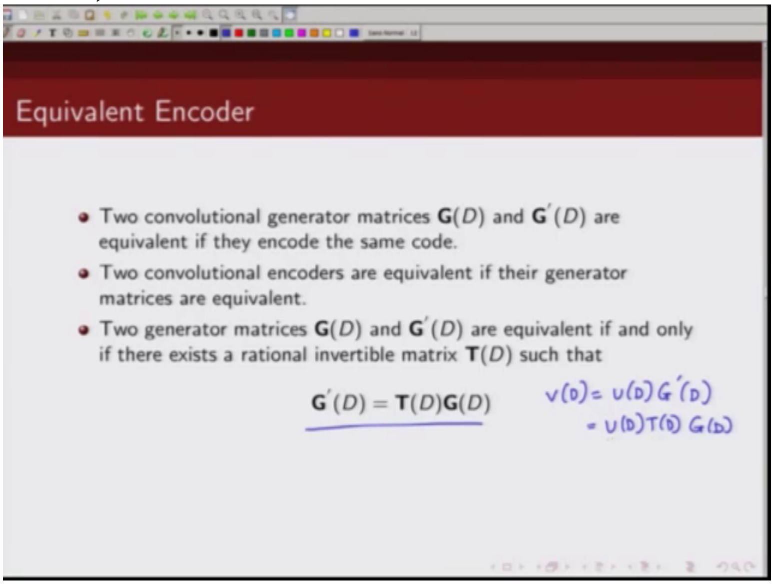

u D T D as u dash D G D,

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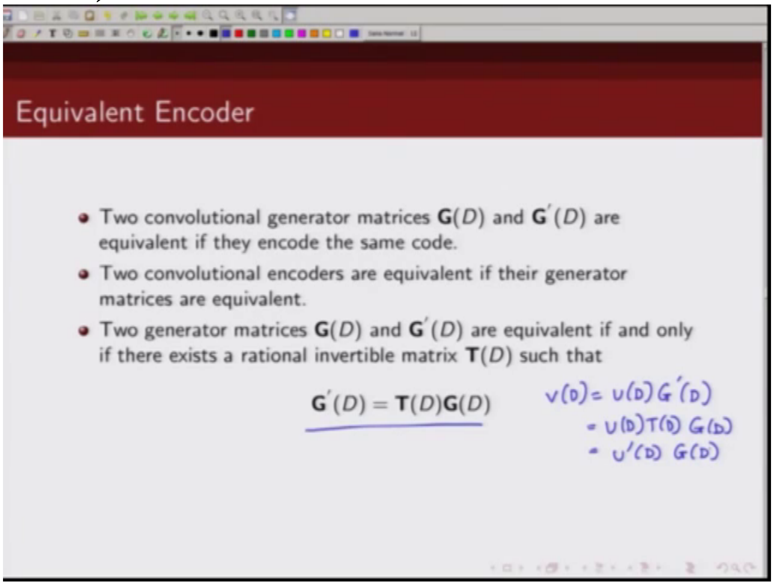

Ok.

So let us take

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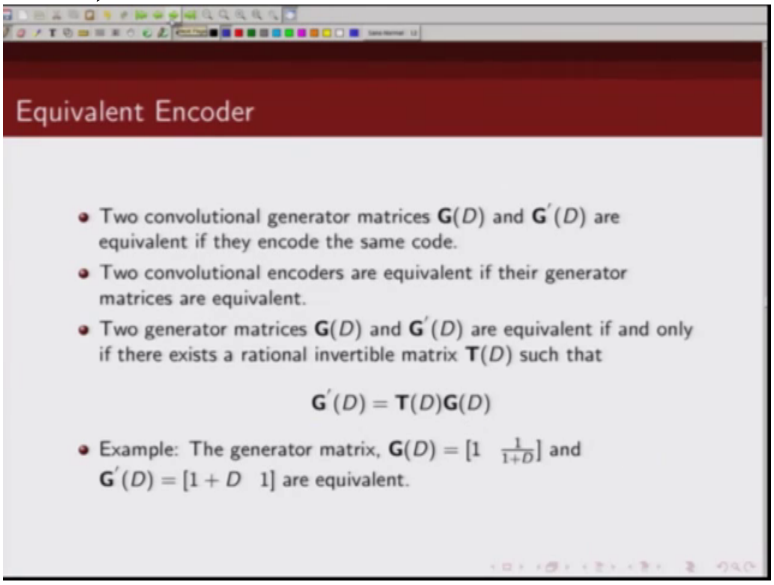

an example. This G d 1, 1 plus 1 by 1 plus D, and G dash D which is 1 plus D 1, these are equivalent encoders because we can write G dash of D as 1 plus D

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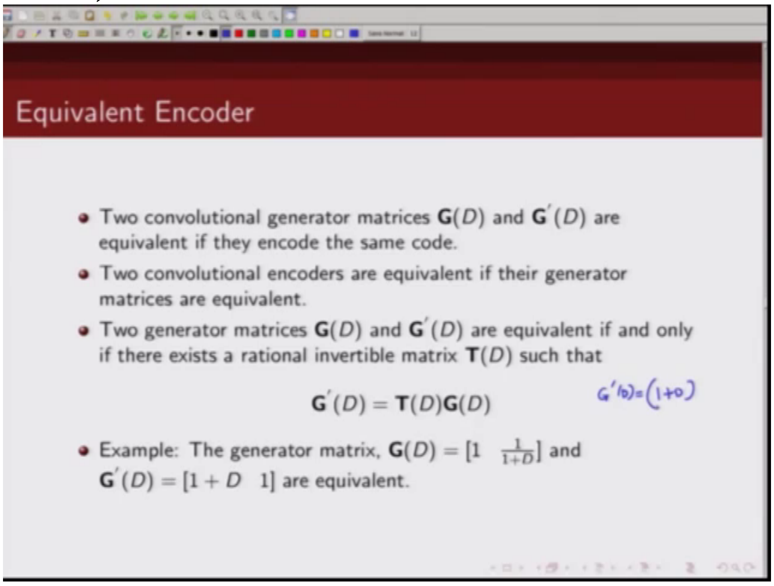

times G of D, Ok. And so for, and we can see this is a systematic encoder, generator matrix for a systematic encoder, Ok. Now for,

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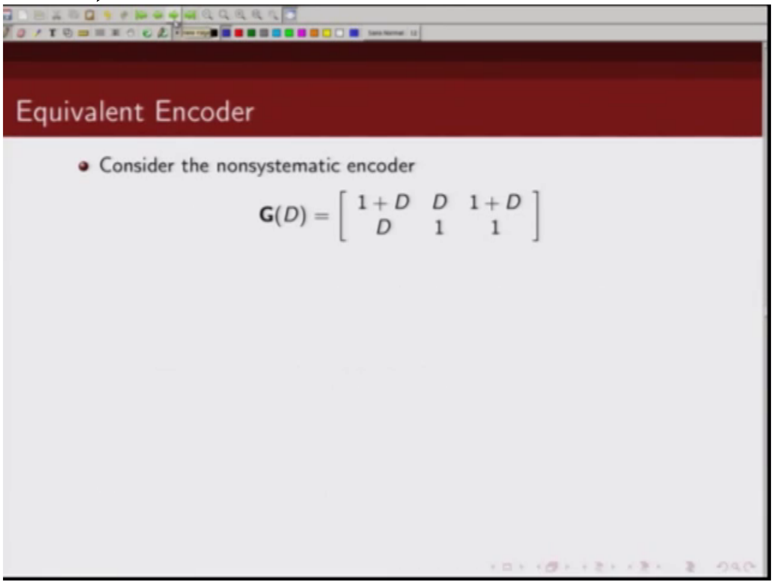

and this is

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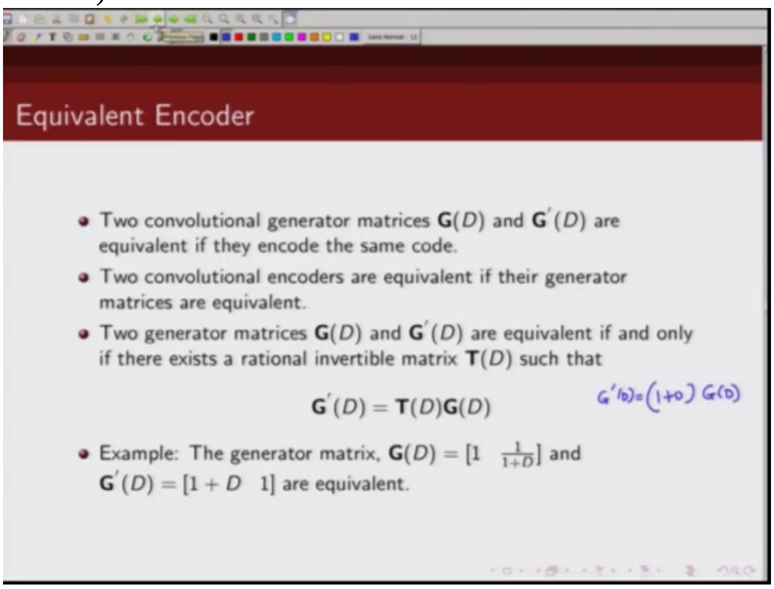

a feedback encoder, this is a feed forward encoder.

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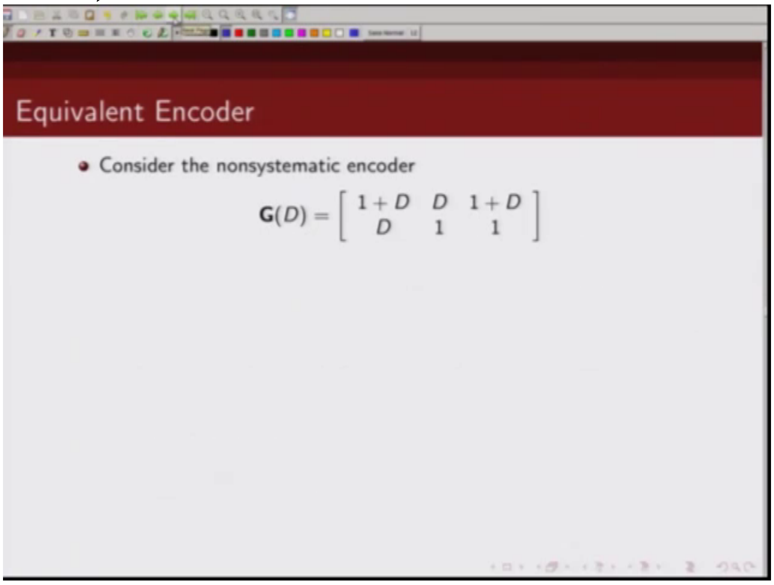

So let us take an example of a non-systematic feed forward encoder and let's try to find its equivalent systematic encoder. So what would be the equivalent systematic encoder corresponding to this non systematic encoder? The generator matrix G dash of D should be of the form identity and some matrix P.

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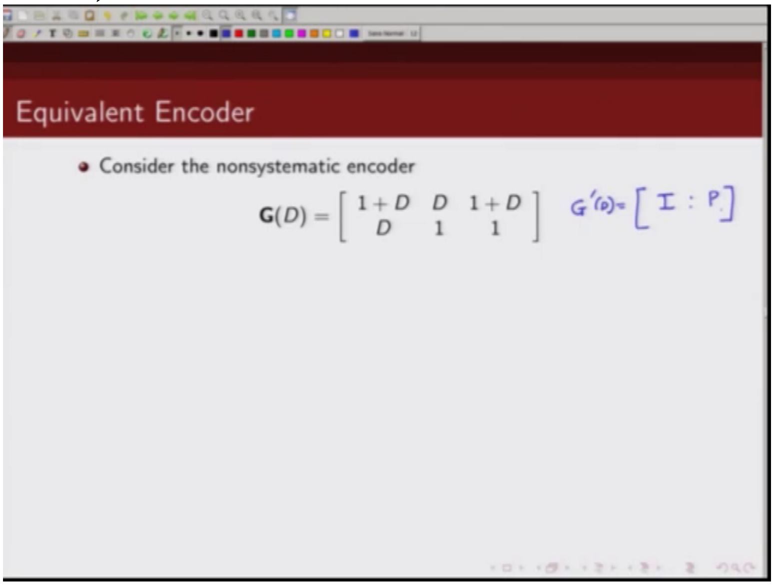

So what we want is basically we want this to be the form 1 0 something here 0 1 something here. So we want to convert this

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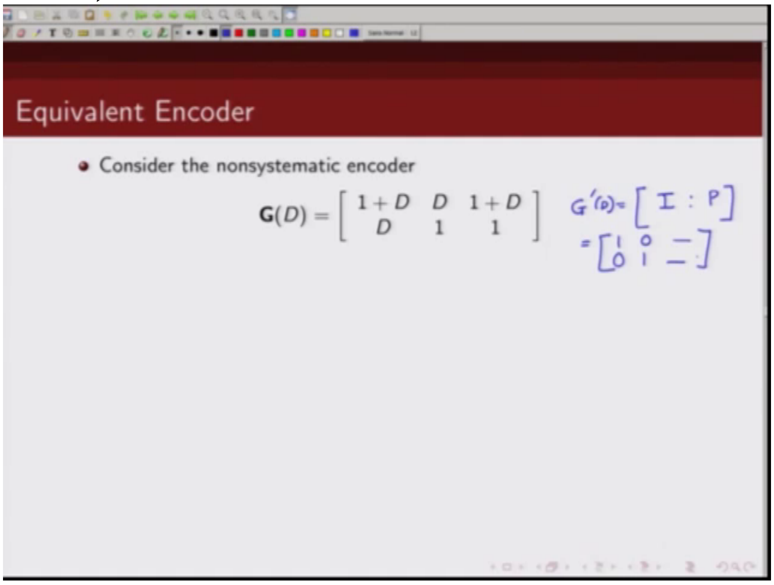

into a form of this type. Ok, so we will do elementary row operation to bring this generator matrix into a generator matrix of this form. So first,

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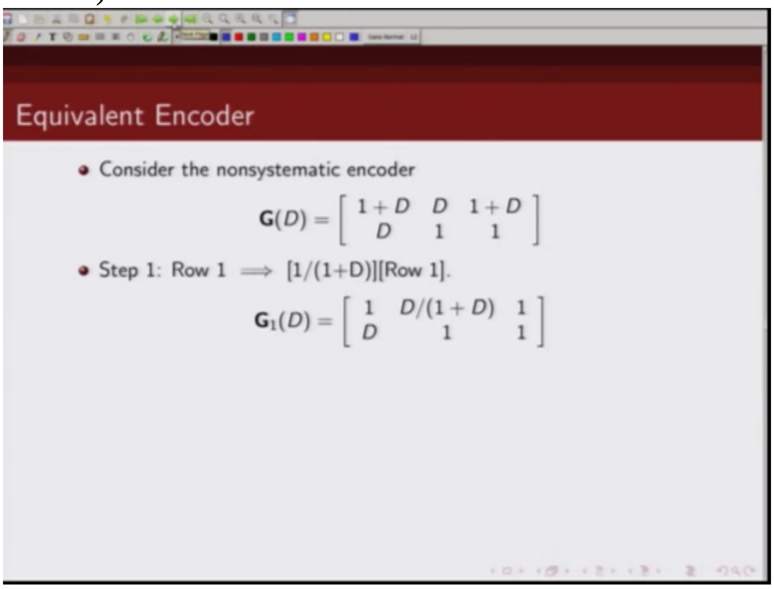

so we will do this transformation row 1, we will try to make this as 1. How can we make this as 1? If we multiply row by 1 by 1 plus D. If we do that, this term will become 1, this term will become D by 1 by D and this term will become 1. We leave the second row unchanged. Next, we want to get a

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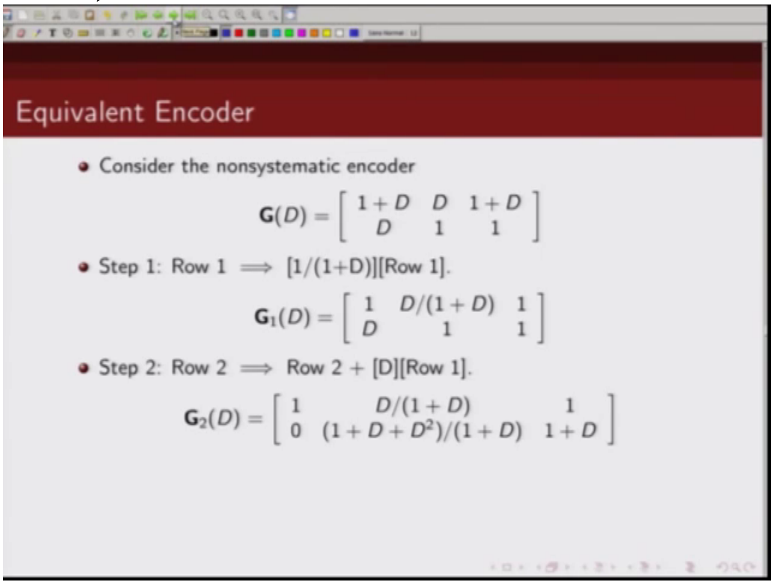

zero here, right? How do we get a zero here? We do this transformation row 2; we will make it row 2 plus D times row 1. So the first row is unchanged but second row we do this transformation. It is row 2 plus D times row 1. So row 2 here is D plus D times row 1, which is another D. So D plus D is zero. Similarly row 2, this 1 plus D square plus 1 plus D, this is basically given by this and we have 1 plus D which is this term. So what we have done is we have converted this into form 1 0. Next we want to get a 1 here, right? We want to get the 1 here. How can we get a 1 here? We will do this following transformation.

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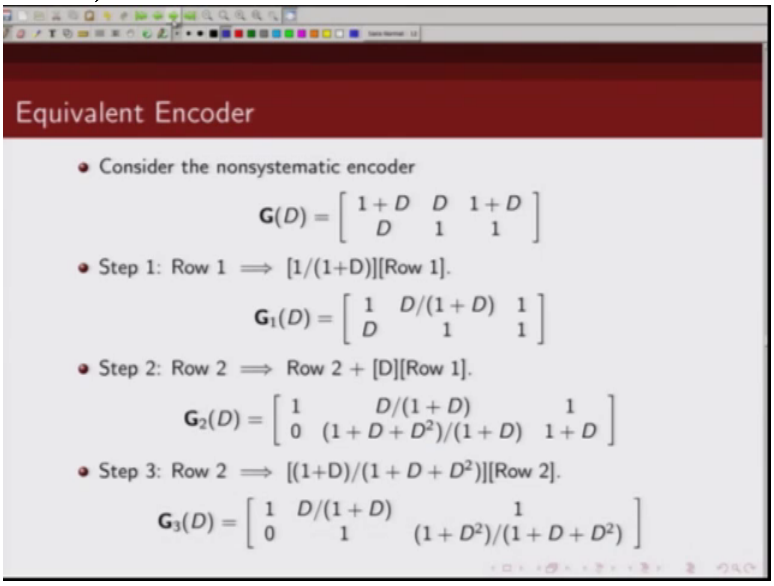

For row 2, we will multiply row 2 by 1 plus D divided by 1 plus D plus D square. If we do that then this will become 1. So we leave the first row unchanged. Here 0, if we multiply by this, it does not change. If we multiply this by this we get a 1 here and here we get this term.

So now we have got, so far is we got a 1 here, we got a 0 here, we got a 1 here, now what else is remaining? We have to make this a, we have to make this a identity

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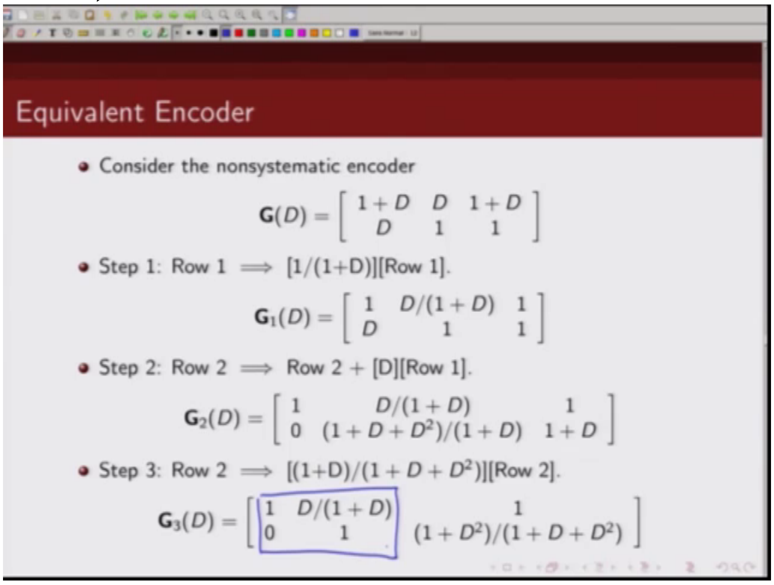

matrix. So we have to make this a zero. How can we make this a zero? We multiply this by this and add it up to the first row. We can make it a zero. So next,

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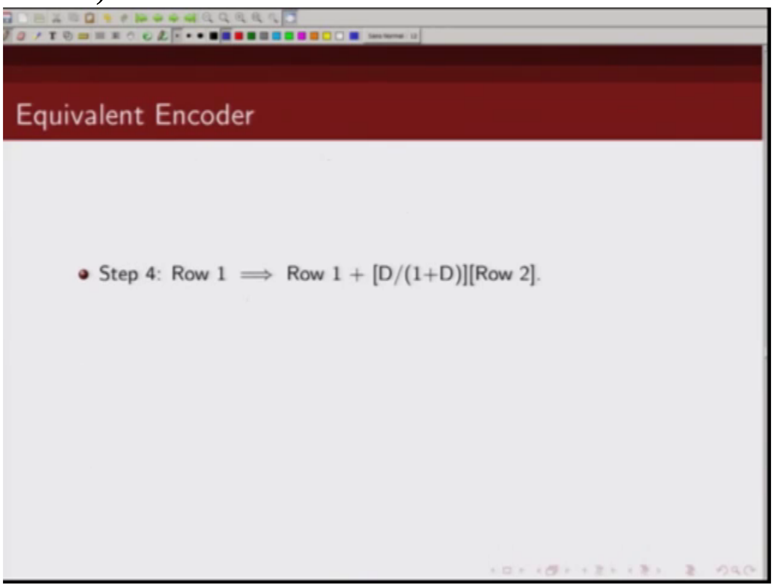

row 1 we add D times 1, 1 plus D times row 2. If we do that

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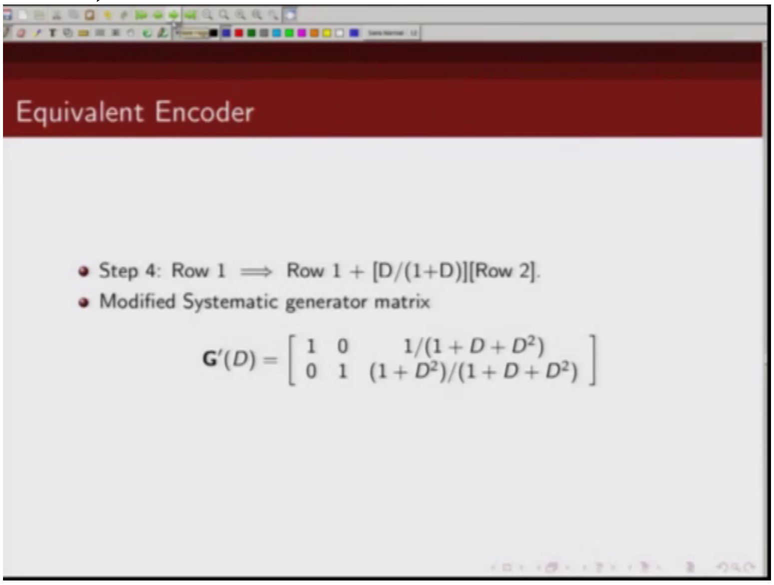

the modified generator matrix that we get is this. Note now this is generator matrix for a systematic encoder. You have your identity matrix here. And you have some matrix

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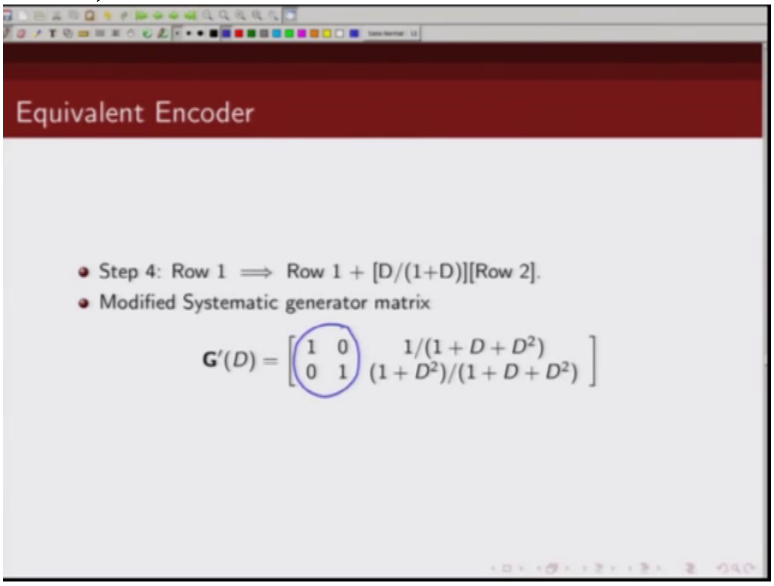

here which is your P matrix.

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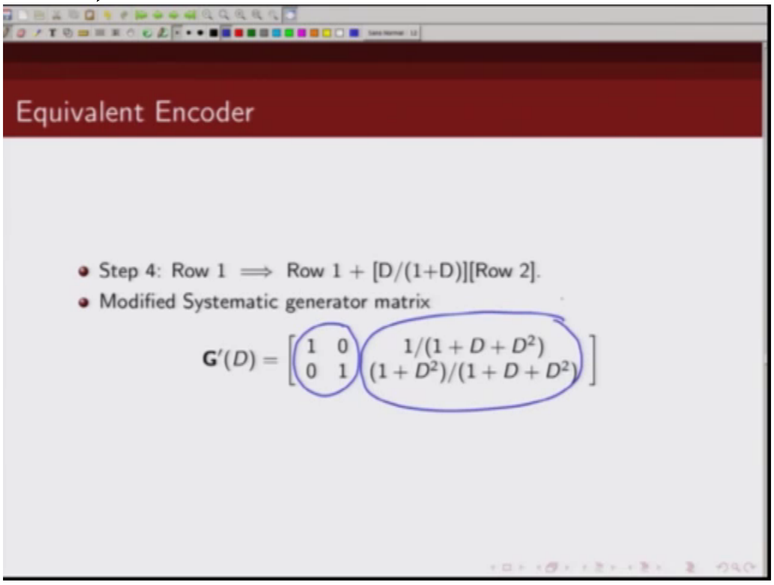

So this is basically

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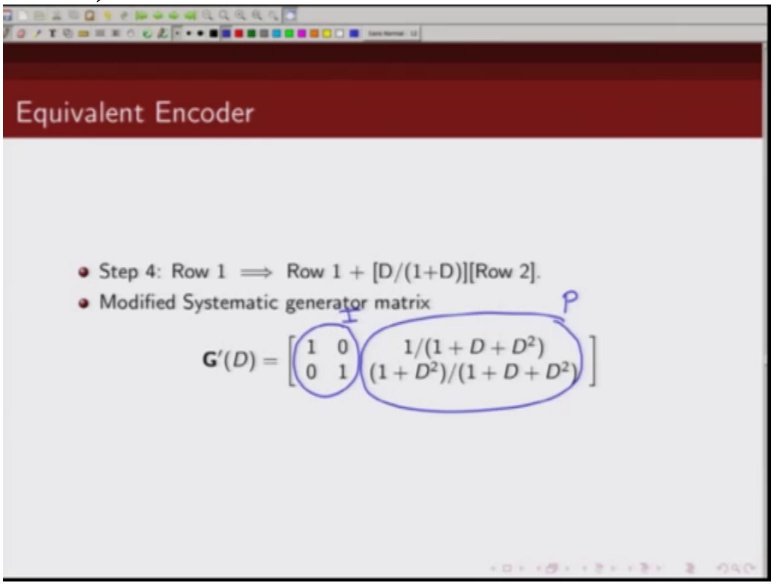

the generator matrix for systematic encoder. So note now by

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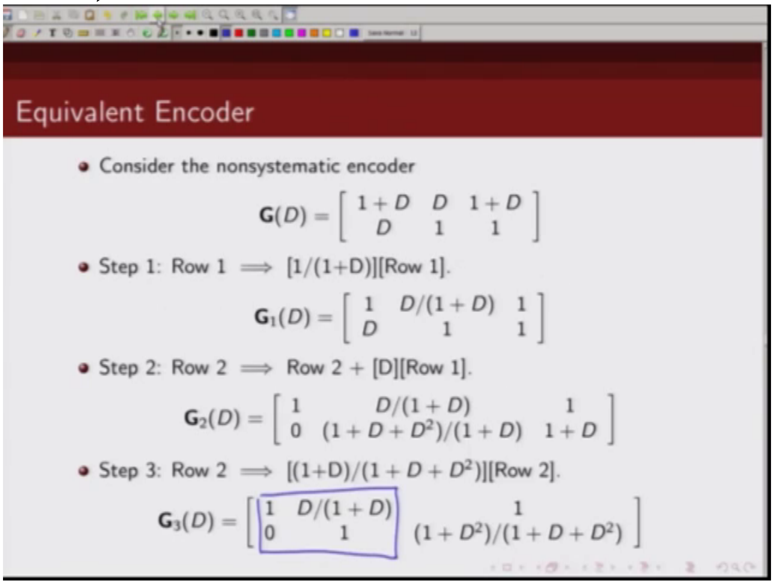

simple row operations we were able to get an equivalent systematic generator matrix for a non-systematic encoder whose generator matrix is given by this.

Next

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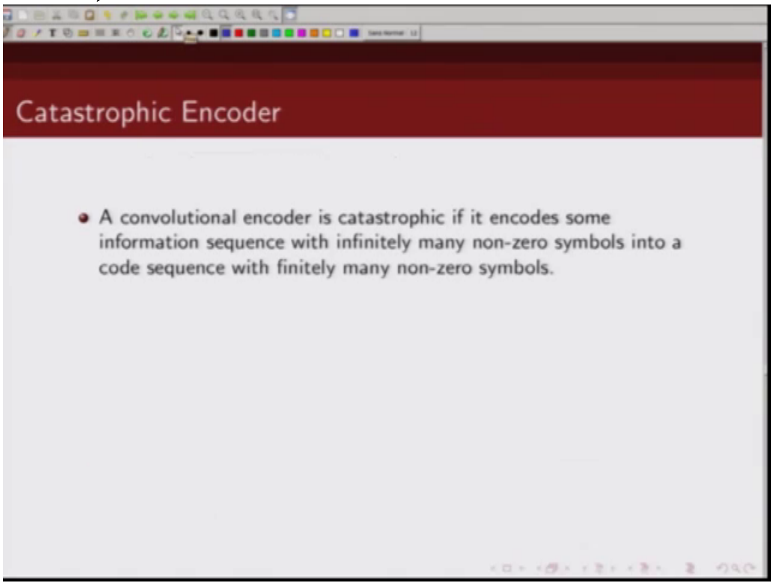

we will explain the concept of catastrophic encoder. So convolutional encoder is catastrophic if it encodes some information sequence which has large weight, which has large number of 1's into a code sequence with finite number of 1's. So if you have an information sequence of let's say,

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u of D which is

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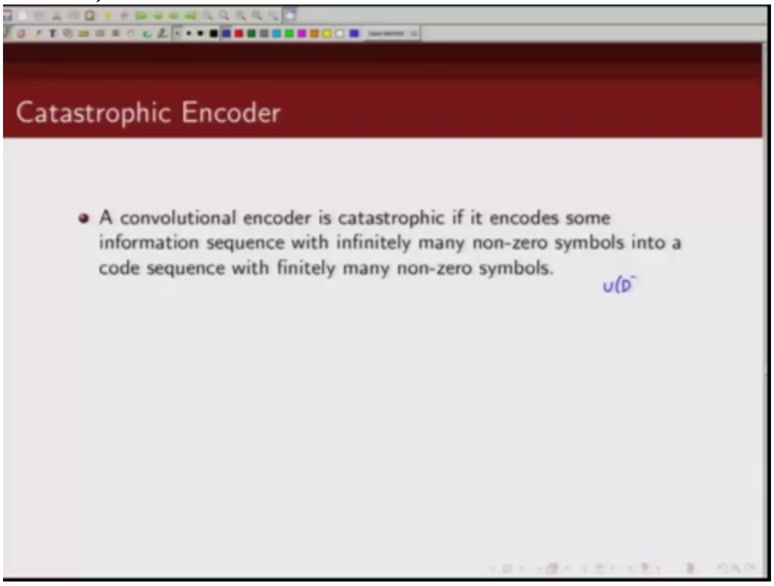

1, 1 plus D. Now this is a sequence of all 1's.

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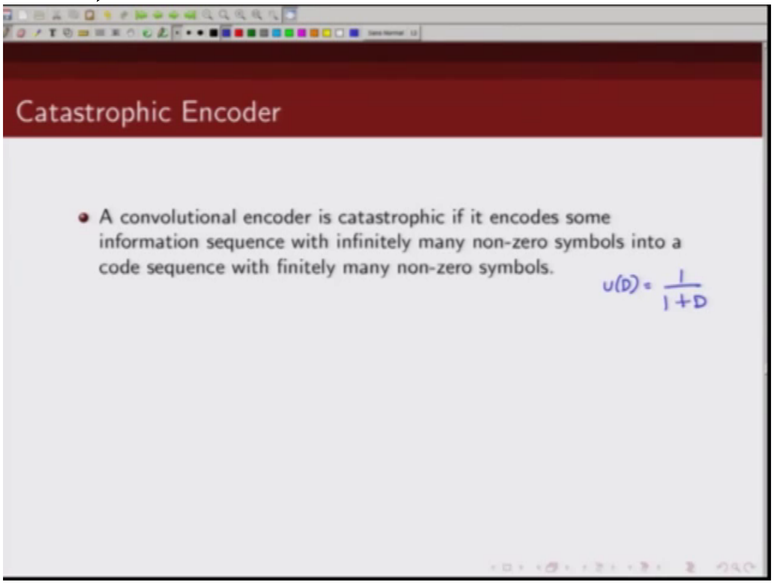

This is basically nothing but 1 plus D plus D square dah dah dah, so this is a sequence of

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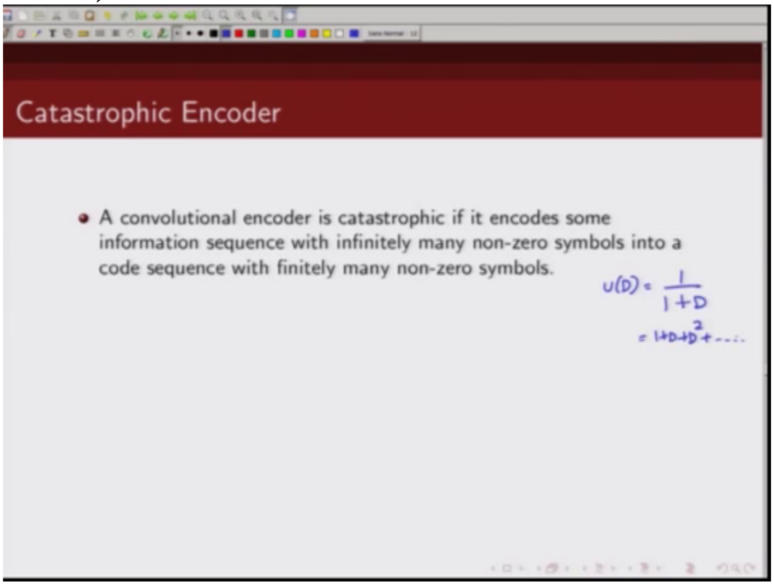

1, all 1's. Now if you have an encoder which maps a sequence, input sequence which has large number of 1's into a sequence, coded sequence with finite number of 1's; now that type of encoder is known as catastrophic encoder.

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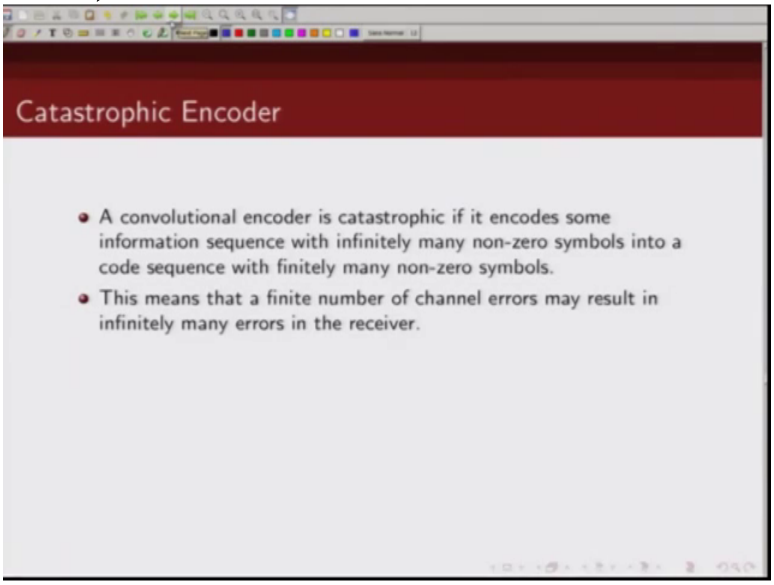

Now why is it catastrophic? So to illustrate it, we will take an example. It is an catastrophic encoder because a finite number of channel errors can result in infinite number of input errors. Because you have your information sequence which has large number of 1's,

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possibly infinite number of 1's. Because that information sequence is getting mapped, coded sequence with finite number of 1s; if error happens in those locations where you have finite number of 1's then your output sequence will get transformed into an all zero sequence and your decoder will think you have transmitted an all zero sequence; whereas actually you had transmitted a sequence of all 1s'. So finite number of channel errors in case of a catastrophic encoders can result in infinite number of input errors.

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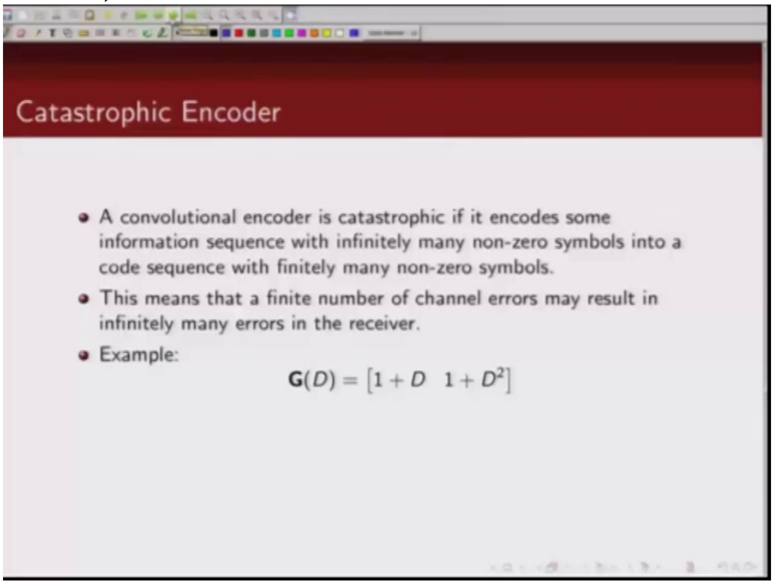

Let us take an example of this encoder with generator matrix G D which is given by 1 plus D and 1 plus D square and let us feed input which is all, sequence of all 1's which I can write as 1

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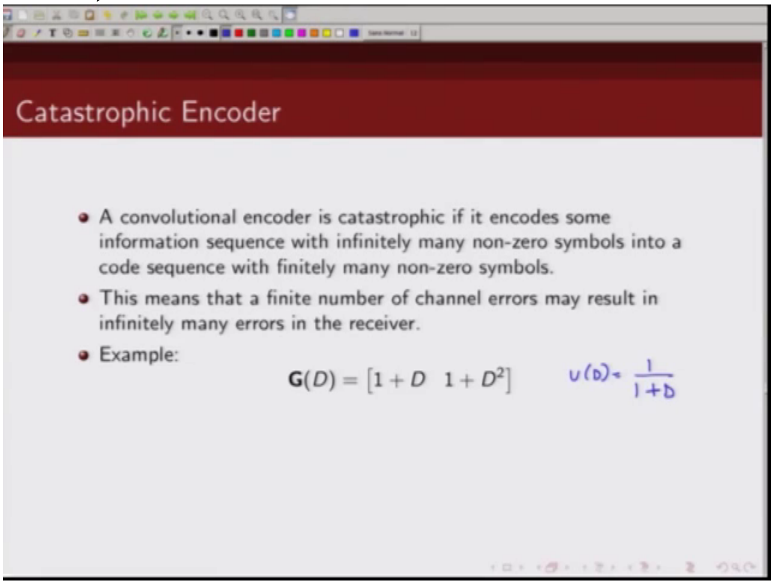

by 1 plus D. Now if this information sequence passes through this encoder what would be your output sequence? Output sequence would be 1 and this would be 1 plus D. So what you would get is

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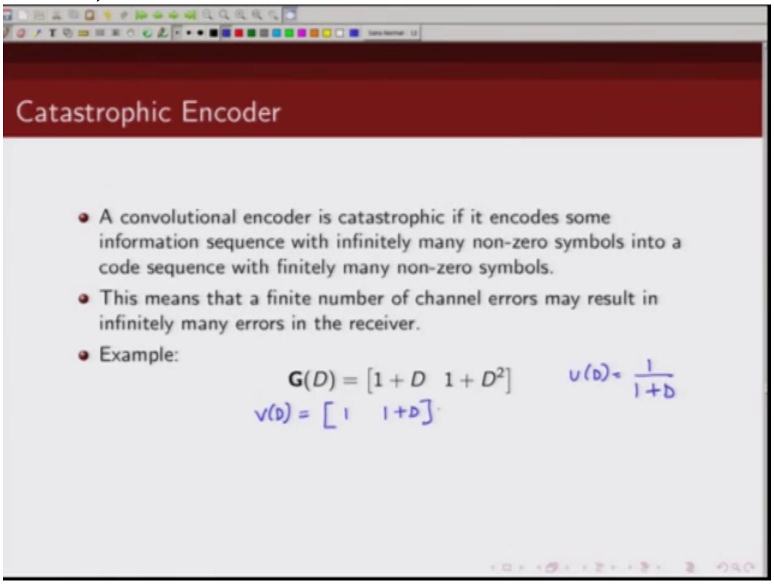

you would get output sequence which has weight only 3 where as information sequence has infinite number of 1's. So here is an example where an input sequence of very large number of 1's getting mapped to an output sequence of only weight 3. What if error happens in these 3 locations where you had 1's? Then your output sequence that

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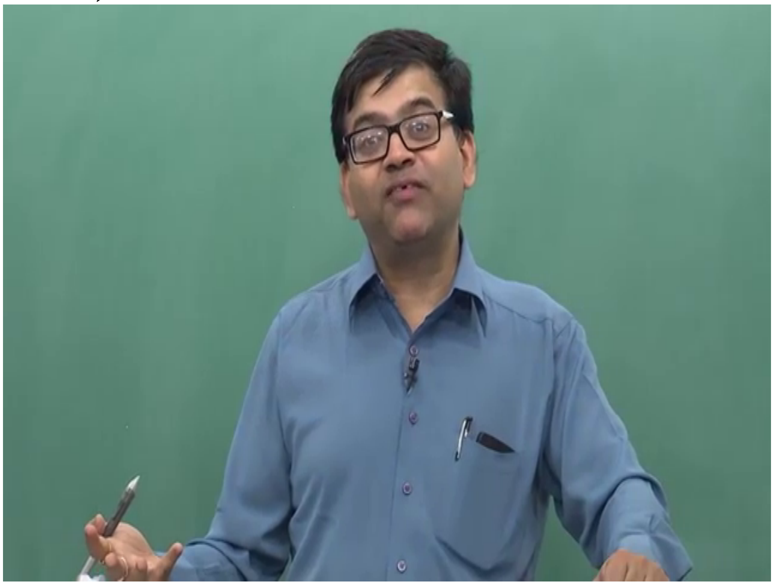

decoder will, receiver will receive will be all zero sequence and the receiver will think that you transmit, you transmitted all zero sequence where as the input is all 1 sequence. So you can see in case of a catastrophic encoder, a finite number of errors, in this example only 3 errors can result in infinite number of errors, input errors Ok.

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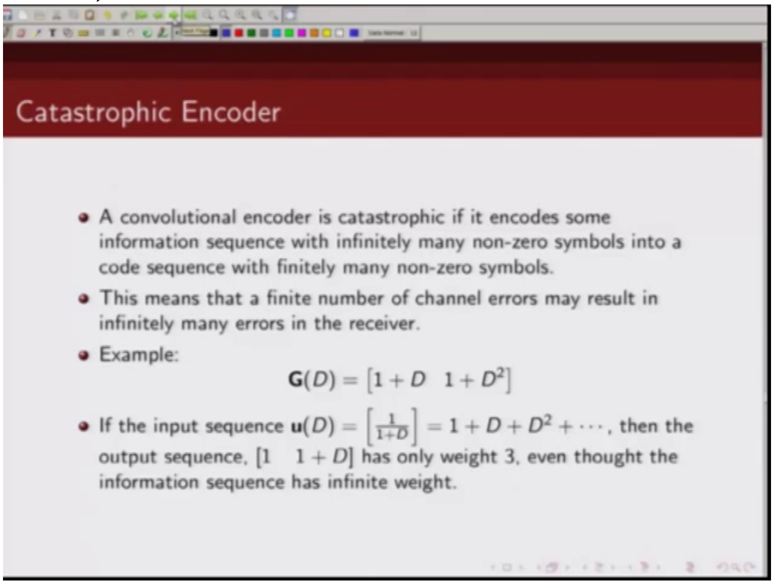

This I have explained.

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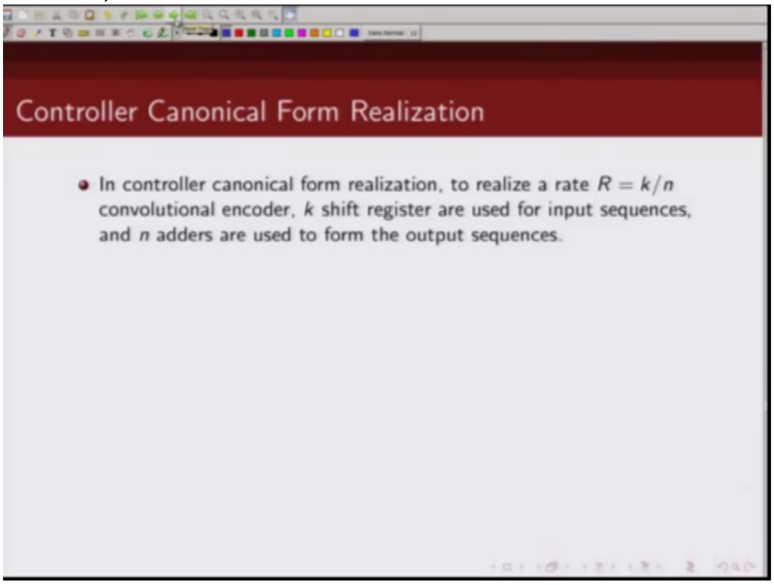

Next I am going to come to the topic of realization of a convolutional encoder. How can we represent

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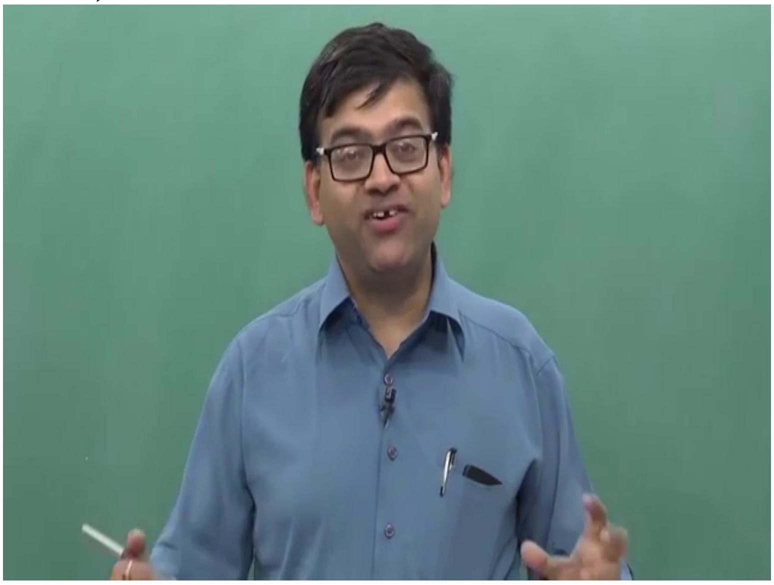

a convolutional encoder using shift register? So given a generator matrix how can you implement a convolutional encoder? So in this we are going to talk about 2 such type of realization. The first one that we are going to discuss now is known as controller canonical form realization. So in a controller canonical

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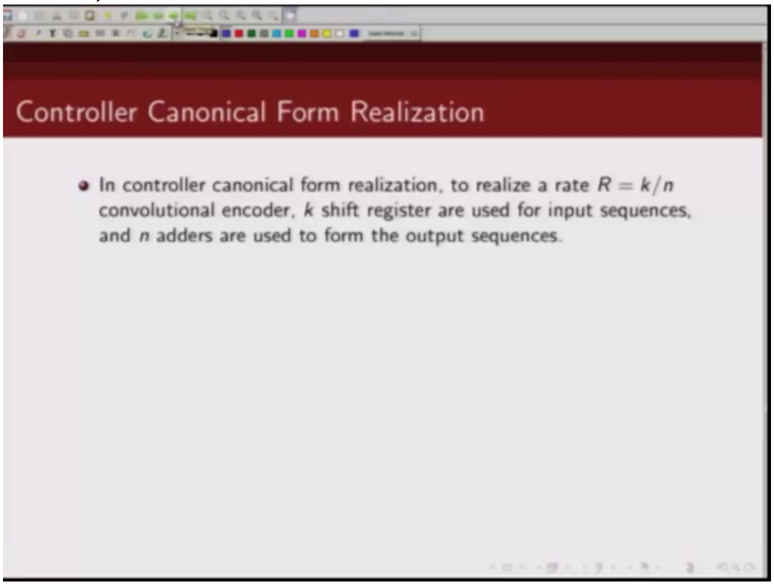

form realization if you have a rate k by n convolutional encoder we use k shift registers. So the number of shift registers used is equal to number of information sequence that you have. And the output is obtained by using n set of adders, one for each output sequence.

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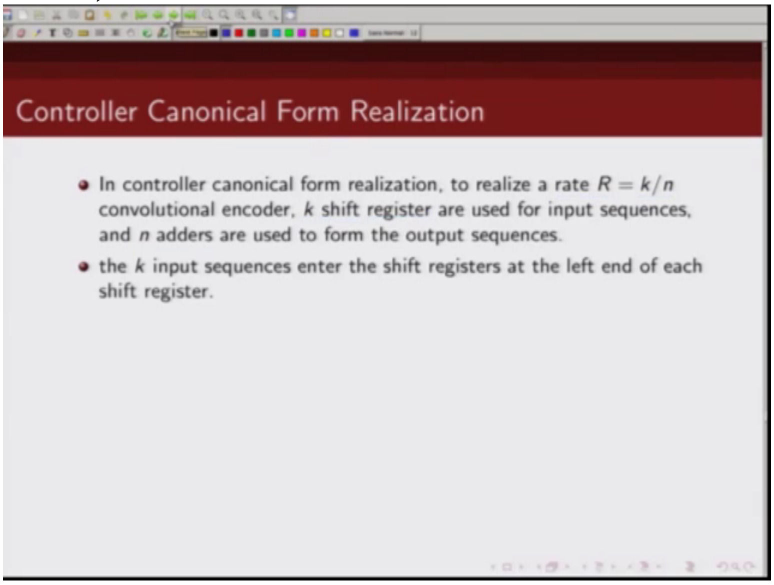

And in this case the key input sequence enter the

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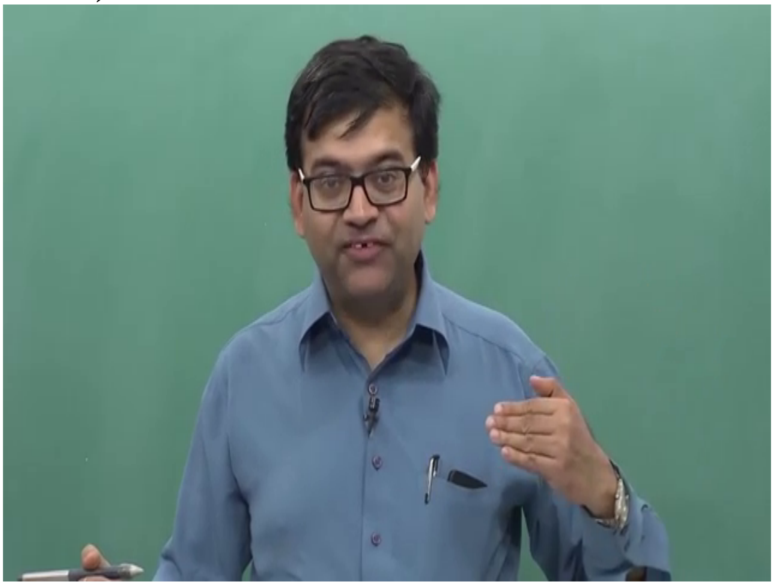

shift register from the left hand side and we take the output from the right hand side.

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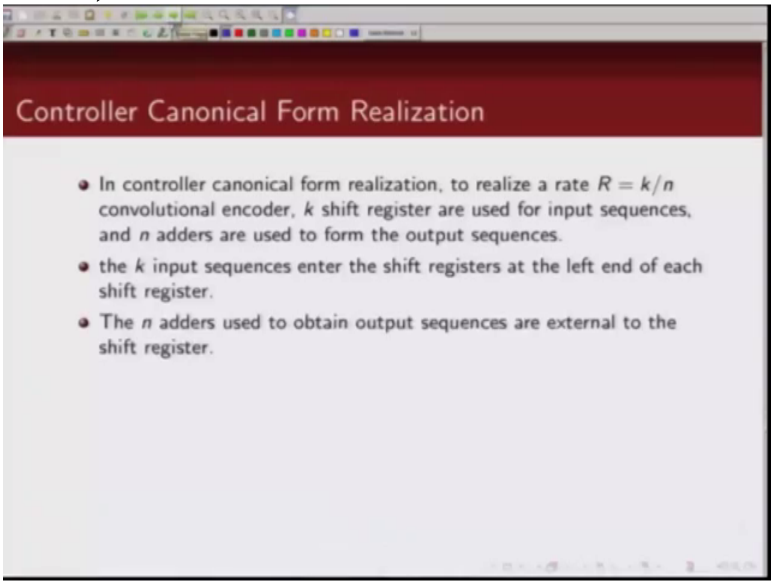

The next point to remember here is in case of a controller canonical form realization; these n adders that are used to obtain the output sequence, the

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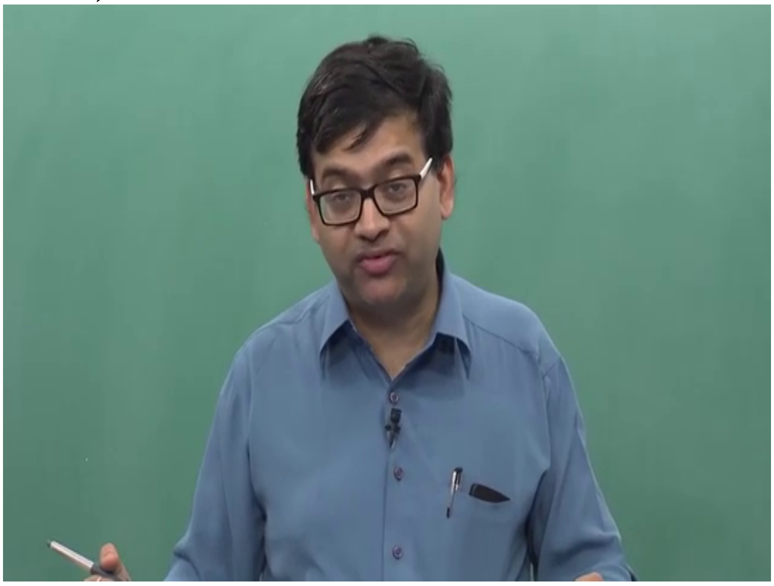

coded sequence, these adders are external to the shift registers. So they are not inside

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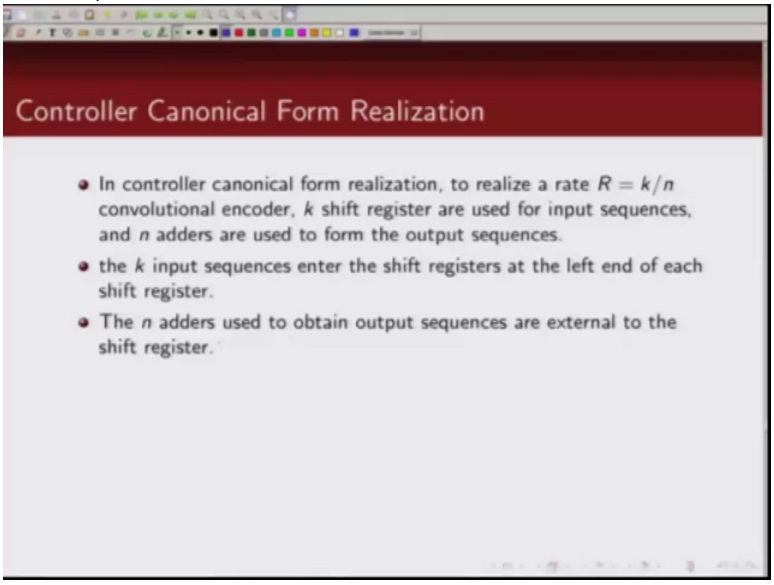

the shift registers.

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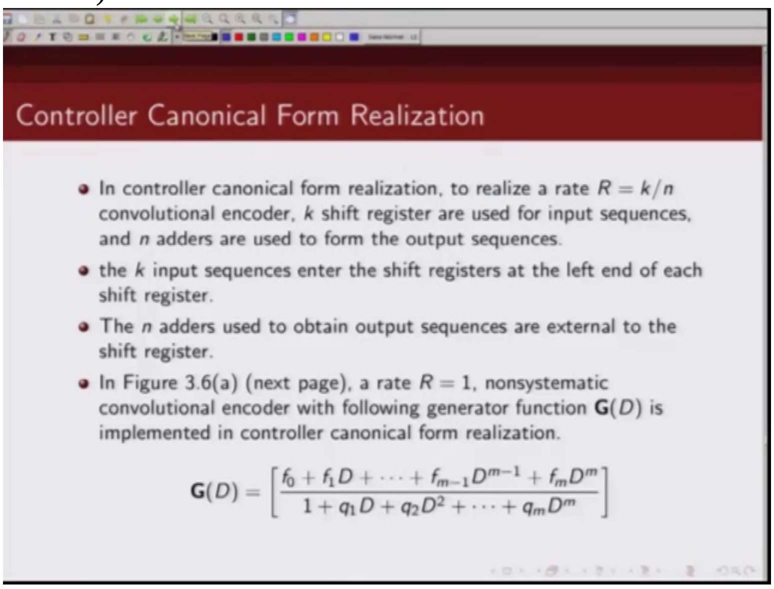

So let us take an example of a rate 1 non systematic convolutional encoder whose generator matrix is given by this. So in the numerator you have f 0 plus f 1 D plus f 2 D square like that. Similarly denominator you have 1 plus q 1 D plus q 2 D square like that. So how can we implement this using controller canonical form realization? So let's go back. So we are going to use k shift registers. So this is rate 1, 1 by 1 so there will be only 1 shift register. So we use

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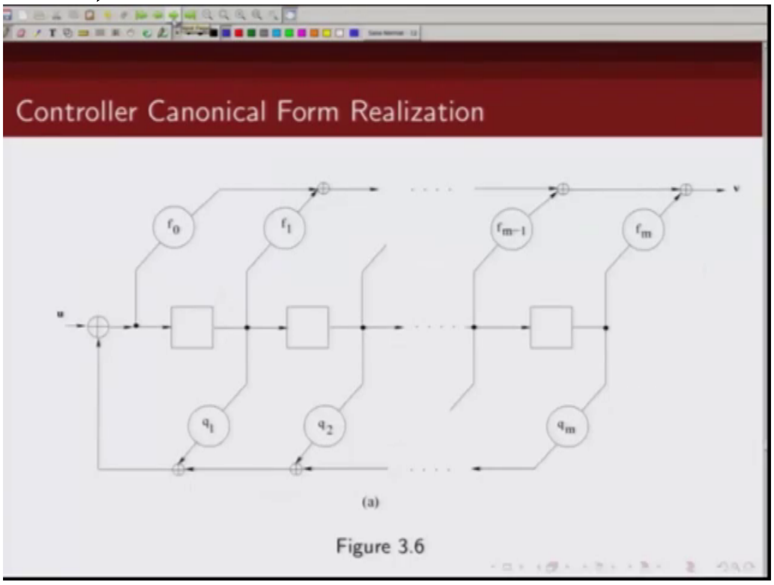

1 set of shift register corresponding to 1 input sequence. Next

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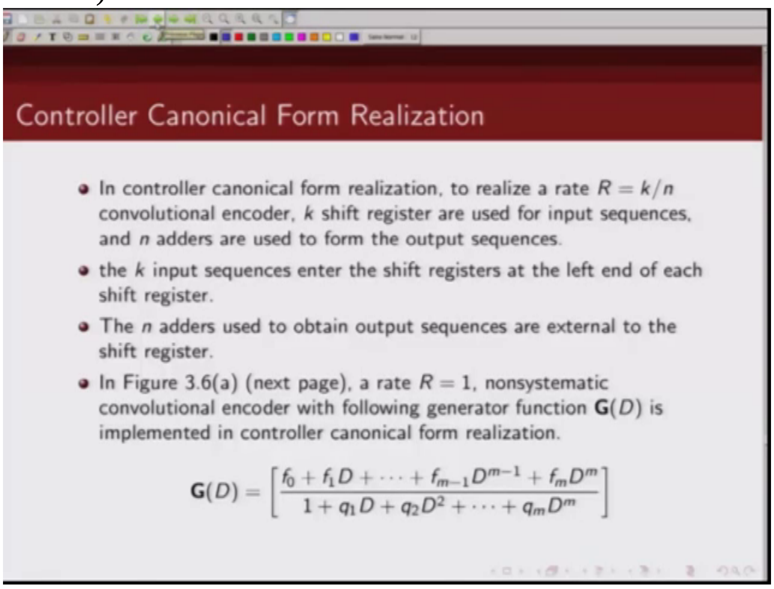

we use n set of adders. Now what is n here? Because it is rate 1, so n is also 1. So we will use 1 set of adders.

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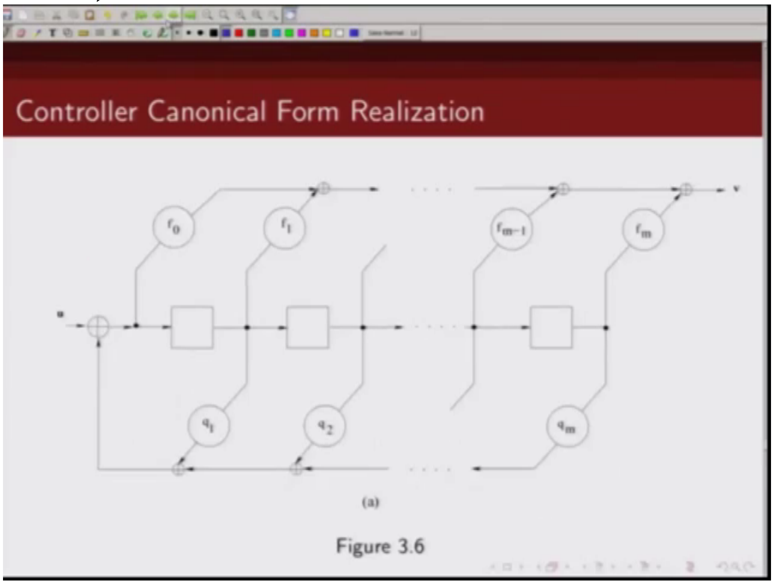

And these set of adders basically, this output that we are seeing, we have this n set of uh, adders that we are using to obtain this coded sequence v. Now

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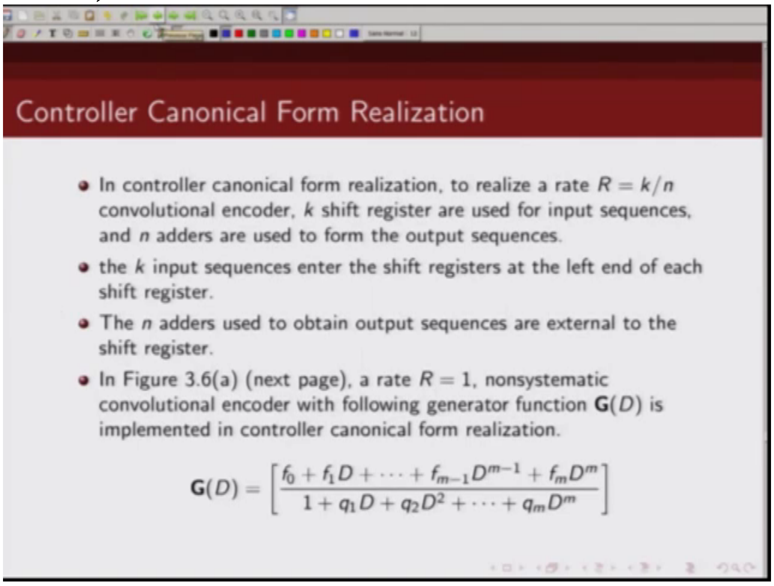

the key input sequence enter the shift register from the left hand side; so we can see here

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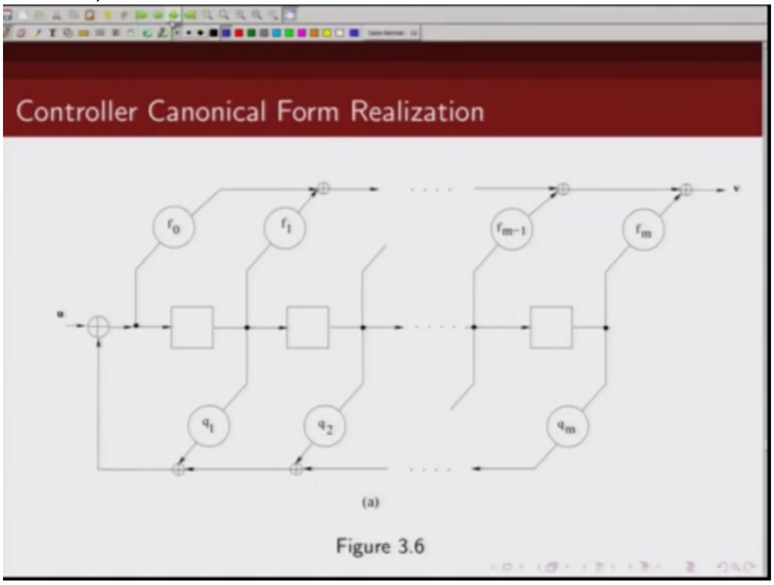

the input is entering from this (()) side. So since this is a feedback encoder so let's

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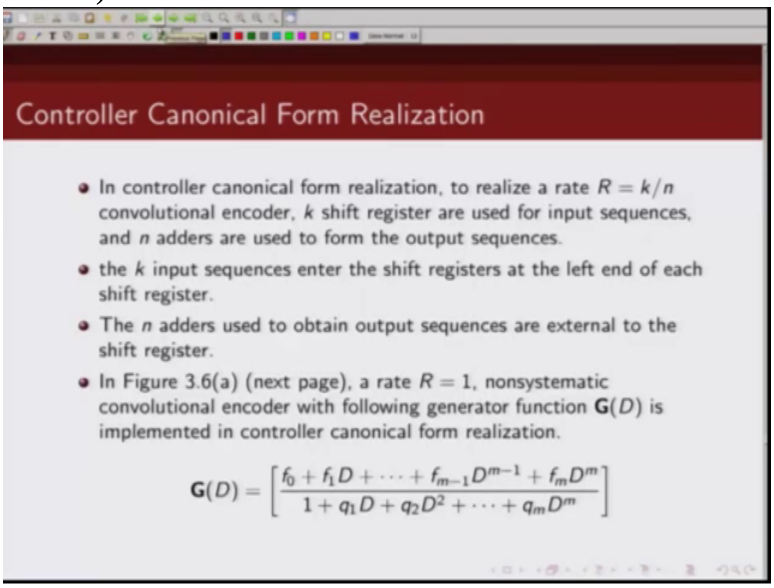

first look at the numerator term. What do we have here? We have f 0 plus f 1 D plus f square D so this input is basically multiplied by f 0. So current input is

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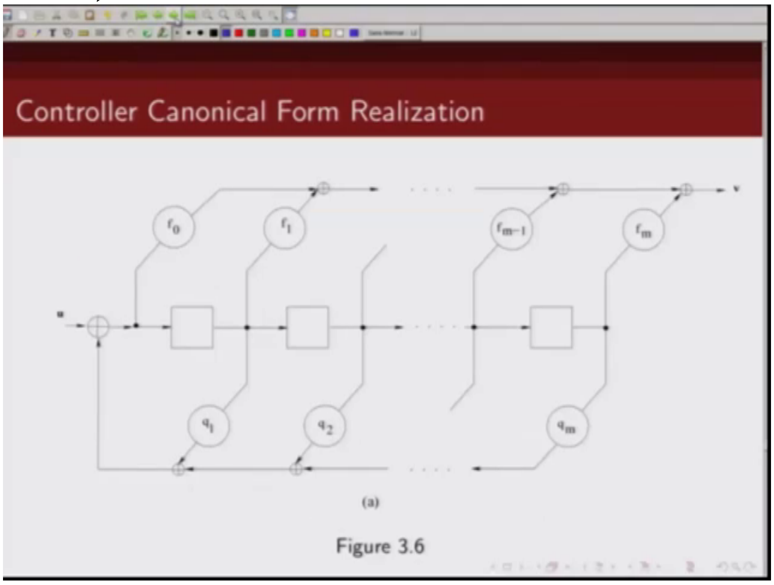

getting multiplied by f 0. Then one delayed version of input is getting multiplied by f 1, 2 delayed version is getting multiplied by f 2. So you can see this is then f 0, this is f 1, this is f 2 and again whether there is a connection from this input to the output, depending on that either f 0, f 1, f 2 will be either 1 or 0. If there is a connection, this will be 1, if there is no connection, this will be zero. So you can see this is f 0, this is f 1 D, f 2 D square like that basically if this is mth delay element this will be f m D m. Similarly you look, go back and look

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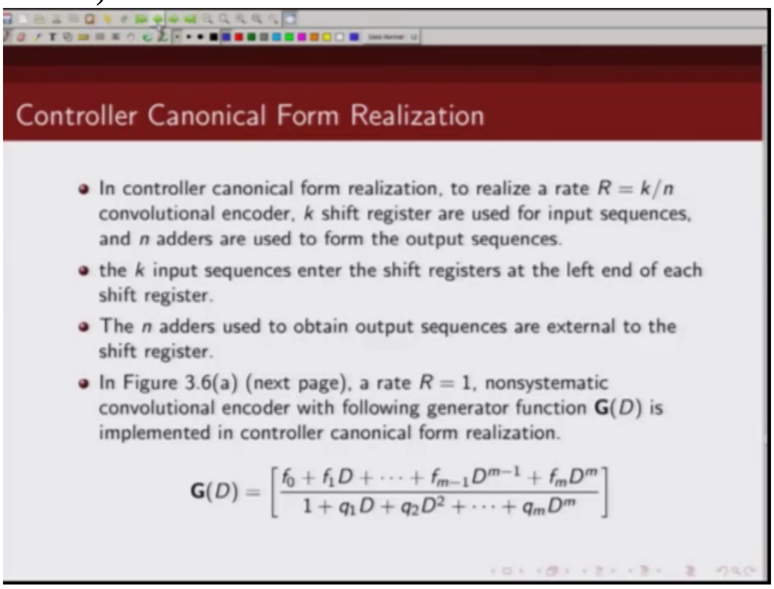

at the denominator. We have 1 plus q 1 D plus q 2 D square like that, so

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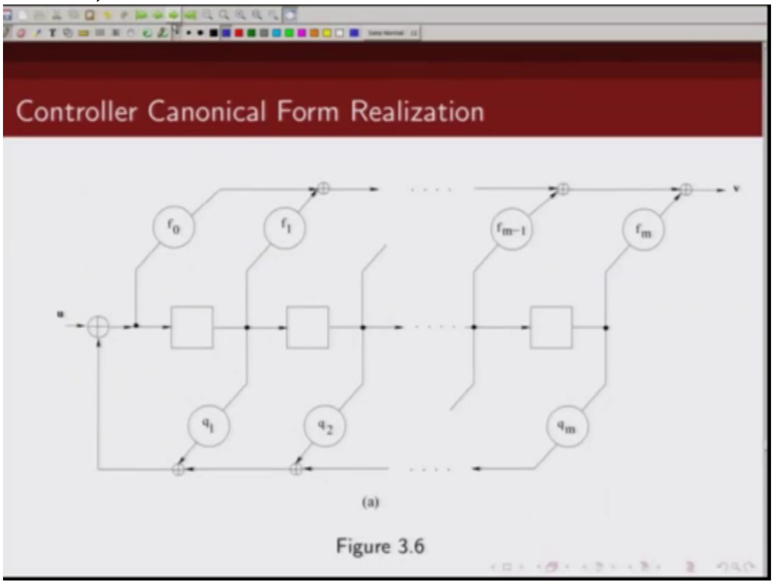

this is the input 1, this is, this is the D term q 1 D term, so this multiplied by q 1, this is D square term multiplied by q 2, like that and then finally you have D m term which is getting multiplied by q m. So you can see this is how we can realize convolutional code using controller canonical form realization. Please note these adders are external to shift register. There are no adders here internal to shift registers. The inputs are entering on left hand side where as output is taken from right hand side.

Now contrast this with

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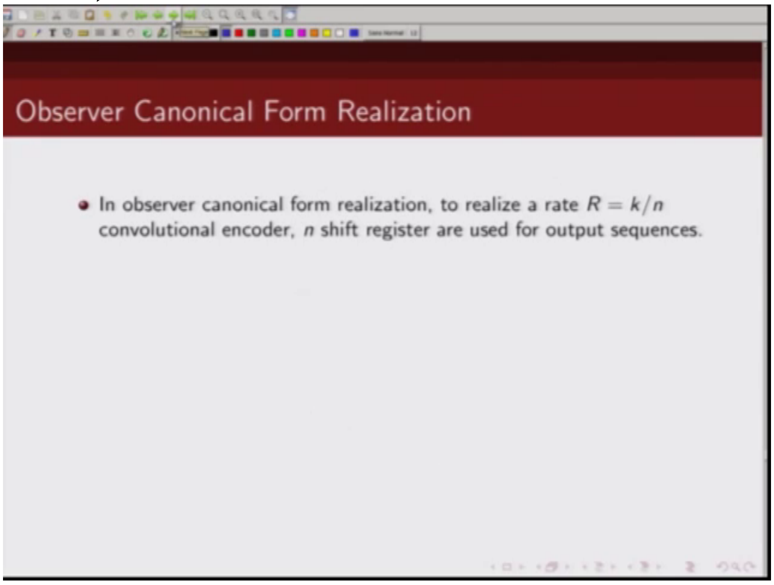

observer canonical form realization. So now observer canonical form realization, we need to realize the rate k by n encoder we require n shift registers. Now please note for the controller canonical form realization we require k set of shift registers; where as in this case we require n set of shift registers, one for each of the coded bits. The second difference is k input sequences in the observer canonical form realization, these k sequences enter into the shift register and these adders are internal to the shift registers. If you recall in case of a controller canonical

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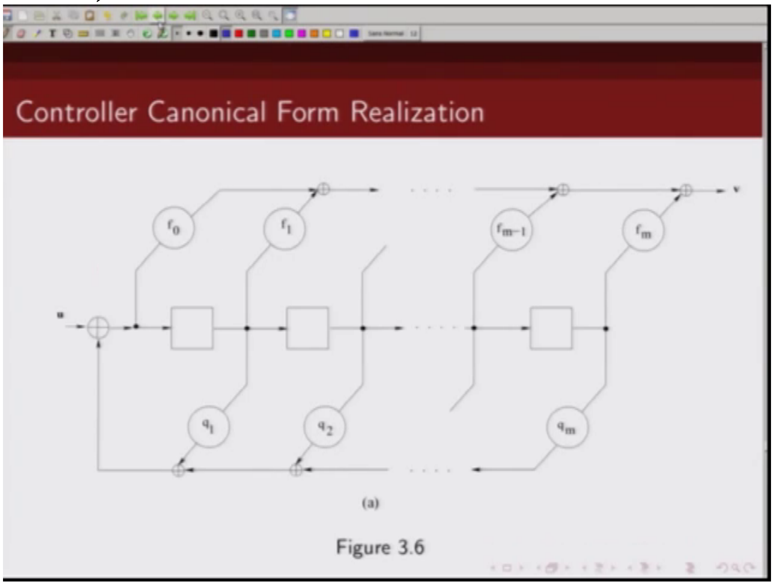

form realization, the input is entering here. And at each time instance when your clock comes they move, they shift to one location to the right. This will move to here, this will move to here where as in the observer canonical

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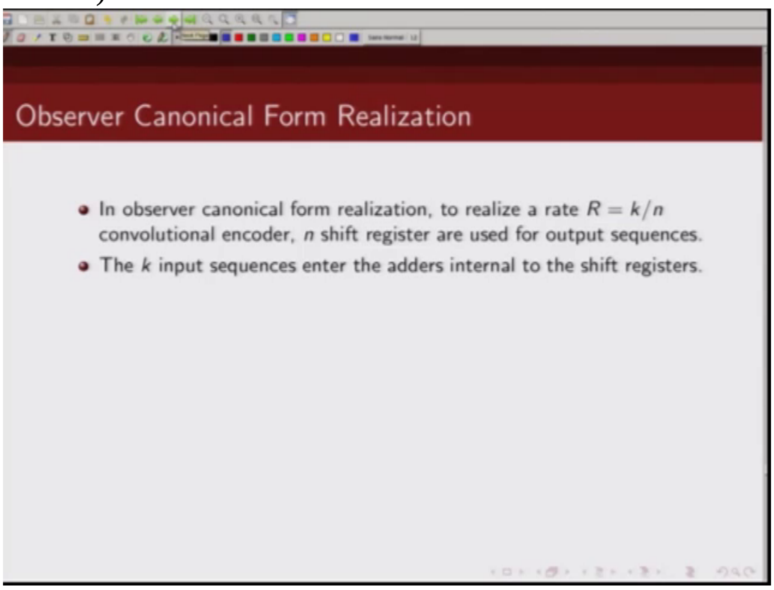

form realization these inputs are directly entering into the shift register and these adders are internal to the shift register. We will give an example to illustrate what we mean.

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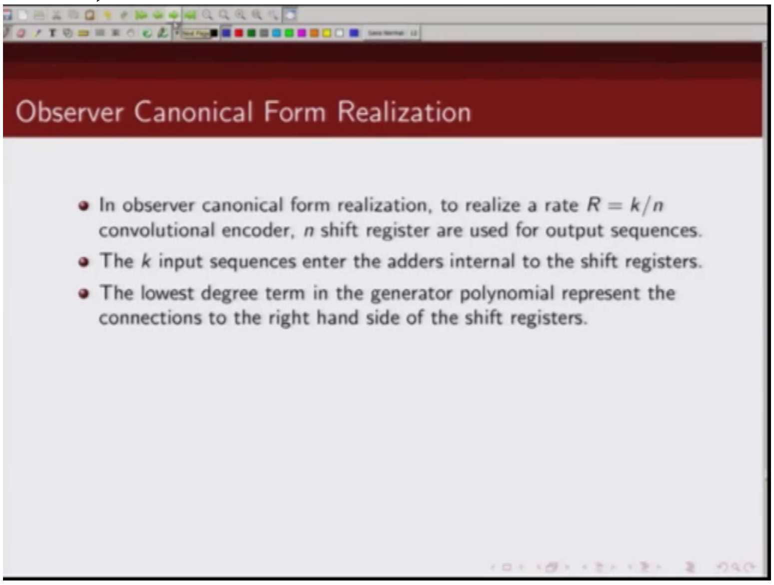

The lowest degree term generator matrix represents the connection to the right hand side of the shift register. In case of controller canonical form realization the lowest degree term was on the left hand side. Here the lowest degree term will be on the right hand side. So

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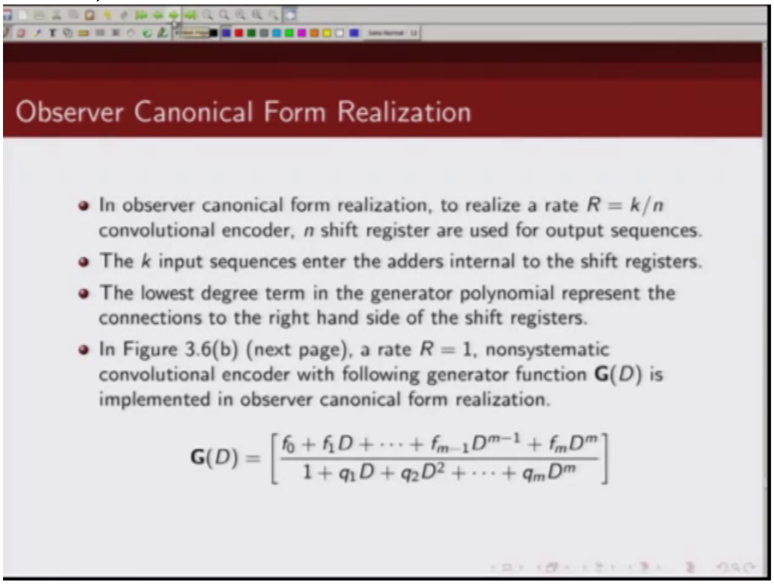

let us take the same example that we considered earlier. So we are considering the same generator matrix and we are going to realize generator matrix now using observer canonical form realization. So again here k is 1, n is 1, so we have n is1, so we have one set of shift registers.

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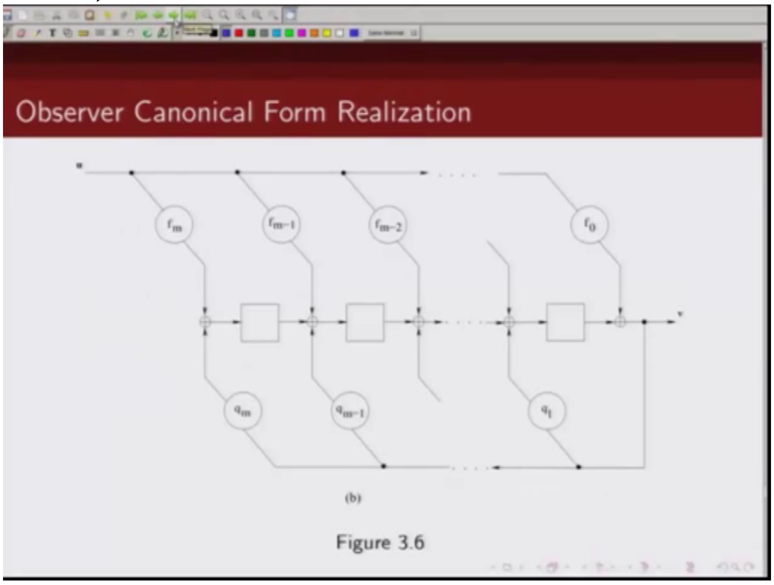

This is one set of shift registers. Next what did we say,

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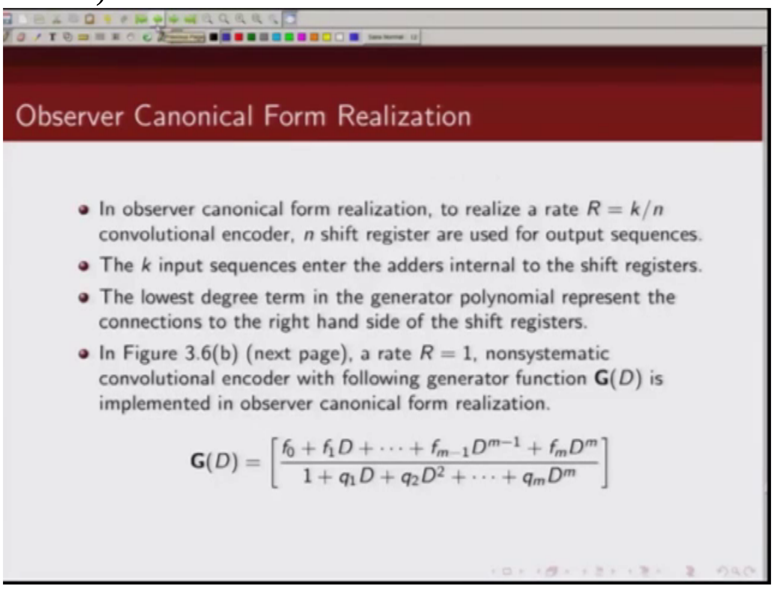

the k input sequence enter the adder internal to shift register and what do we mean by internal? So these are shift register elements,

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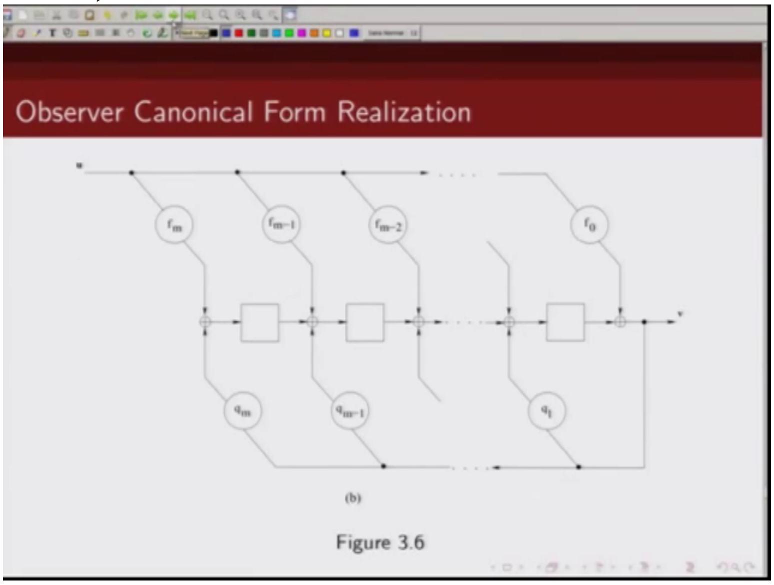

delay elements and note these adders are in between

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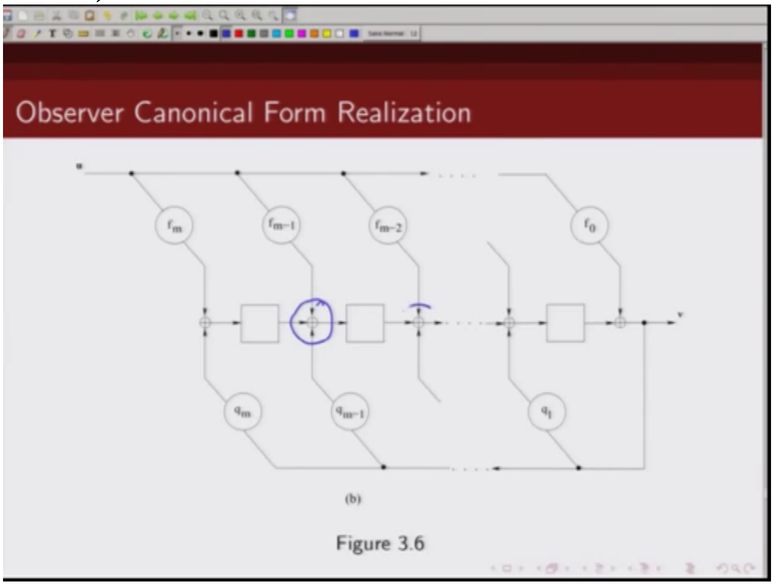

the

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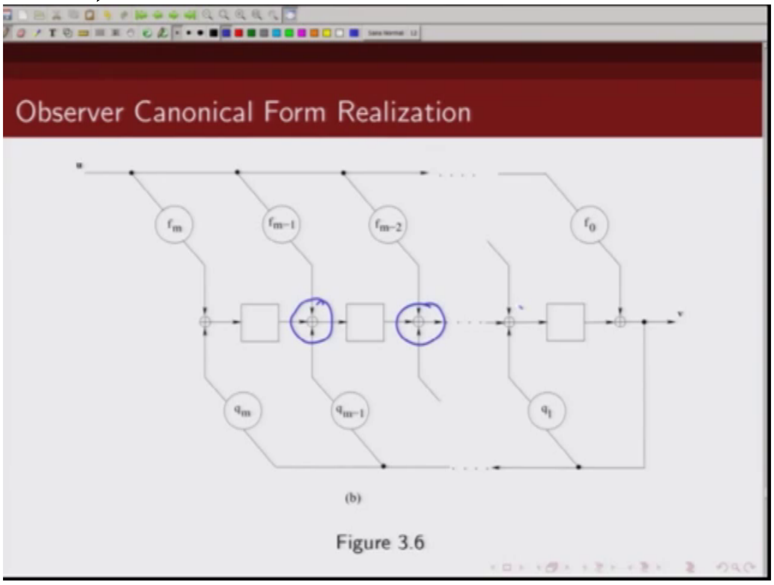

shift registers. These

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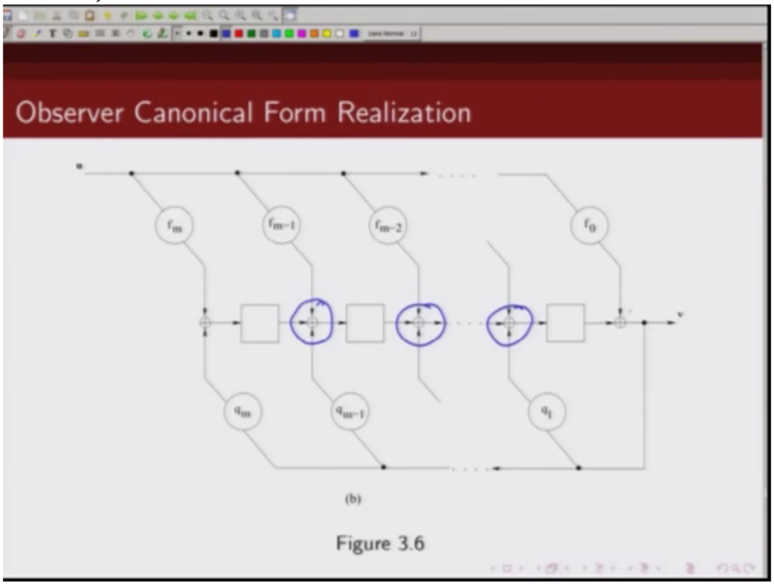

adders are internal

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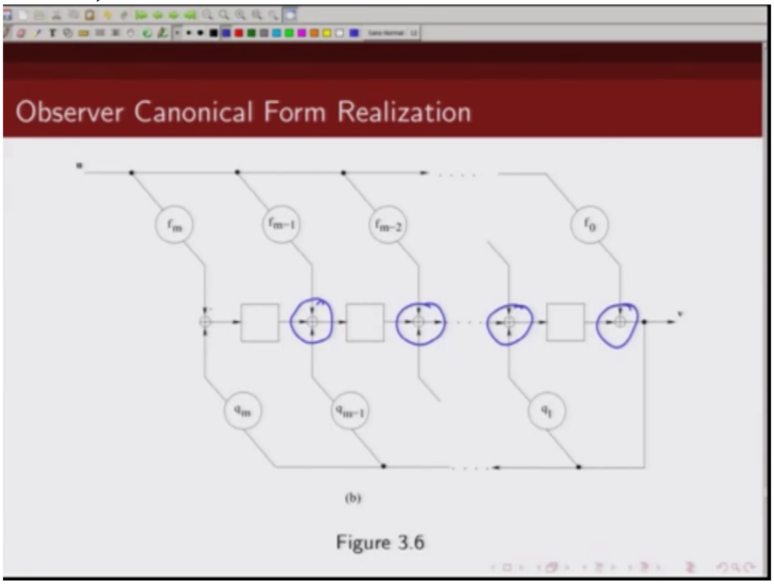

to the shift registers, Ok

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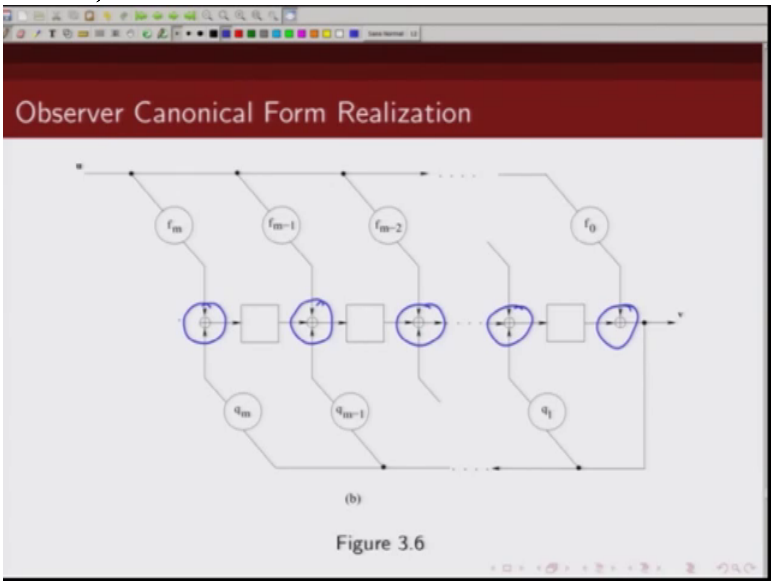

and next thing that we said

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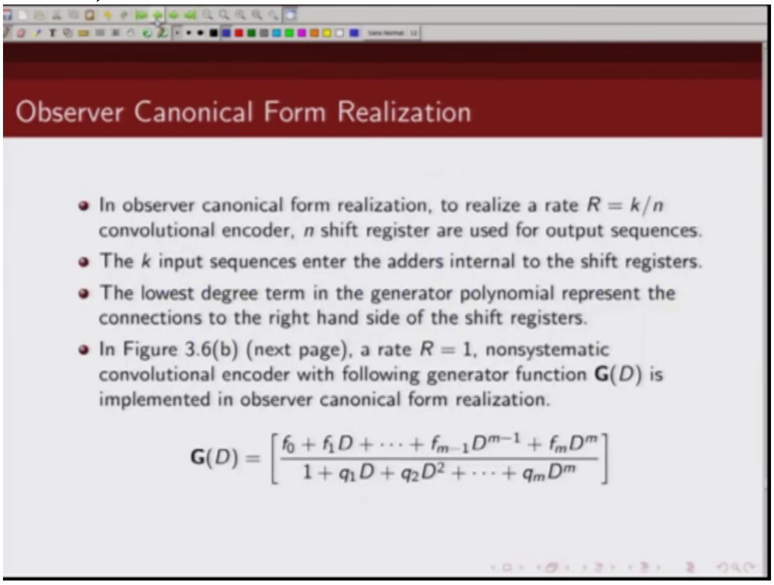

was the lowest degree term in the generator matrix represents connection to the right hand side. You see here,

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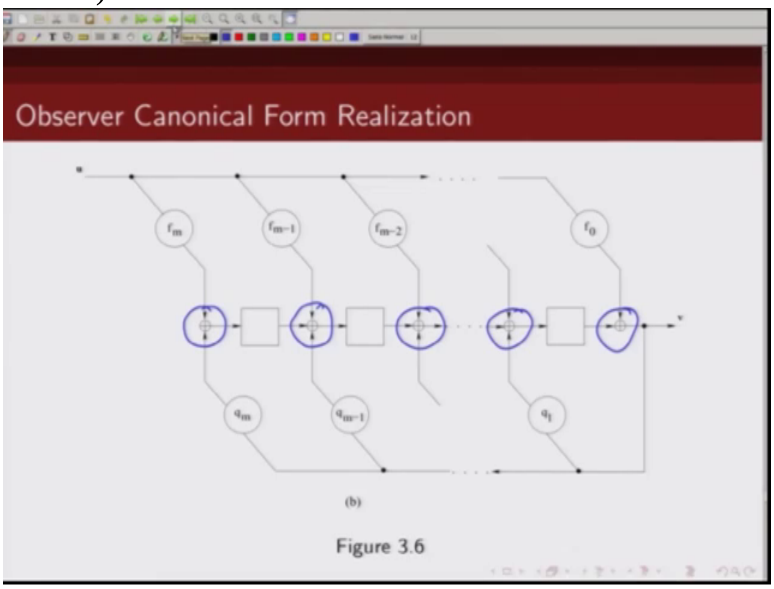

the inputs are directly coming to the adder. So this term is corresponding to f 0 u of D, this term corresponds to f 1 D of u of D. Where as in the controller canonical form the leftmost term was f naught and rightmost was f m. Here just opposite. So you can see this is f 0 term, f 1 term, f 2 term and similarly in the denominator this is q 1, this is q 2, like that this will be q m. Same generator matrix can be realized using 2 different forms.

So let us take an

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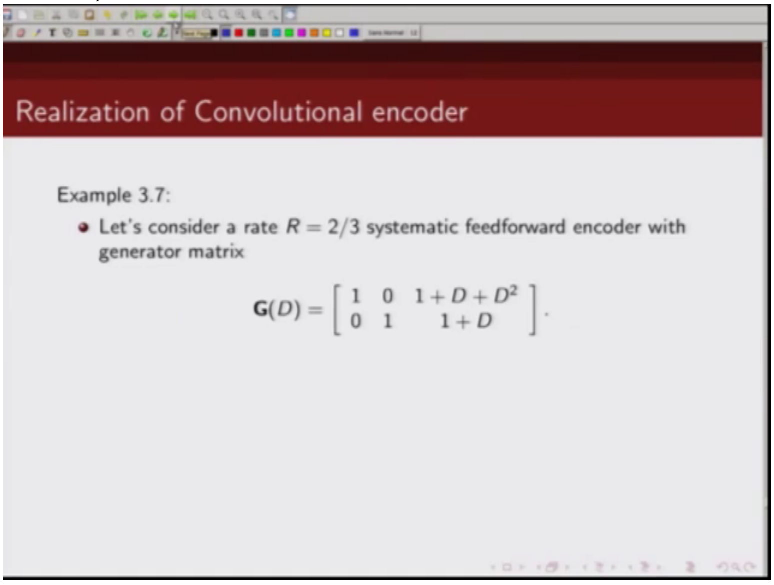

example to illustrate this. So we are considering a rate 2 by 3 systematic feed forward encoder whose generator matrix is given by this. Now let us try to realize this generator matrix using controller canonical form realization and observer form realization. So the parity check matrix for

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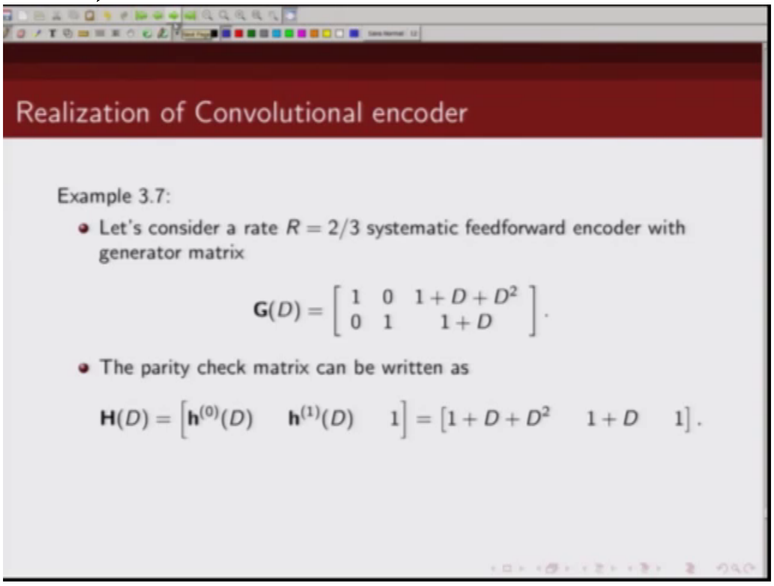

this is given by this expression. We will just

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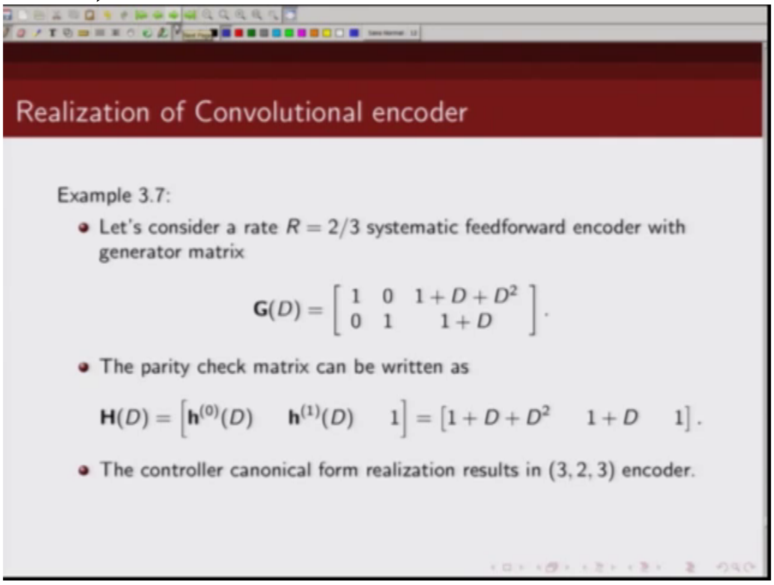

show you that, so in controller canonical form realization, we have, so there are 2 inputs here. So we will have one set of shift registers for each of the input. So we will have one set of shift registers for this

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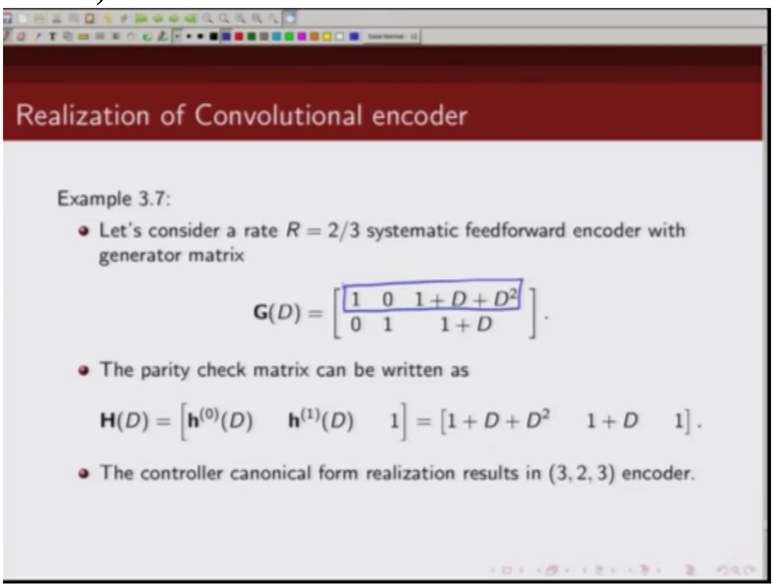

and one set of shift registers for this.

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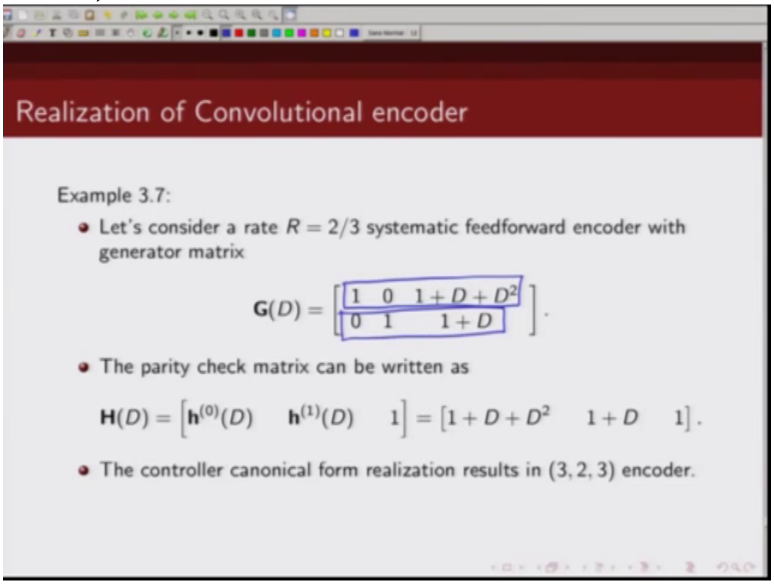

And to realize this we need two memory elements because here, the highest degree of D is 2. And to realize this, we require 1 memory element. So total we would require 3 memory elements. So that's what I said, for controller canonical form realization for this rate two third, this is my n, this is k and this is memory order.

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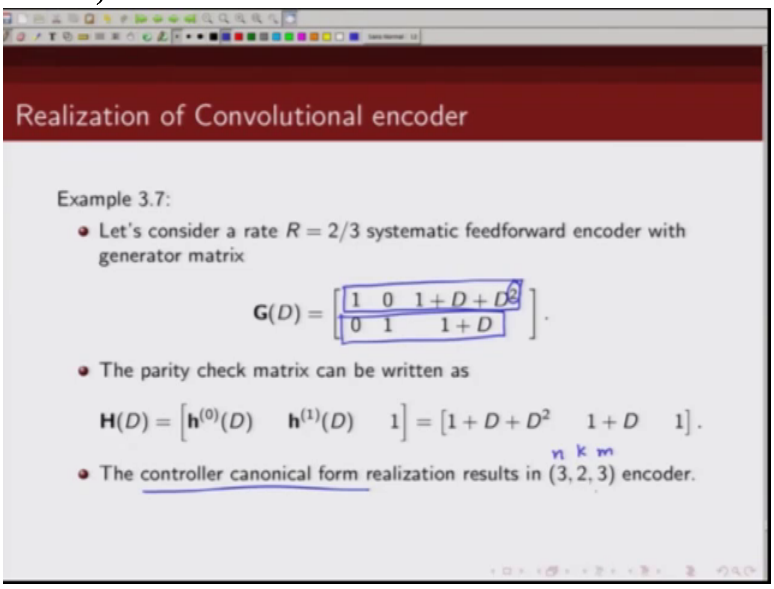

p basically requires 3 memory elements to represent this convolutional encoder in the controller canonical form realization. Now what observer canonical form realization? In observer canonical form realization we use one set of shift registers

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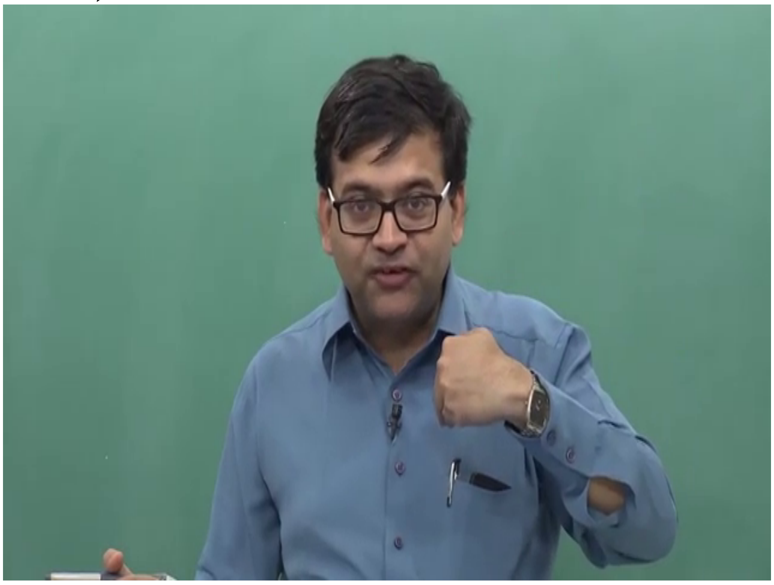

for each of the n coded bits. So how many coded bits we have,

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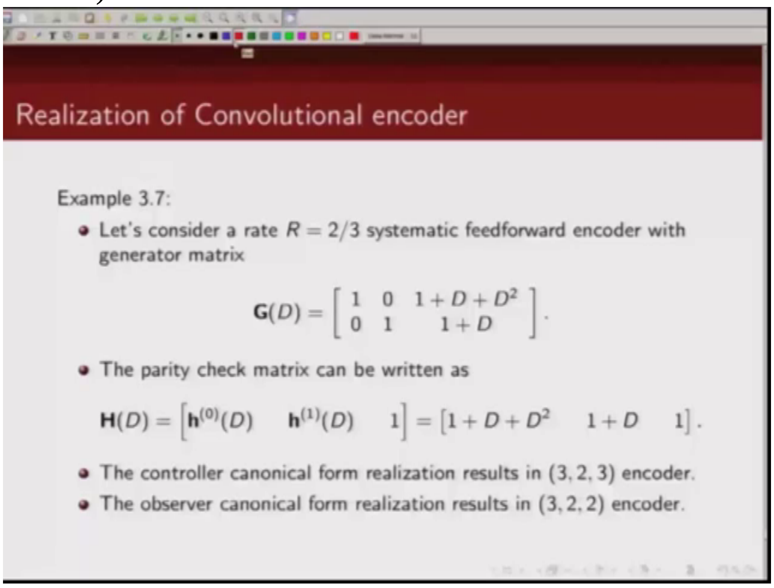

we have 3. One is this, one is this

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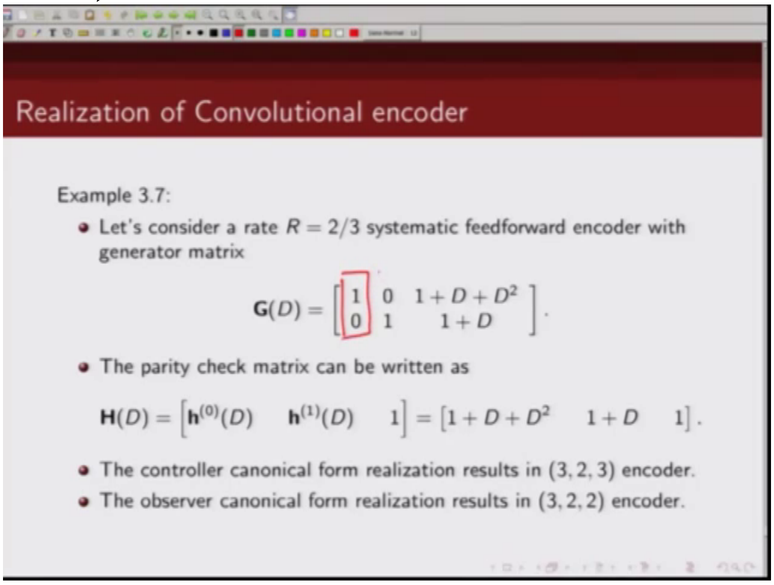

and

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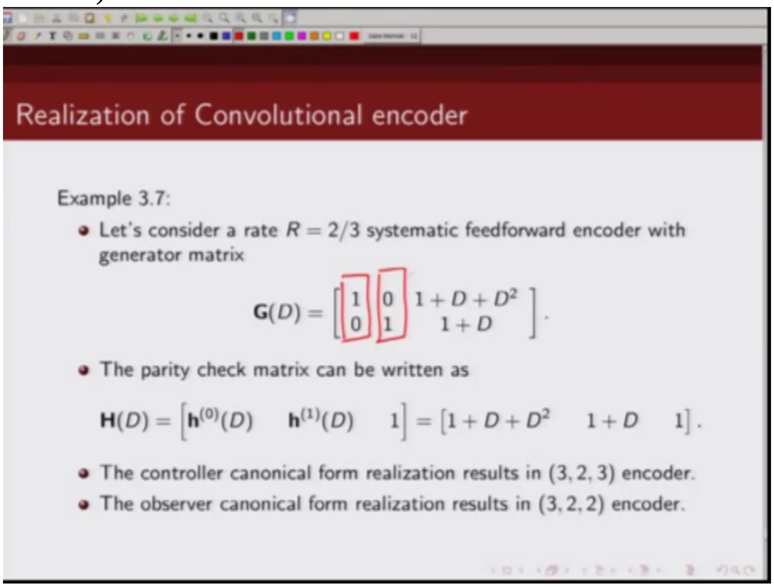

one is this.

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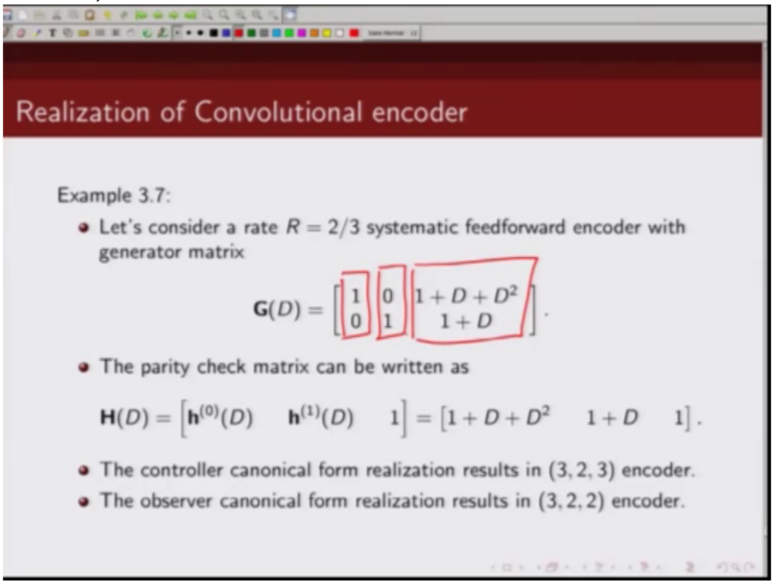

Now how many memory elements you require to represent this? Zero, directly the input is coming in here. Here zero, the direct input is coming here and what about this, its maximum degree is 2, we will require 2. So overall for this generator matrix if we try to realize it using observer canonical form realization, we require only 2 memory

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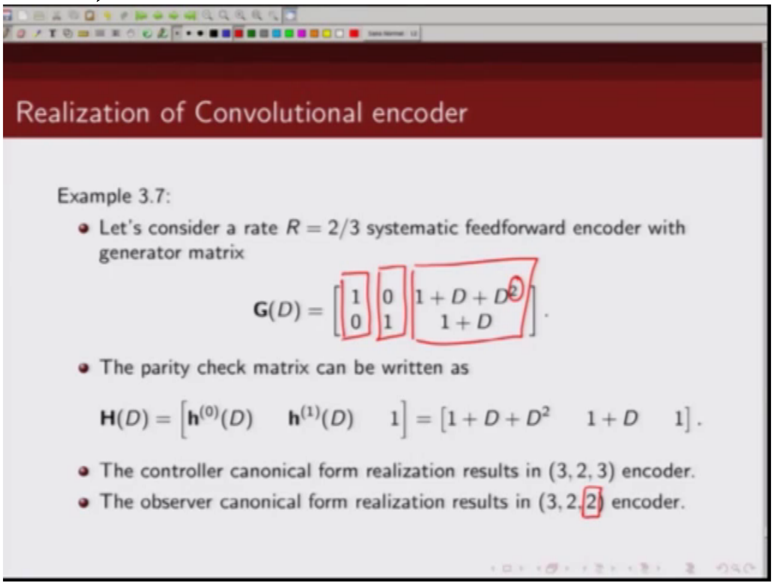

elements.

And in the next slide I am going to show you those 2 encoder realization. So let me just write down the generator matrix. My generator matrix G of D

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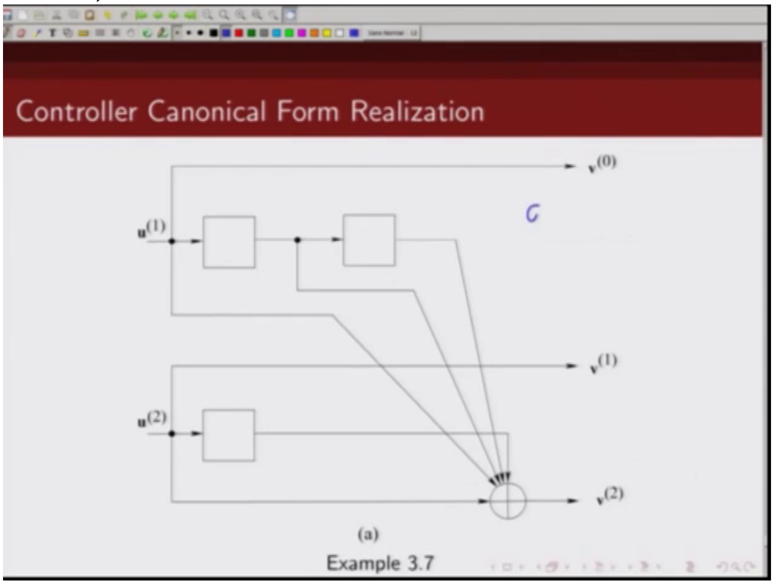

is 1 0 0 1, then what do we have, 1 plus D plus D square, 1 plus D plus D square, 1 plus D,

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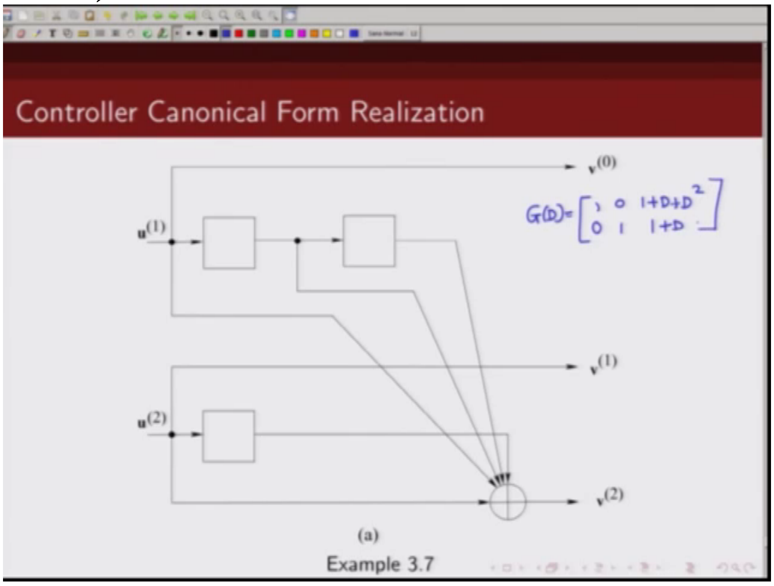

so one set of shift register for this. So this maximum degree is of these 2, so we use 2 memory elements and for this maximum uh degree of d is 1, so we use 1 memory element, Ok. Now what is the first output? First output is directly input u 1, so this is my u 1. Second output is directly u 2, this is basically this and the third output is 1 plus D plus D square of u 1 so this is u, this is the D of u D, u 1 D and this is D square of u 1 D plus 1 plus D times u 2 D. So 1 plus D meaning one term is u 2 and second is delayed version of u 2. So this will be my third coded bit. So you can see, to realize this generator matrix we require total 3 memory elements, 1, 2 and 3. Now let us see

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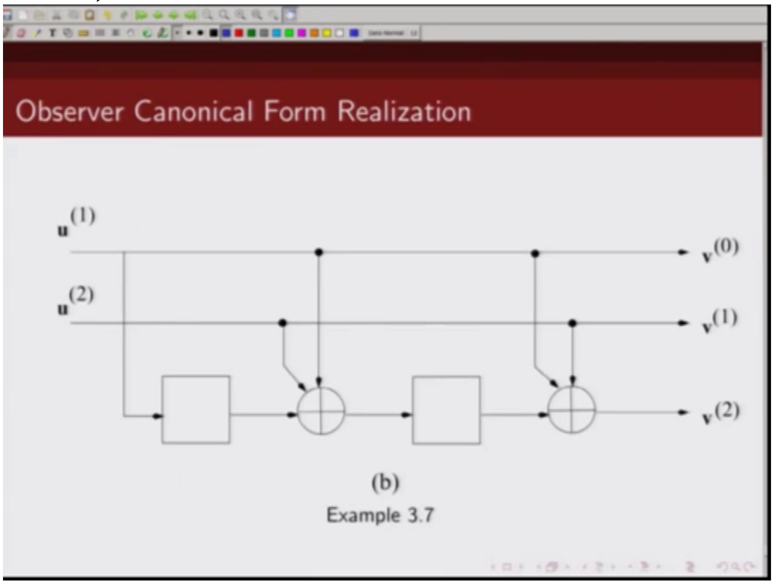

for the observer canonical form realization. Again let me write down my generator matrix. This is 1 0 0 1, 1 plus D plus D square 1 plus D. So we said one set of

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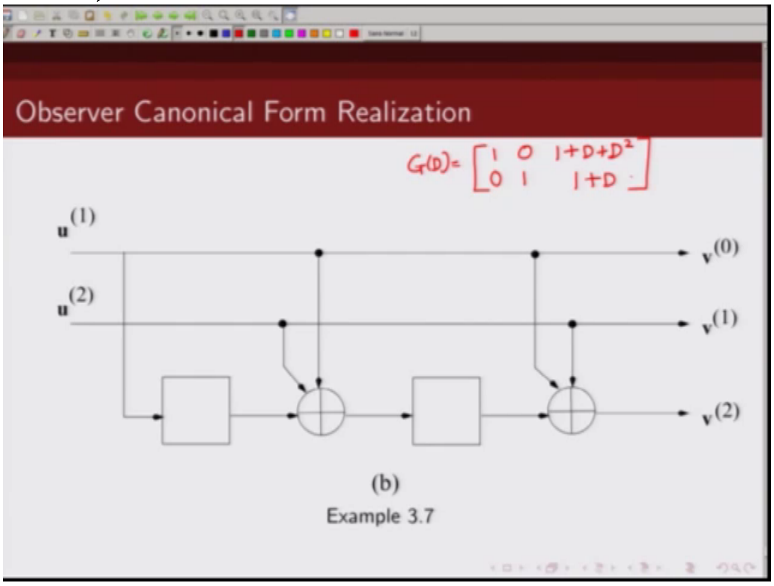

register. What is the maximum delay element here? Zero, so you can see directly. What about this? Again maximum degree of D is basically zero so no shift register. And here for the third line, D is 2 so we took 2 D. So what is the final output then? First one is, first coded bit is just u 1 of D, this is what it is. Second coded bit is u 2 of d, like this. And third coded bit is 1 plus D plus D square of u 1 of D. So what is u 1 of D? u 1 of D is,

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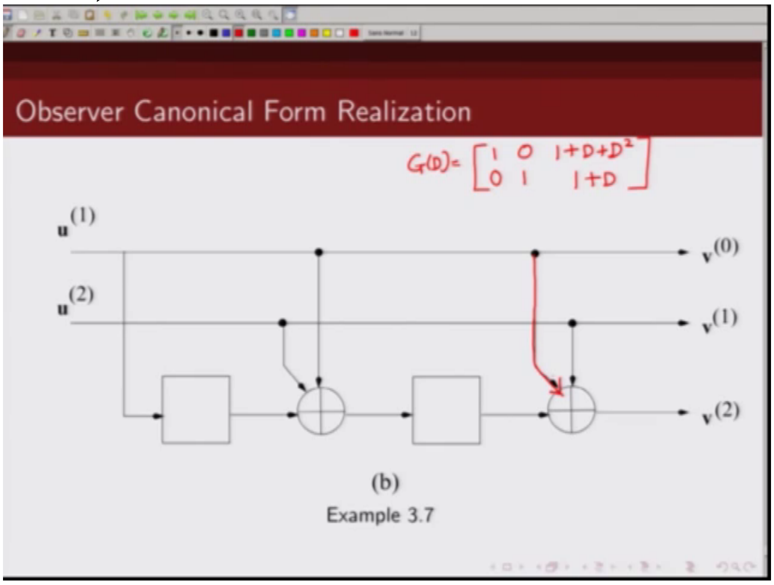

what is D times u 1 of D? That is this term. And what is D square

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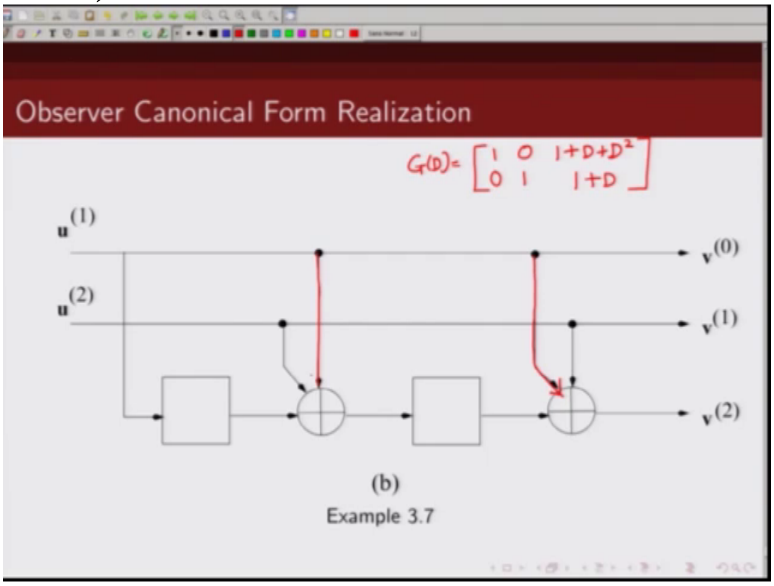

what is D times u 1 of D? That is this term. And what is D square of u 1 of D? That is this term,

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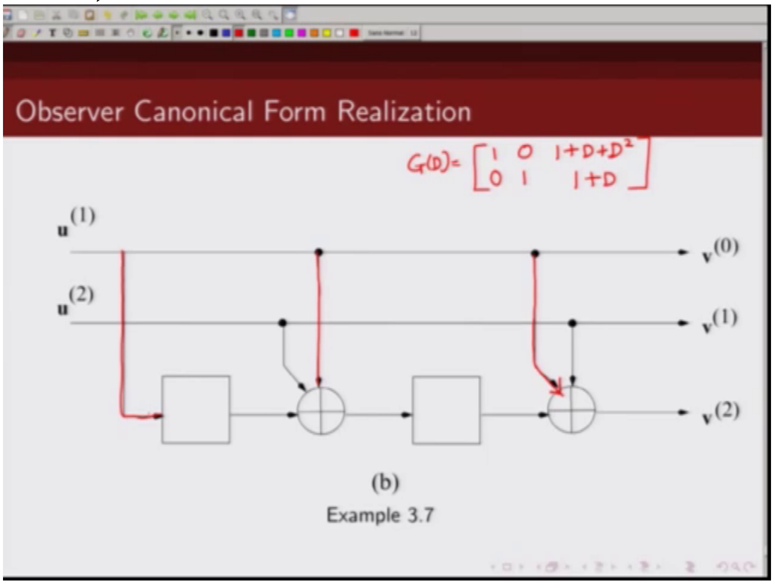

fine plus 1 plus D times u 2 of D. So then what we have is u 2 of D is this and

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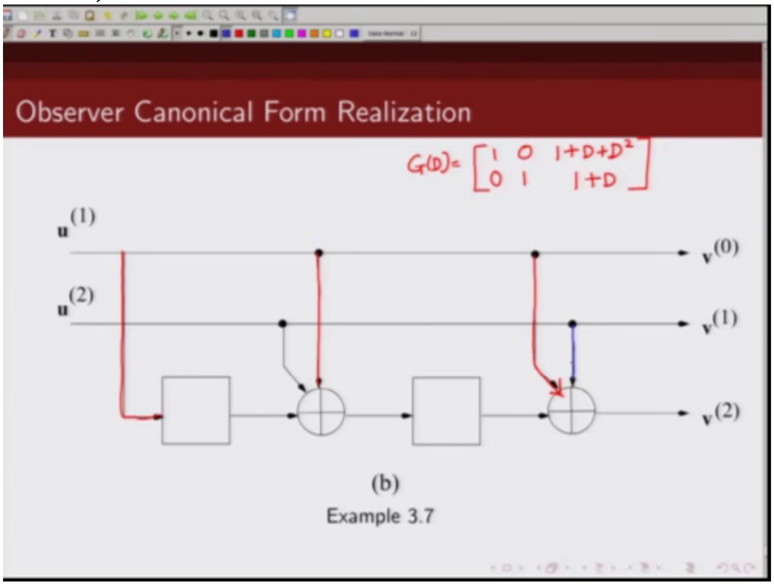

D times u 2 of D is this.

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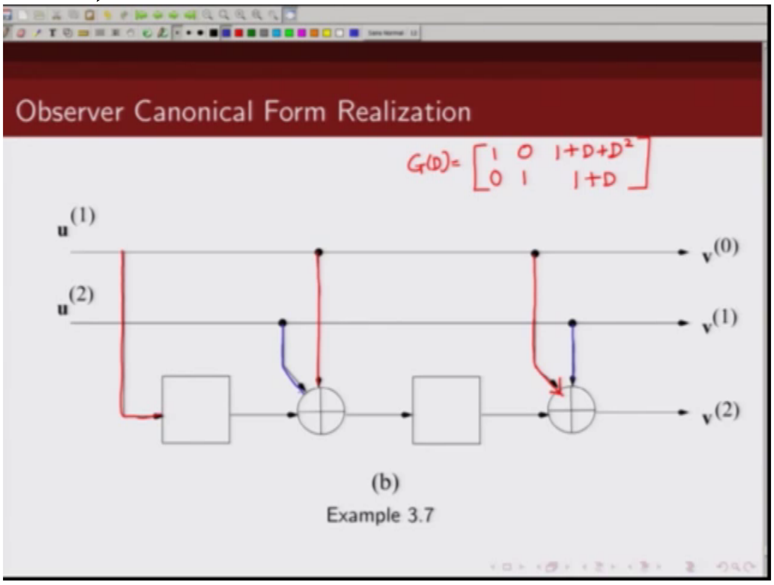

So this is our observer canonical form realization for this convolutional encoder with this generator

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matrix and note we only require two, 1, 2

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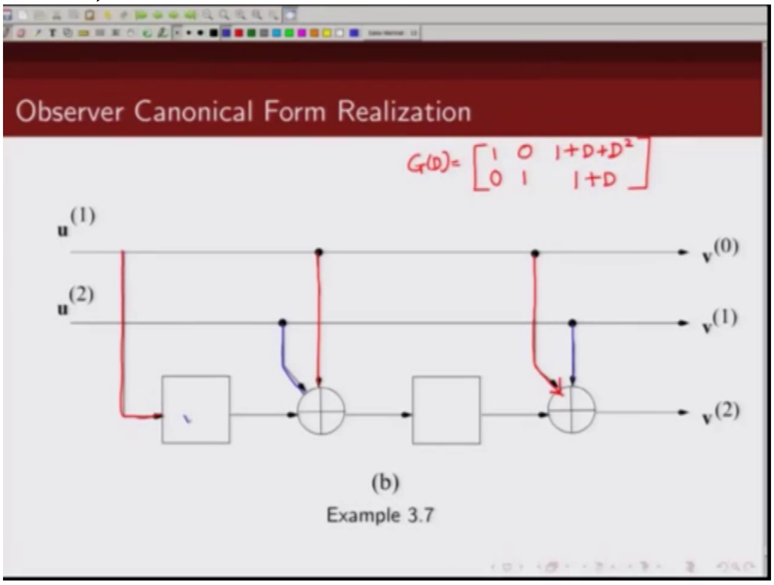

we required two memory elements. So same encoder here with two memory elements, for the controller canonical form realization we require 3 memory elements. So that brings

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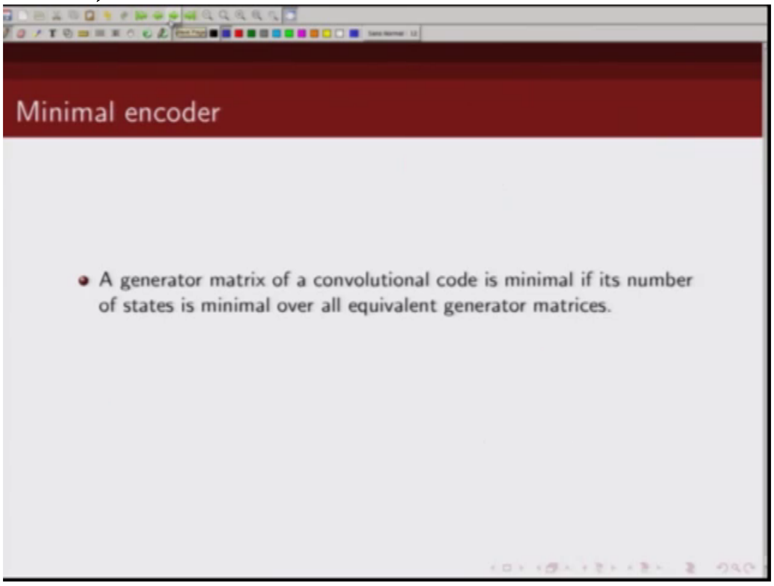

us to this notion of

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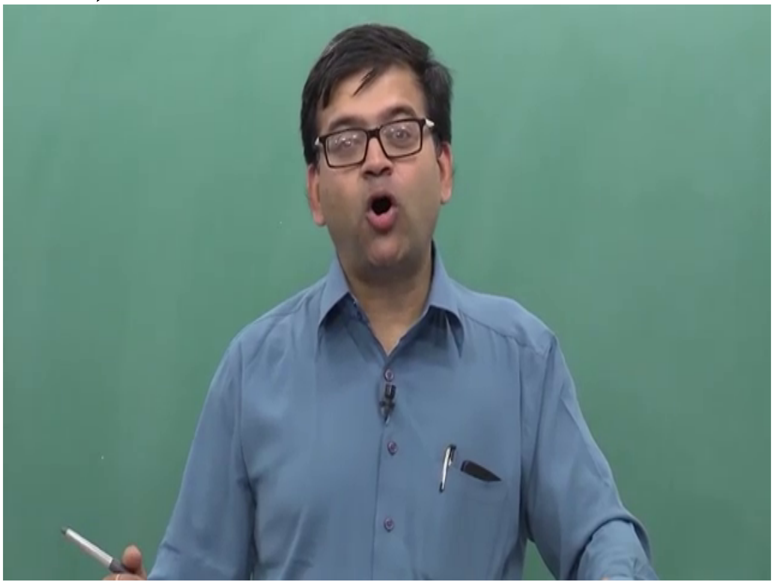

minimal encoder. We saw the same encoder; convolutional encoder with same generator matrix can be realized using 2 different ways, one that resulted in 3 memory elements, other that resulted in 2 memory elements. So we say a generator

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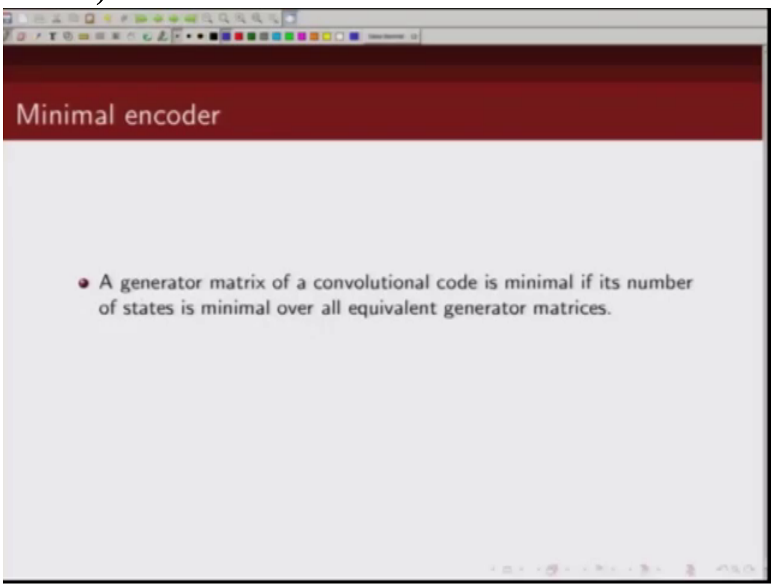

matrix is minimal if the, if its number of states is minimal over all possible equivalent generator matrix and among

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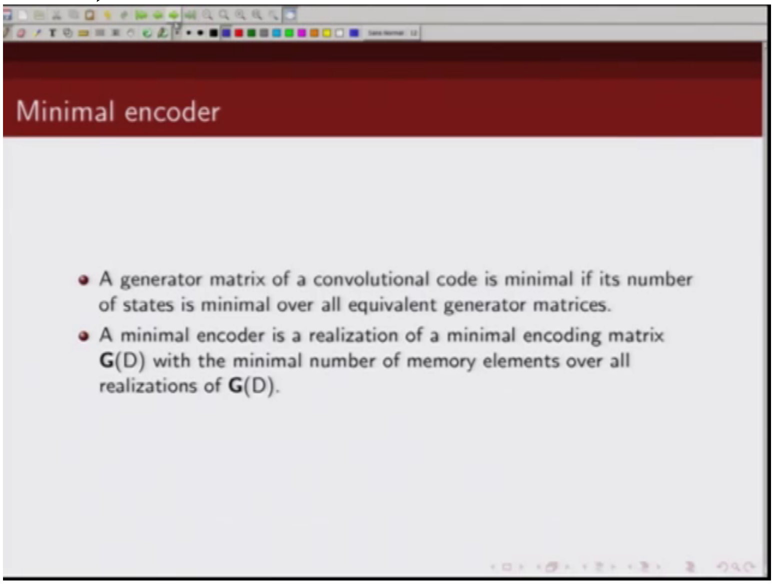

the minimal encoder matrix, a minimal encoder is basically a realization of a minimal encoding matrix which will result in minimum number of memory elements used to represent that particular convolutional encoder. So we define a minimal encoder as

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the minimal

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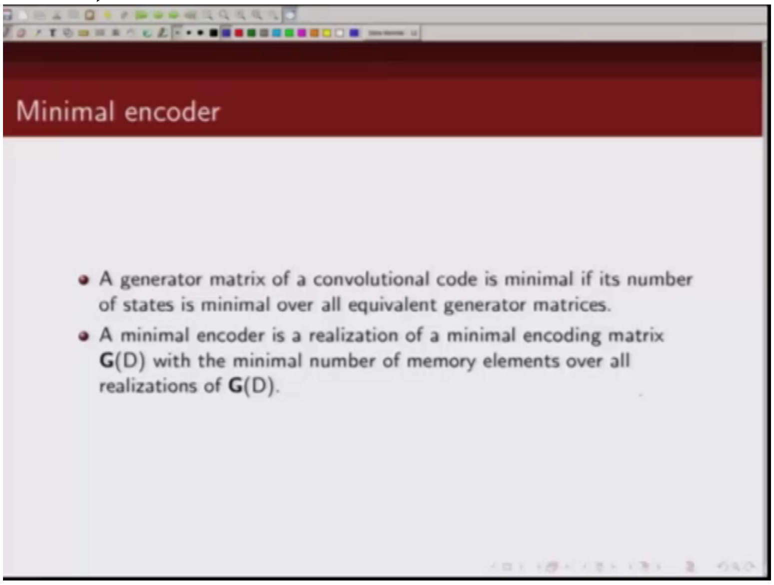

realization of a minimal encoding matrix. So the minimal encoder should result in minimum number of memory elements used to represent that particular convolutional encoder and for the example we have considered,

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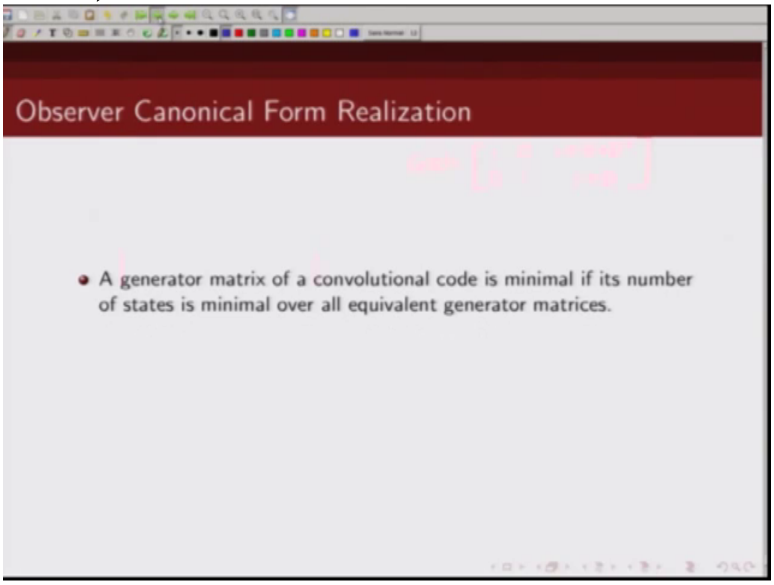

this, in this case you can see

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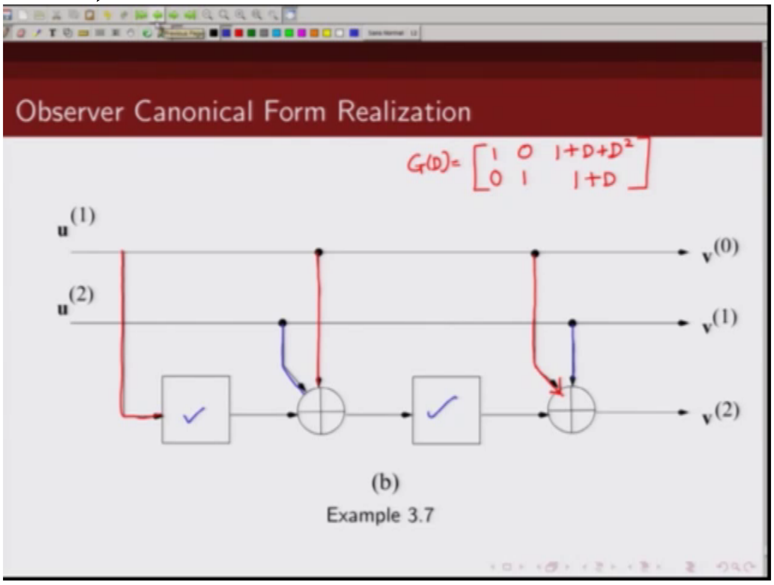

from the generator matrix the maximum degree of d is 2. So we at least need 2 memory elements to represent it and you can see the observer canonical form realization in this particular example will result in minimal encoder of this convolutional encoder. So this realization will result in minimal encoder realization for this convolutional encoder, thank you.

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