System Design Through VERILOG
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Switch level modeling
Lecture - 13
Signal strengths

Last class we have discussed about this transmission gates and then we have discussed about the non-ideal characteristics of CMOS. Normally if CMOS transistor, in that if NMOS is on, we will take as closed circuit; if it is off, we will take as open circuit, but practically there will be some resistance.

So, we have shown the resistance equivalent model of NMOS and PMOS and I have given the expressions for the resistance, ok. Now, today we will discuss about the delay times.

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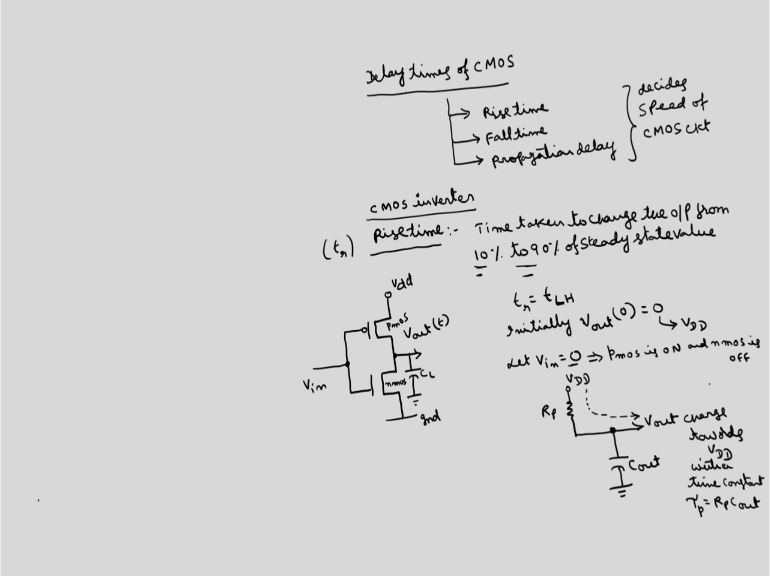

Delay times of CMOS

- Rise time
- Fall time
- propagation delay

decides speed of CMOS ckt

CMOS inverter

(t_r) Rise time :- Time taken to change the o/p from 10% to 90% of steady state value

$t_r = t_{LH}$

initially $V_{out}(0) = 0 \to V_{DD}$

Let $V_{in} = 0 \Rightarrow$ Pmos is ON and nmos is off

Vout charge towards V_{DD} with a time constant $\tau_p = R_p C_{out}$

In order to find out the speed of the CMOS circuits; so there are three important delay times are there, one is called rise time, fall time, and propagation delay. So, these three will decide the speed of the circuit. So, in order to find out this rise time, you have to consider a CMOS circuit; I will take a simple CMOS inverter. So, what is the rise time of CMOS inverter? So, once if you understand this rise time derivation of the CMOS inverter, you can do it for any CMOS circuits.

So, rise time is normally defined as the time taken to change the output from 10 percent to 90 percent of final value. For example, if I take this CMOS inverter, this is ground and this is V dd and this is PMOS transistor, this is NMOS transistor, this is V in, this is V out. Say this is a function of time and let us assume that here we have some C L.

V out is function of time. So, I will write as V out of t. So, in order to find out the rise time, the output has to change from 10 to 90 percent; means the output has to change from logic 0 to logic 1. Rise time is t r; t r is also equivalent to t low to high. So, low to high transition time; L stands for low, H stands for high. So, in order to find out this, initially we will assume that V out of 0 at 0 time is equal to 0.

Now in order to change the output from 0 to V DD. So, the input you have to apply as let input V in is equal to 0. Then what happens? Implies this is pMOS and this is nMOS. So, pMOS is on and nMOS is off. So, in the previous analysis we have assumed that, on means short circuit and off means open circuit, that is the ideal case; whereas, in practical case as we have discussed in the earlier lecture, so there will be a resistance.

So, now, the equivalent circuit here will be something like this V DD, here we have the on resistance; whereas the lower part is open circuited. So, here we are going to take the output V out. So, this capacitance will be now C out, which is sum of C L plus the capacitance of the fit, this is R p. Now, the output was initially 0, now it will charge towards V DD; this is the charging path with the time constant of tau p we will call as, this is R p into C out, this is the time at which it will charge.

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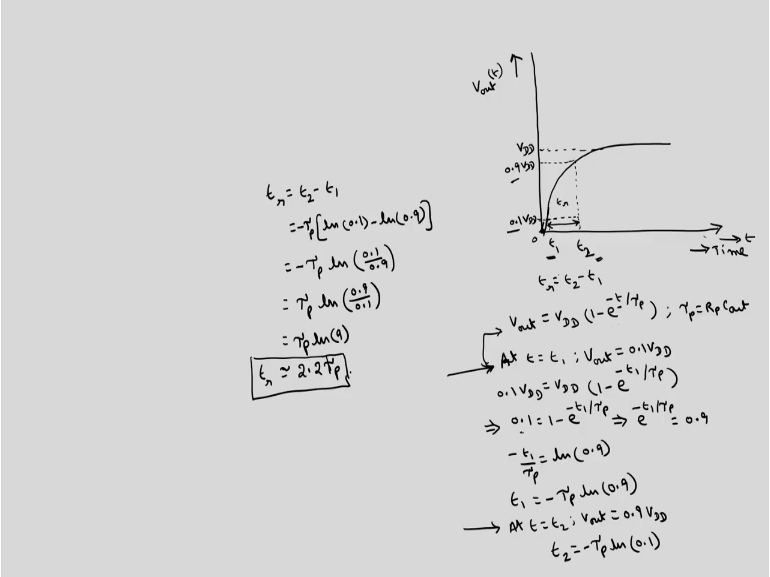

$t_r = t_2 - t_1$

$V_{out} = V_{DD}(1 - e^{-t/\tau_p})$; $\tau_p = R_p C_{out}$

At $t = t_1$; $V_{out} = 0.1V_{DD}$

$0.1V_{DD} = V_{DD}(1 - e^{-t_1/\tau_p})$

$\Rightarrow 0.1 = 1 - e^{-t_1/\tau_p} \Rightarrow e^{-t_1/\tau_p} = 0.9$

$-\frac{t_1}{\tau_p} = \ln(0.9)$

$t_1 = -\tau_p \ln(0.9)$

At $t = t_2$; $V_{out} = 0.9V_{DD}$

$t_2 = -\tau_p \ln(0.1)$

$t_r = t_2 - t_1$

$= -\tau_p[\ln(0.1) - \ln(0.9)]$

$= -\tau_p \ln\left(\frac{0.1}{0.9}\right)$

$= \tau_p \ln\left(\frac{0.9}{0.1}\right)$

$= \tau_p \ln(9)$

$\boxed{t_r \simeq 2.2\tau_p}$

Now, if I take if I draw the output waveform and say function of time V out of t. So, initially 0, after that it will rise as exponentially. So, this will be 0, it will go to V DD; so this is the steady state value is V DD, infinite time it will goes to V DD. So, initially it was 0, t is equal to 0.

Now, to define the rise time, we are going to define two points; one is 90 percent, if I call this one as t1 time, this is 0.9 V DD, which is 90 percent of the final value. And here somewhere we have 10 percent of V DD, this is 0.1 V DD. And if I call this time as t1, this as say t2; then this particular time from here to here is called rise time tr.

So, tr can be defined as t2 minus t1. So, this can be easily written. The mathematical expression for this V out as a function of time is V out of time; I am not writing function of t, it is understood. So, this can be written as V DD times 1 minus e raised to the power of minus t by tau p, where tau p is Rp, C out.

This is clear that when t is equal to infinity, e raised to the power of minus infinity is 0, 1 minus this one. So, at infinity when t reaches to infinity, this will reach to V DD. When t is equal to 0, e raised to the power of 0 is 1, 1 minus 1 0. Output is 0 here so, it will rise exponentially.

To derive this expression for the rise time. At t is equal to t1 output, V DD will be output V out will be 0.9 V DD, 0.1 V DD, at t is equal to t1 0.1 V DD. So, if you substitute this here, 0.1 V DD is equal to V DD into 1 minus e raised to the power of minus t becomes t 1 divided by tau p.

So, what is t1 expression? V DD, V DD get cancel. So, 0.1 is equal to 1 minus e raised to the power of minus t1 by tau p. And if I take this 0.1 to that side, this to this in place e raised to the power of minus t1 by tau p is equal to 0.9. If you take logarithm on both sides, minus t1 by tau p is equal to logarithm to the base to 0.9. So, t1 is equal to minus tau p ln 0.9.

Similarly, to get that t2, this is the case at, this is the at t is equal to t1, this is a expression. Similarly, at t is equal to t2, V out is equal to 0.9 V DD. If you do in a similar manner, you will get t 2 as minus tau p ln 0.1. Now, you will see that this will be 0.9; so if we subtract from 1, it will be 0.1.

Therefore, what is t r is equal to t2 minus t1, this is equal to minus of tau p is also common minus tau p is common, ln of t2 is 0.1 minus ln 0.9; this is equal to ln a minus ln b is ln a by b, ln b.

And if I take this minus sign, this division will be reversed; this is equal to tau p ln 0.9 by 0.1; this minus sign I have removed. I have changed this order, this is equal to tau p ln 9, ln 9 is approximately equal to 2.2. So, this approximately equal to 2.2 tau p. So, this is the rise time of CMOS inverter.

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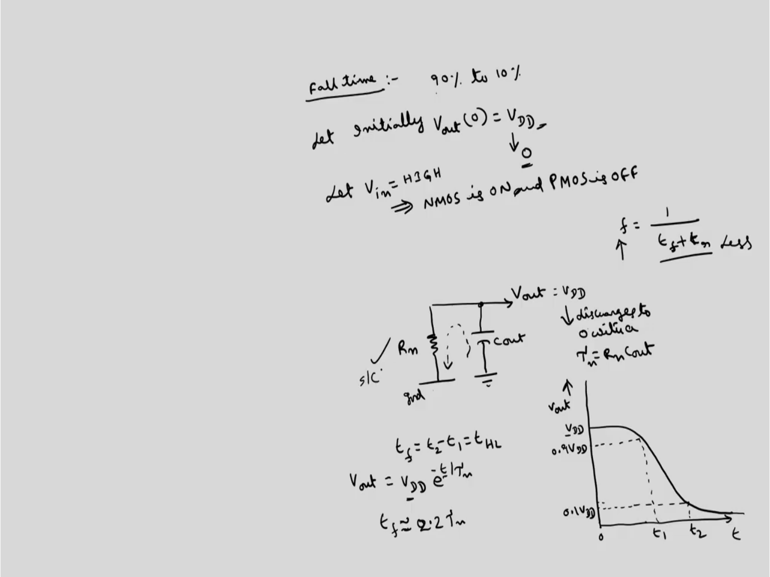

Fall time :- 90% to 10%

Let initially $V_{out}(0) = V_{DD}$ ↓ 0

Let $V_{in} = \text{HIGH}$
$\Rightarrow$ NMOS is ON and PMOS is OFF

$f = \frac{1}{t_f + t_r}$ less ↑

$V_{out} = V_{DD}$ ↓ discharges to 0 with a $\tau_n = R_n C_{out}$

$t_f = t_2 - t_1 = t_{HL}$

$V_{out} = V_{DD} e^{-t/\tau_n}$

$t_f \simeq 2.2\tau_n$

Similarly, to find out the fall time, fall time is defined as a time taken to change from 90 percent to 10 percent, this is the reverse of that of rise time. So, to change from 90 percent to 10 percent, initially we will assume that, V out of t is equal to or 0, V out of 0, is equal to V DD. Now, I want to make this to 0. So, in order to get to 0, we have to make let input is equal to V DD; when input is high, it implies NMOS is on, PMOS is off.

So, what will be equivalent circuit? PMOS is off means, off resistance is infinite, so it will be open circuited. So, the only lower part will be there. So, this is the capacitance, this is the output point V out, this is ground, this will be C out, this is Rn. Now, this is the discharging path. So, the output was initially at V DD; now it will discharge to 0 with a time constant of tau n is equal to Rn C out.

So, if you draw the output characteristics versus time. So, initially output y it will be V DD; then it will change to. So, this is V DD and 90 percent of this one is this 0.9 V DD; we call this as some time and 0.1 of V DD is somewhere here, this you call as t2, this call as t1, then fall time is t2 minus t1, this also can be called as the time to change from high to low.

So, what will be the expression for this one? So, you can derive the expression in a similar way to that of rise time. So, this V out expression will be as a function of time is V DD into 1 minus will not be there; simply e raised to the power of minus t by tau n. Because at t is equal to 0, what is the value t is equal to 0? E raised to the power of 0 is 1 V DD. So, this is V DD, at t is equal to infinity, 0; this will be just to 0 at infinity.

So, we can derive in a similar manner, the t f expression also will get approximately as 2.2 tau n; both the expressions are same, the only difference is in time constant. So, the time constant of rise time fall times will be different. Now, once if you know this rise time and fall time; then the frequency at which the MOSFET can operate is given as 1 by t f plus t r, this is the frequency at which the MOSFET can operate.

So, in order to operate the MOSFET at higher speeds, higher frequencies; if you want the more value, this should be less. So, means the time constant should be less; if time constant is less, speed of the CMOS circuit is more. So, in order to represent, there is another parameter called propagation delay.

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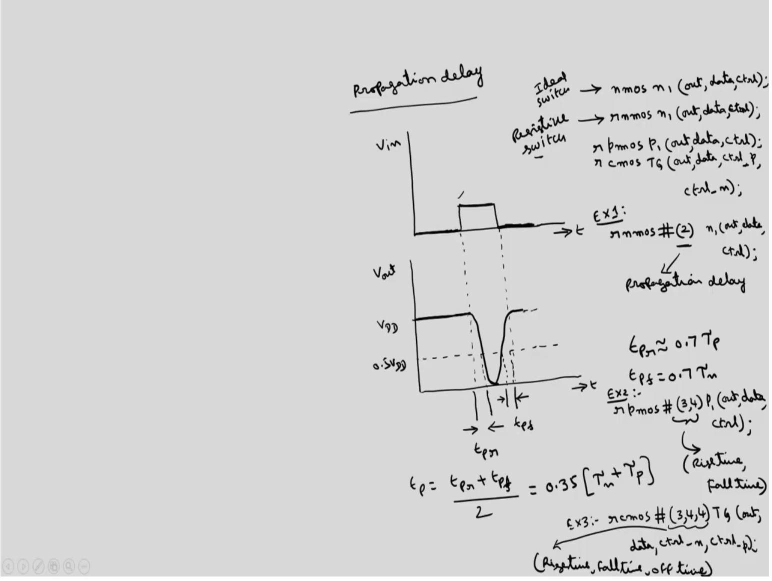

Ideal switch → nmos n1 (out, data, ctrl);

Resistive switch → rnmos n1 (out, data, ctrl);

```
rpmos p1 (out, data, ctrl);
rcmos TG (out, data, ctrl_p,
          ctrl_n);
```

Ex1:

```
rnmos #(2) n1 (out, data,
          ctrl);
```

propagation delay

$t_{pr} \simeq 0.7\,\tau_p$

$t_{pf} = 0.7\,\tau_n$

Ex2:

```
rpmos #(3,4) p1 (out, data,
          ctrl);
```

(Risetime, Falltime)

$$t_p = \frac{t_{pr} + t_{pf}}{2} = 0.35\left[\tau_n + \tau_p\right]$$

Ex3:-

```
rcmos #(3,4,4) TG (out,
          data, ctrl_n, ctrl_p);
```

(Risetime, falltime, off time)

So, these three can be represented using some syntax in Verilog code, that is why I am discussing this. If pulse step of the input is applied; say this is 0, this is 1, again this is 0, if this is the input as a function of time. Then what will be the output of the inverter? So, when the input is 0, output will be V DD. So, this is V DD, up to here this is V DD.

When input is 1, output will be 0; but that 0 will come slowly, because this is the practical case. So, this will come like this. So, like this, then again it will rise; it will come with some slope and again it will rise to V DD, because here it is 0, this will be V DD again.

So, somewhere here the 50 percent of V DD is there, 0.5 V DD; this difference, this is the point where this V DD is there, this is the point where it reaches the 50 percent. So, this gap is called as propagation delay of rise time. And similarly this 50 percent this value and where it reaches to the full value V DD. This is 50 percent and here it reaches to the V DD. So, this value is called tp fall time. Then t p is called average of tpr plus tpf divided by 2.

Now, if we derive the expression for this tpr and tpf in a similar way to that of the rise time and fall time. We will get this expression as tpr is approximately equal to 0.7 times tau p, tpf is equal to. So, the expression for the rise time is p and this one is 0.7 times tau n. Therefore, this will be 0.35 times sum of the time constant of NMOS time constant of PMOS. This is the expression for this total propagation delay.

Now we have three primitives. So, earlier we have discussed about the three primitives in ideal case, that we have discussed as nMOS, the general structure is some n1 out data control; whereas in non-ideal case, that is called resistive switches, you see the ideal switch, this is corresponding to ideal switch.

If I take the resistive switch, we will get rnMOS n1 out, data, control; the only difference between nMOS and rnMOS is. So, here we are going to represent with the resistive type of equivalent circuit. Whereas in case of just nMOS, this will act as a short circuit, that is the difference.

Now in order to represent the delay, normally you can represent delays; similarly you can write for this pMOS also, we have similarly we have pMOS is for ideal, whereas r pMOS is for resistive. You have similarly r CMOS p1 out, data, ctrl control. And CMOS is normally we will get TG transmission gate, we have discussed in the earlier lecture also. So, this will be out, data; we have two controls, control underscore p, control underscore n, ok. So, these are the three primitives for the resistive switches.

Now in order to represent this rise time, fall time, and propagation delay; we can use a pound type of the symbol. So, if I write say rnMOS pound type of the symbol and if represent within the parentheses from 2; then the remaining is same out, data, control. This is one example, if we have only one value; then this represents propagation delay.

On the other hand, if we have something like r pMOS and if you have two values; if you have something like 3, 4 p1 out, data, control. So, these two values represents, the first one is rise time and then second one is fall time. Sometimes you can represent three values also; another example, this is example 1, where we have only one value; this is example 2, we have two values.

Example 3, we can have three values, say rCMOS pound symbol, we have 3, 4, 4; we have some name of this TG out comma data, control underscore n, control underscore p. So, here these three value represents this is rise time, fall time, then off time; this is how one can represent this rise time, fall time, or propagation delays in case of CMOS circuits.

Till now we have discussed about the various primitives of switch level modeling. So, one is simply nMOS, rnMOS, pMOS, rpMOS, CMOS, rCMOS and then we have supply 0, supply 1. So, these are the various primitives that we have discussed till now. So, there are some more primitives, such as pull up and pull down.

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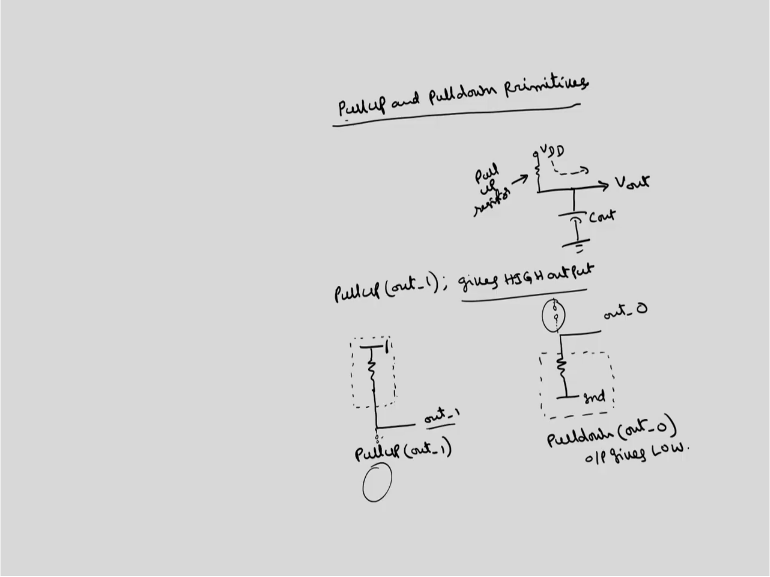
Pullup and Pulldown Primitives

Pullup (out_1); gives HIGH output

Pullup (out_1)

Pulldown (out_0)
o/p gives LOW.

So, what are these pull up and pull down? As we have discussed in the earlier lecture, when the output charges, if I take this CMOS inverter; so if it charges through this pMOS, which is connected to V DD, this capacitor, C out, this output will charge to this one. So, this resistance is called pull up resistor.

So, in order to represent this pull up and pull down, normally we can define this as pull up; if I represent with out_1, this will give high outputs. So, this will be something like, here we have connected high and there will be resistance; so this will be connected, this is 1, logic 1, this is in a block box. If you have this in a block box and if we take this point; if I write this as out underscore 1, if I write simply pull up out_1, this will give high output.

Similarly, we have pulled down out; so which will be something like if we take output here and if you have resistance and if I connect to ground, this if I take as a block box, this will be out 0. If we write pull down out 0, so this finish the output will gives low value; the upper circuitry here I will assume that this is the open circuit type of thing, similarly here the lower circuit will be something like open circuit.

So, if I connect this in a complete circuit; depends upon this upper circuitry of this and lower circuitry of this, this output will vary, this can be either 0 or 1. So, simply I will use pull up out or pull down out; instead of 0 and 1, I will write pull up pull down out. This will be better understood, if I consider an example.

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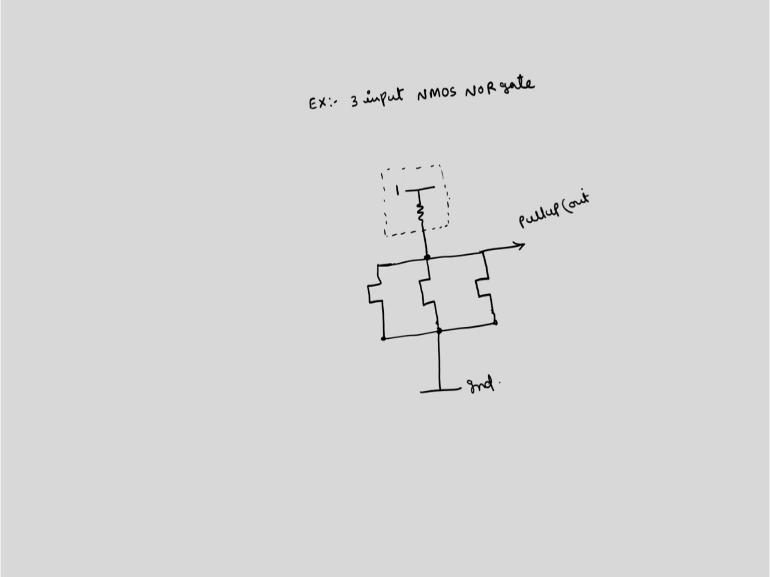

Let us take a 3 input NMOS NOR gate, we can also call it as pseudo NMOS. Here we are not going to use p type MOSFETs; because this p type MOSFET the equivalent circuit will be represented by the pull up resistance. So, the circuitry for this one will be, this is pull up resistance, then we have 3 input NOR gate.

This we how to connect to the ground, this one will be connected, this will be in block box. So, here we are going to take the output and this is pull up, out; we can also call as just simply output V out.

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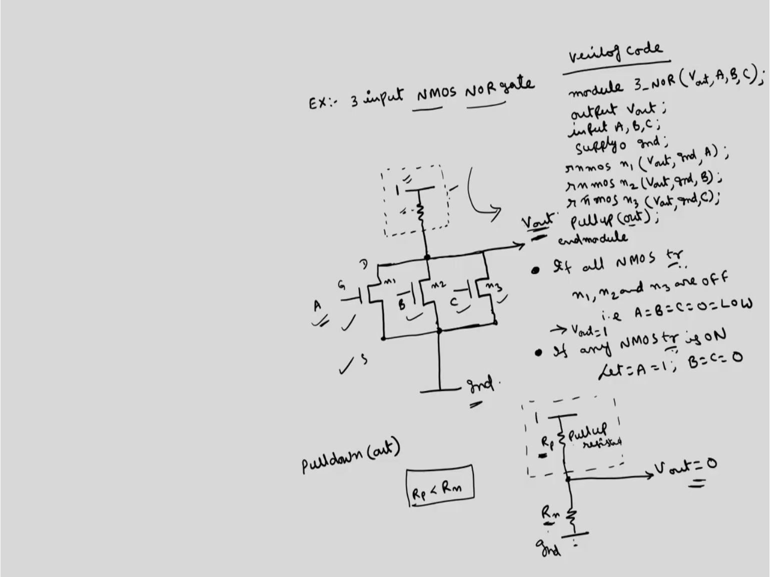
EX:- 3 input NMOS NOR gate

verilog code

```
module 3_NOR(Vout,A,B,C);
output Vout;
input A,B,C;
 supply0 gnd;
rnmos n1(Vout,gnd,A);
rnmos n2(Vout,gnd,B);
rnmos n3(Vout,gnd,C);
pullup(out);
endmodule
```

- If all NMOS tr
  n1, n2 and n3 are off
  i.e A=B=C=0=LOW
  → Vout=1
- If any NMOS tr is ON
  Let: A=1; B=C=0

pulldown(out)

$\boxed{R_p < R_n}$

This is NMOS, if you have three inputs; say A, B, C. Here, the thing is as long as this 3 NMOS transistor, if I call this one as n1, n2, n3. If all NMOS transistors n1, n2 and n3 are off means A is equal to B is equal to C is equal to 0 or low. Then what happens? This entire circuit will be open circuited; this output will be connected to this one.

So, this will be, because this is pull up resistance; the output becomes output to pull up to 1, output will be 1. So, if any one of these input is on. Let A is equal to 1, B C is equal to 0; then what will be equivalent circuit? This will be on, so this will have some resistance; this will have some resistance of this network, this is pull up resistance.

So, the equivalent circuit will be this is 1, this is pull up resistance. Now, this point here also we will be having some resistance connected to ground, this is where you are taking the output. So, in this case what is V out? V out will be 1, because this V out will be pulled up.

Whereas, in this case V out will be; so this is Rn and this is some pull up resistance, say some Rp. This is not p type, if I use the p type; then equivalent circuit we can write this one, but this is actually pseudo NMOS, only NMOS transistors we are using, there is you know PMOS transistors here.

So, here what will be the output now? Here also there is some resistance, here also some resistance. So, normally we will choose this pull up resistance, such that this is less than Rp is less than the on resistance of NMOS. So, that the output will become 0, that is what the operation is required for the NOR gate.

So, you will choose this pull up resistance, such that R p is less than R n. In that case, the one which dominates, that will come to the output; Rn dominates, Rn is connected to ground, so output becomes 0. So, this is how we can pull up or pull down this network and the Verilog code for this circuit is, we can write the Verilog code as module; you take 3 underscore NOR gate some name, the inputs are output is only V out, inputs are A, B, C; output V out, input A, B, C.

So, one important point that you have to remember is, no need to define the supply 1, only supply 0 ground is enough. And no weights are required, because these three points are connected to V out, these three connected to ground. Then you can define nMOS, we can also write down rnMOS also; because this is not ideal n1.

What is the output and input? Output, data and then control; control is A, output is drain source gate, output is V out, data is ground, control is A. Similarly, rnMOS n2 V out, ground and B; similarly, rnMOS n3 V out, ground, and C. Then the output will be pull up out. So, this out will be 1, if all these three inputs are 0s; otherwise the output will be 0, end module.

So, in a similar manner you can explain where we have about pull down also; I have explained about the pull up with example. So, in a similar manner, we can use pull down also, pull down out. These are the other two primitives. Then we have the bidirectional switches also. Till now, we have discussed about the unidirectional, the current flows from drain to source only. We can have bidirectional switches also.

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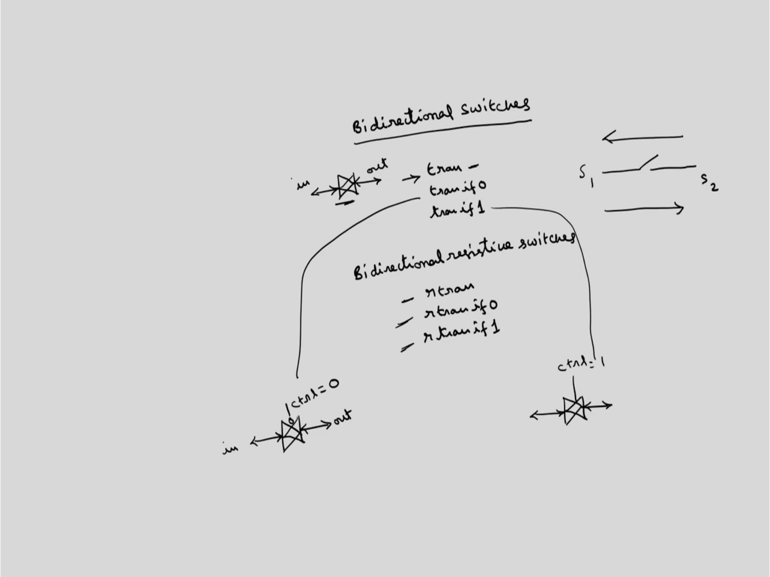

The primitives for these bidirectional switches are tran, tran if 0, tran if 1; of course this you can use with r also. So, that you can use for the resistive type; this is without this the ideal switches, we can have three resistive switches also, bidirectional resistive switches r tran, r tran if 0, r tran if 1. So, there are totally six primitives on bidirectional switches.

As the name implies, so the data can flow from input to output or output to input; if you have this s1 and if you have a switch, this is s2, data can flow from s1 to s2 or s2 to s1, depends upon the position of the switch. So, in case of tran, directly switch is closed, data can flow from both the directions. Trans if 0, so the switch will be closed if control signal is 0, there will be a control signal here.

So, this will be something like just a simple switch, we have some simple switch; this is the symbol for the tran with input and output. Whenever you write this tran, the switch will close; so data can flow from input to output or output to input. Whereas, in this case tran 0 and tran 1; tran if 0, we can have a switch, this switch will be closest whenever if there is a control signal which is, if control signal is 0, switch will be closed.

So, data will flow from input to output or output to input. Yes, for tran 1 its reverse, there is a control signal without any bubble; if control signal is 1, then there will be a data transfer, otherwise the switch will be open circuited. So, instead of open circuit and short circuit, if you have resistance; then we will use this r tran, r tran if 0, r tran if 1. So, these are three some bidirectional switches and there are some six primitives related to bidirectional switches. There are some signal strengths. So, we can have totally eight different signal strengths.

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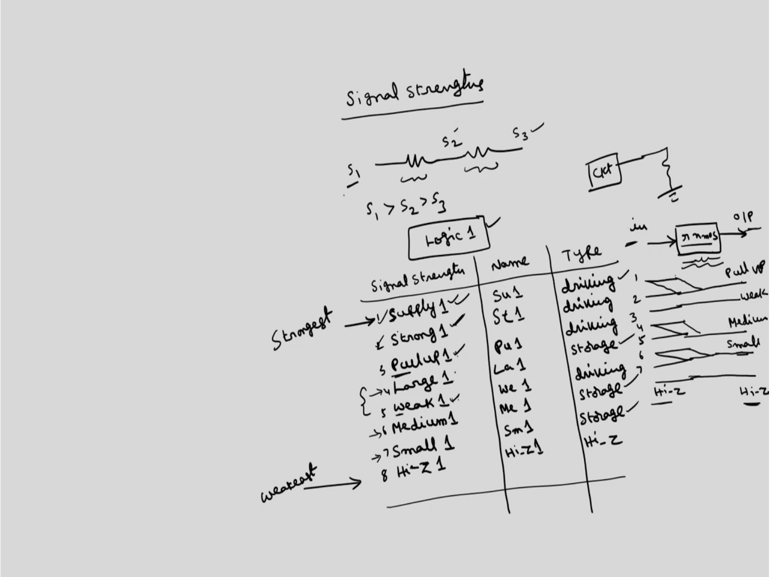

Signal strength	Name	Type
1 Supply 1	Su 1	driving
2 Strong 1	St 1	driving
3 Pullup 1	Pu 1	driving
4 Large 1	La 1	storage
5 weak 1	We 1	driving
6 Medium 1	Me 1	storage
7 Small 1	Sm 1	storage
8 Hi-Z 1	Hi-Z 1	Hi-Z

So, as you know that in case of resistive switches, here the signal level is something like s1, signal level is s2. Similarly, if I pass this s2 to some other resistance s3; then in terms of the signal strength, s1 is greater than s2 is greater than s3. Because s1 corresponds to some voltage level; there will be some voltage drop across this resistance, so s2 is less than s1.

So, after that there is some more voltage drops. So, s3 is less than s2 and so on. So, when the signal propagates through the resistances, the signal strength will decrease because of the voltage drop across the resistances.

So, totally we can have which is the strongest signal, which is the weakest signal. So, like that we have total eight different signal strengths, and corresponding to each signal strength there is some name; then we have what type of signal is this. So, we have total eight such signals.

So, the strongest signal is called as supply 1, this is for logic 1; I am representing this for logic 1, similarly you can obtain for the logic 0 also. For logic 1, the strongest signal is called supply 1, which is V DD; if we call it as Su1, I will come to that type later. Then supply one after that, pull up 1, Pu1 is the next signal strength. Then we have strong 1, these two are reverse; this is strong 1, this is pull up, strong 1, St1.

Then we have pull up 1, then large 1, weak 1, medium 1, small 1; then high impedance 1, z stands for impedance. This is called as Pu1, La1, We1, Me1, Sm1, Hi z1, these are the names. This is the strongest and this is weakest, its high impedance; high impedance is nothing, but open circuit, this is floating.

So, the type is, we can use this supply 1 for driving; this also you can use for driving, this you can use for storage, this you can driving, this is storage, this is storage and this is high impedance, high impedance is floating just. So, the meaning of this one is, if the output of a circuit in some circuit is there; if this output is at supply 1 or strong 1 or pull 1, even if it is weak 1.

So, in all these cases, this can be used to drive some other loads; some other circuit if you want to drive this, we can use. Whereas if I want to store as a logic 1, this largest signal strength is also enough to store. Similarly, medium and even small also is enough to store as a logic 1; whereas high impedance is not enough, this will be almost like open circuit.

So, these are the signal strengths. Starting from supply 1, after that strong 1, pull up 1, large 1, weak 1, medium, small and high impedance. Suppose if I connect to r nMOS, this is corresponding to logic 1. Similarly, we can write for the logic 0, this is input output. Suppose if the input levels are in the same order, this is supply strong; if these two are connected, then pull up, large, small, weak, medium, small, then high impedance.

The output is also high impedance, this is high impedance, output is also high impedance; if I apply to the r MOS circuit, if input is high impedance, output is also high impedance. Whereas, here this is the order that I have given. If I call this one as 1, 2, 3, 4, 5, 6, 7, 8.

So, the levels 1 and 2, which is the supply 1 and strong 1 will give pull up; these two will give to the pull up as the output. If I give the input as either supply 1 or strong 1, the output will be; because in r nMOS there will be resistance, there will be some voltage drop. So, because of that, these two levels will come to pull up.

Similarly, this third level pull up will come to weak. If I give the input as pull up, output will be weak. If I give input as this is 3rd level, 4th is 4th and 5th; that is if I give the large and weak as the inputs, then you will get output as medium. And if I give this medium and 6 and 7, medium and small; medium and small if I give, so you will get output as small, for high impedance, high impedance.

If I take the r nMOS circuit, the input and output levels; so the first two level supply and the strong will be reduced to pull up, and pull up and large third and fourth will be reduced to weak, large and weak will be reduced to medium, and then medium and small will be reduced to small in case of r NMOS.

So, here about some signal strength; when the signal propagates through the resistive switches, the signal levels will decrease. So, this is about this the signal strengths and the modeling of these CMOS circuits using switch level.

Thank you.