Microprocessors and Interfacing
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Lecture – 29
Initialization command Words of 8259

Okay, So in the last class, we are discussing about a 8259. So, I have explained the a flowchart of the initialization resistors as I have discussed that 8259A uses 2 to 4 initialization command words ok. So, in that the ICW1 if I take the format of ICW1 initialization command word 1.

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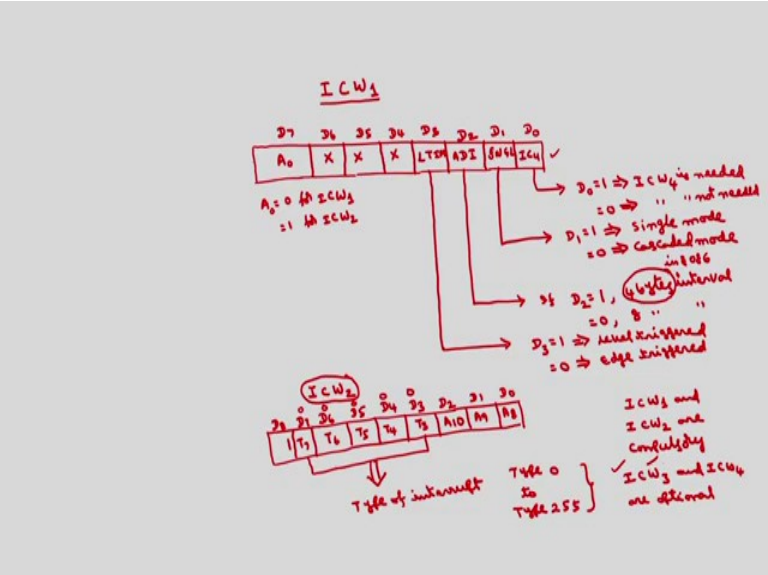

So, the format is. So, the last bit D 0 bit of this one will decide whether ICW4 is needed or not. This is IC4. So, this will decide if this bit is equal to 1 if we call this one as D 0 bit, if this D 0 bit is equal to 1 implies ICW4 is needed, if this is equal to 0 implies ICW4 is not needed. As I have discussed in the flowchart also, this can be ICW4 can be is a optional one.

Then the second bit D 1 bit will be here, either we say single mode or cascade mode SNGL, this if D 1 bit is 1 implies single mode as I have discussed this 8259 can operate in single mode as well as cascaded mode. So, in single mode we can have 8 different devices can be connected to 8259 whereas, in cascade 64 devices can be connected. I

will discuss how this 8259 will be cascaded to service 64 different IO devices. Then we have, address interval ADI.

So, the address interval of different types of the IRs we can have either 4 or 8 intervals, as I have discussed in the last class also. So, this if this bit is equal to this is D 2 bit if this D 2 bit is equal to 1. So, there will be interval of 4 bytes. If this is equal to 0 then 8 bytes interval, but in case of 8086 it is only 4 bytes interval so, this D 2 will be you have to set to 1 in case of 8086.

The next bit is LTM level triggered or edge triggered, as I have told one of this important feature of this 8259, is it will accept both edge triggered as well as level triggered interrupts. So, if this is one level triggered this bit D 3 if D 3 is 1 implies level triggered, if D 3 is 0 edge triggered and the remaining 3 bits will be used for only these 8085 whereas, in 8086 they will be do not cares.

This is D 4 D 5 D 6 D 7, in case of 8086 they are do not cares whereas, in 8085 they have some different purpose, but here we are discussing about only 8086 they are do not cares and D 7 bit is A naught, A naught of this 8259 we can see that one of the pins of 8259A is A naught and for ICW1 this A naught is equal to 0, this is equal to 1 for ICW2.

So, this is about the format of the first initialization command word ICW1 so, this will decide whether ICW4 is required or not and then whether we are going to operate in single mode or cascaded mode, and what will be the interval between the 2 successive interrupt vectors 4 bytes or 8 bytes, but in case of 8086 by default 4 bites.

And it will decide whether the interrupts are level triggered or edge triggered. So, this information will be supplied by this initialization command word 1. Then coming for this second initialization command word ICW2. So, the format of this ICW2 is, so this is also 8 bit register D 0 to D 7, D 0 D 1 D 2 D 3 D 4 D 5 D 6 and D 7.

So, the last bits are A 8 A 9 A 10 A 8 status of A 8 A 9 and A 10. Then the next bits are T 3 T 4 T 5 T 6 and as I have told D 7 bit is 1 for ICW2. So, there will be one more bit which is called T 7 this is 9 bit in fact, D 7 D 8. So, these bits in case of 8086 will decide the type of interrupt, as we know that in case of 8086 this will decide the type of interrupt. So, we know that in case of 8086 there are 256 types of the interrupts type 0 to type 255.

This we have discussed while discussing about the interrupt system of 8086. So, in order to have 256 different types we require 5 bits. So, these 5 bits T 3 to T 7 will be used for selecting the type of the interrupt. So, if it is type 0 all bits will be 0 this bits will be 0 0 0 0 0 so, that will get type 0 if all are 1s we will get type 255 in between for different combinations, we will get different types of the interrupts will be selected.

Whereas this A 8 A 9 and A 10 will be used for generating the address of this 8259, that we will discuss while discussing about the interfacing of 8259 to 8086, so, this is ICW2 format. So, this ICW1 and ICW2 are mandatory compulsory, as it is clear from the yesterday's flow chart also. Whereas, ICW3 and ICW4 are optional. ICW3 will be used for cascading mode, which is clear from the yesterday's flow chart. So, in this ICW1 we can decide whether ICW4 is required or not.

So, before going to discuss about this ICW3 which is required in cascading mode only I will discuss how the cascading of 8259s will be performed.

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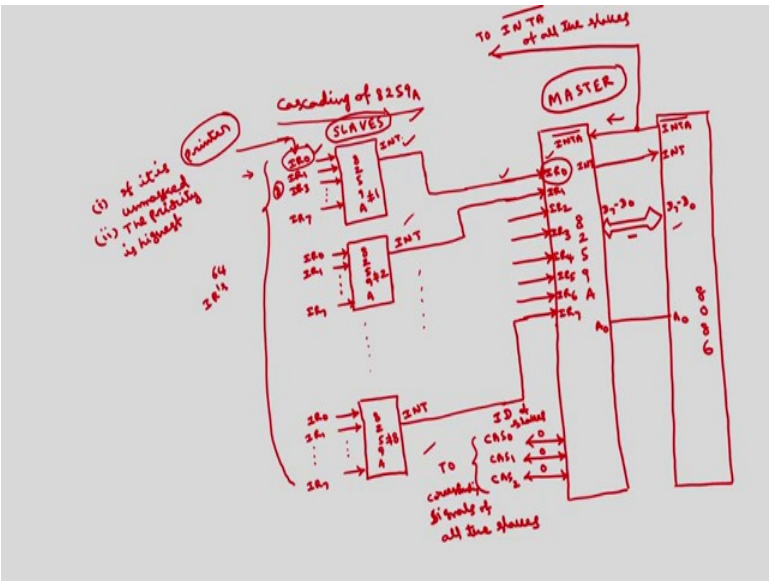

So, I will first discuss about the cascading of 8259s and then I will go to ICW3. So, here in this case one master has to be present if I call this one as a master 8259, so we know that this will be having IR 0 to IR 7 interrupt requests, IR 0 IR 1 IR 2 IR 3 IR 4 IR 5 IR 6 and IR 7, and there is 1 INT signal, this INT signal will be connected to the INT of 8086. This is your 8086 this INT is connected to INT of 8086.

So, this INTA bar will be connected to INTA bar will be connected to INTA bar of 8259. So, I am showing the connections of only the important signals how this cascading will be performed, then we have this A 0 line of this one is connected to A 0 and data bus will be connected together. We have D 7 to D naught this will be connected to D 7 to D naught of the lower order 8 bits of 8086 address data bus.

Then if I use another 8259A. So, with this also will be having 8 different IRs, IR 0 to IR 7. So, we can connect one more, like that I can connect a maximum of eight 8259As, this also will be having 8 different IRs IR 0 to IR 7, like that if I call this one as number 1 if I call this as number 2 like this number 8, this also will be having IR 0 to IR 7.

Now, the INT of this signal, this 8259A so, each 8259A will be having one INT. So, this INT will be connected to IR 0 of this or to any of this IRs of 8259A master this is called master, and these are all called slaves. And the INT of master is connected to 8086. So, the INT of this one is connected to IR 1 so on up to INT of the 8th 8259 will be connected to IR 7 of master.

Now, totally how many interrupt lines are there interrupt request lines are there? This is having 8 this is having 8 and so on we have 8 such devices total we can have 64 interrupt request lines. So, I can connect 64 different devices, such as printer's IO keyboard and all ok. Now the process is here, so whenever if any particular interrupt occurs over any of these slaves say here at IR 0 some interrupt occurs through some printer.

So, then under two conditions this interrupt will be accepted one is this IR 0 should be non masked so under two conditions IR 0 should be whatever the interrupt that we are going to use it should be unmasked. How to mask and all will discuss in this initialization register if it is unmasked, is one condition and if the priority of that particular IR should be high, priory is highest.

So, what happens is this will recognize the request placed by the printer then this INT signal will be activated so, this INT signal is connected to one of the interrupt request of master.

Again the same conditions here if IR 0 of the master is not masked which is unmasked and the priority of IR 0 is highest among all the serviced interrupt then this master will place a request through INT to the 8086. Then 8086 after completing the execution of the

current instruction it will send a pulse on INTA bar of course this INTA bar is connected to the INTA bars of all the 8259s. So, this will be connected to INTA bars of all these slaves.

So, as I have discussed in the last class also, so, this INTA bar consists of 3 pulses. So, first INTA bar pulse, for the first INTA bar pulse this master will enable whereas, this slaves simply neglects the first INTA bar cycle. So, in response to the first INTA bar cycle what the master will do is. So, the master will place the ID of this corresponding slave each slave will assign some ID, I will discuss what is the idea of this slave in initialization command word 3.

So, each I mean slave will be having some ID that ID will be informed through CS lines. There are 3 lines called CAS 0, CAS 1, CAS 2. This will be connected to the corresponding CAS lines of all the slaves, corresponding signals of all the slaves.

So, in the response to the first INTA bar acknowledgement cycle this master 8259 places ID. So, normally this ID is if this is connected to IR 0 this ID will be 0 0 0 if this request is through IR 1 this will be 0 0 1 and so on.

So, this ID will be placed on this CAS0 to CAS2 so, which will be received by all these slaves the slave which has initiated this interrupt that will enable now it will respond to the second and third cycles of INTA bar signal. So, the first INTA bar cycle will be just neglected by this slave, which is initiated the interrupt request. Whereas, after receiving this CAS0 to CAS2 the ID ID of that particular slave then the corresponding slave will respond to the second or third pulses of INTA bar cycle.

So, in second and third what it will do is? So, this will place the type of interrupt. So, which type of interrupt you want to perform by using this IR 0, as I have told there are 256 types of the interrupts so that corresponding information has to be placed on to the data bus, the data bus of all these slaves will be connected to together to the 8086.

So, on the lower order 8 bits of this is 8086 data bus it will receive the type of interrupt that is to be performed so, based on these type of interrupt. So, the micro bus will branch to the interrupt service sub routine whose address will be calculated based on the type of interrupt.

I have discuss it this interrupt vector table correspond to each I mean type we have 4 locations. The locations of CS core segment and the location of instruction pointer. So, those values will be stored in an instruction interrupt pointer table so, correspond to that address the micro processor will switch over to that location.

So, that is the procedure of this, cascading of 8259 now based on this cascading of 8259 operation I can discuss now the initialization command word 3 and initialization command word 4, initialization command word 4.

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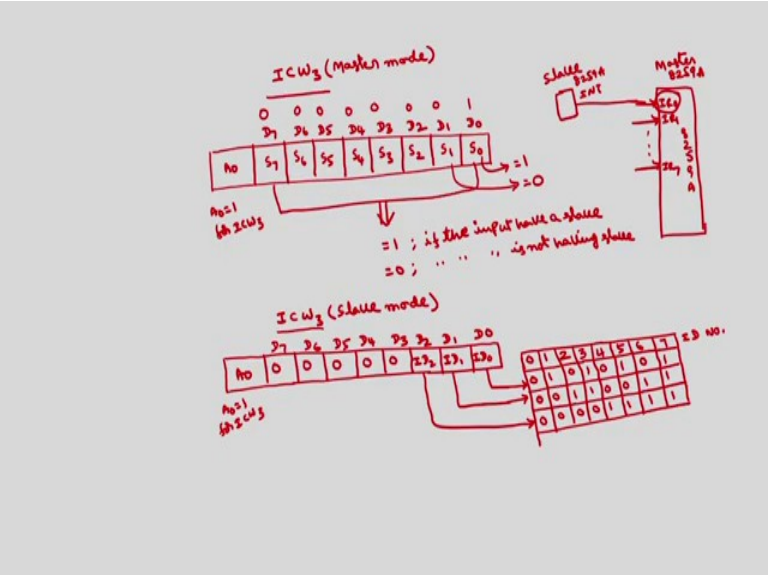

So, if I take the format of initialization command word 3. As I have discussed in the flow chart ICW3 will be used only when cascading mode is performed. So, this ICW3 we have two different ICW3s, one for the master mode another for the slave mode.

So, I will first discuss about the ICW3 format for master mode. So, in ICW3 the last bit will be S 0 S 1 S 2 S 3 S 4 S 5 S 6 and S 7. And this is A 0 and A 0 should be 1 for ICW3. This is D 0 D 1 D 2 D 7, this is the additional information this is actually in fact, not a pin of this 8259 format. So this is not included in the register of this one that is why this is 8 th location.

So, these pins, means all say 8 pins this will be 1 if the input has a slave. Now, I will explain what is meant by this. 0 the input is not having slave, thus we have just now discussed about that cascading of 8259. So, this is master 8259. So, this is IR 0 IR 1 so

on up to IR 7. If I connect a slave to this IR slave 8259A this is INT of this will be connected to IR of master. Then this is 0 bit will be 1 indicates that there is a slave connected to IR 0.

If this IR1 is there is no slave here connected then IR1 bit will be S 1 bit will be 0 indicates that there is no slave. If I assume that only one slave is there which is connected to IR 0 then this bit will be S 0 bit will be 1 remaining all bits will be 0s. So, depends upon whether this IR 0 to IR 7 of master 8259 is connected to slave 8259 or not these particular bit S 0 to S 7 will have a status of logic 1 or logic 0, 1 means the corresponding IR is having a slave, 0 means the corresponding IR is not having a slave.

This is for ICW3 in master mode, ICW3 in slave mode, the format is; this is ID0 to ID2, then we have all 0s this is A0 as I have told this A0 is not a part of this resistor the resistor length is only 8 bit D 7 to D naught. This is additional information A 0 is equal to. So, A 0 is one of the pins of 8259 this is one for ICW3, and this is 0 for only ICW1 remaining it will be 1. So, as the name implies the ID as I have told the ID will be generated in response to the first INTA bar cycle the master will generate ID.

So, the ID number will be decided by these 3 bits. So, the ID number will be here, if these 3 bits are 0 0 0 the ID number is 0, if these 3 bits are we have 8 combinations 0 0 1 this ID number is 1 and this is 0 1 0 ID number is 2, 0 1 1 ID 2 is MSB ID is 3, like that 4 5 6 7 this is ID number. This will be 1 0 0 1 0 1 1 1 0 1 1 1.

So, this is the ID generated by master 8259 in response to the first INTA bar cycle. So, this will be in slave mode. So, whenever this slave 8259 receives this ID, then it will respond to the second and third interrupt acknowledge cycles it will give this the type of interrupt code on the lower order 8 bits of data bus of 8086.

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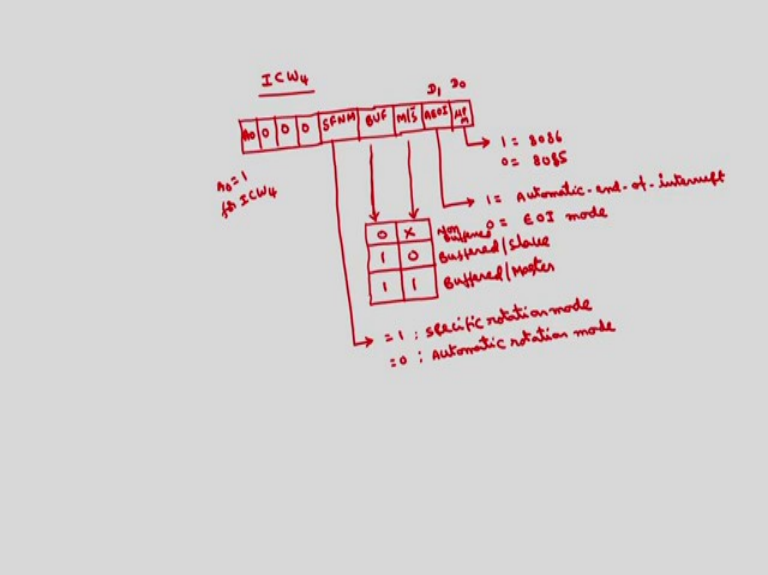

This is about the ICW3 in master mode and slave mode. Now, going for the ICW4. The format of ICW4 is then we have 8 bits and A 0 will take additional bit. This D 0 bit will be microprocessor mode. So, this will be 1 for 8086 and 0 for 8085. The next bit is D 1 which is AEOI this is 1 for AEOI the abbreviation of AEOI is, automatic end of interrupt.

Once the interrupt is interrupt service subroutine is executed then to indicate that the interrupt service is completed. So, you have to use there are two modes of this interrupt service and process to indicate the end of the service, one is automatic mode so another is just simply manual mode. This is 1 for this automatic mode and this is 0 for just by default end of interrupt mode.

I will discuss this in detail later so, this is second pin. So, after the completion of the service of interrupt so to show that to indicate that the interrupt service is ended. So, we can have two types of the this end off interrupt indications one is automatic another is EOI. So, this is 1 means automatic 0 means EOI, then third bit will be M by S bar and forth bits together this one buffer. M by S bar this is master master slash slave bar and BUF stands for buffer.

So, these 2 bits will decide, there are four combinations here using 2 bits. So, the corresponding operation is 0 X, means this can be 0 0 or 0 1 and we have 1 0 1 1, this is 0 X means this is non buffered. So, what is meant by this buffering we will discuss and this 1 0 means buffered in slave mode, and this is buffered in master mode. So, these

about these two next 2 pins buffer and M by S bar, then we have specific nested mode, as I have discussed in the last class.

So, this 8259 can operate in three modes fully nested, and automatic rotation mode specific rotation mode, so that will be decided by this bit of ICW4. This is 1 means; specific mode specific rotation mode, and 0 means automatics rotation mode. As I have discussed this modes in the last class in case of automatic rotation mode the priority which is recently served will be given lowest priority and then so, in the order of this IRs the priority will be assigned.

Whereas in case of specific rotation mode the lowest priority can be assigned to any of the IRs by the user. So, these are the 5 bits remaining three are do not cares and this is A 0 bit, A 0 is equal to 1 for ICW4 also. So, using this initialization command words so, we will write a later some programs that time the operation of this ICW4 how to form this ICW 1 to 4 will be clear.

Then in addition to this initialization command words there are some operational command words also OCW, so we have 3 operational command words so, we will discuss this operational command words in the next lecture.

Thank you.