Optimization Techniques for Digital VLSI Design

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Lecture – 12
Physical Synthesis: an Overview

Welcome everyone. So, today we are going to discuss on Physical Synthesis. So in specifically we are going to talk about all the sub steps of physical synthesis partitioning, floor planning, placement and routing briefly.

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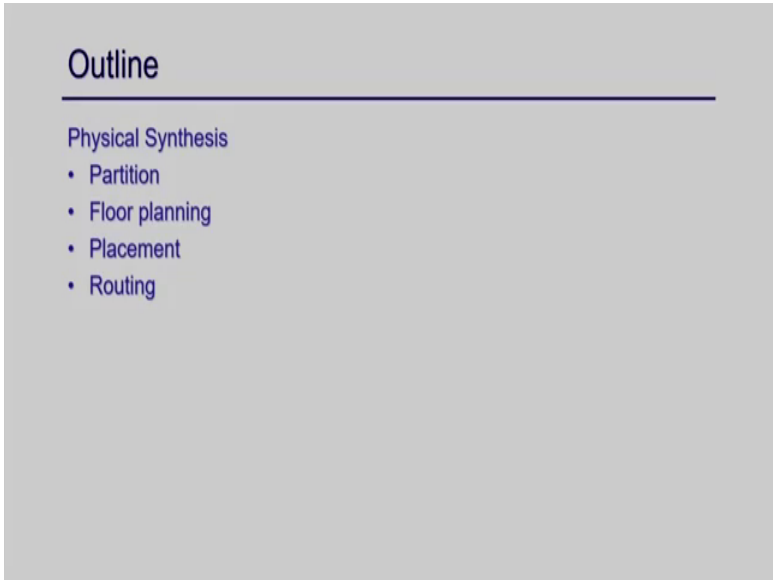

In physical synthesis, if you want to cover it might take maybe 20 20 lecture. So, instead of going into detail or each techniques in each in each techniques detail what I am going to talk about in this always try to give a brief overview of the whole physical synthesis process, what is the objective of the sub steps and what is the problem definitions and what are the general equation to solve that? So, instead of going to solving them using exact algorithms ok; So, let us start.

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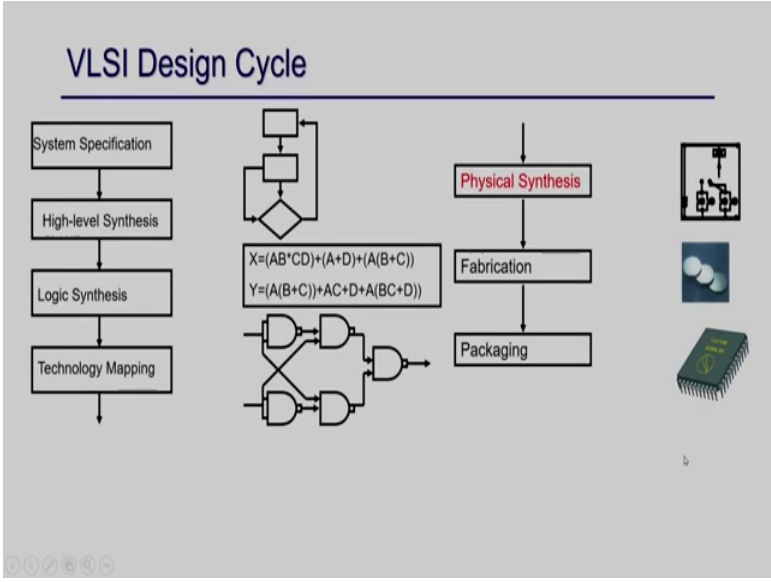

So, if you look into VLSI design cycles we have seen that we already discussed that it start from some specification, then it go through high level synthesis, logic synthesis, technology mapping and then physical synthesis fabrication and packaging right. And we already have discussed about high level synthesis, logic synthesis and technology mapping.

And we are going to talk about physical synthesis today. So, if you just think about after the technology mapping step? What we have? We have a transistor level or sorry gate level circuit which have when it have there is a huge circuit and those are actually represent by the libraries cell libraries it is if it is f p g; then it might be this l u ts RAM; d s p's or if it is ASIC, then it is the library elements like NAND gate, NOR gate, a flip basic flip flops RAMs and all right.

So, this is something the representations and now in physics physical synthesis what are all our objective? We have to give a physical form of the your chip right because. So, far we have talked about lot of optimization, synthesis and all the stuffs; now we have to give a physical representation of your design let us how which is important. And now which what do you do what do you mean by physical synthesis?

Physical synthesis in the in the sense that now you have to place all the your gates or those transistor gates which actually to converted to transistors in this physical synthesis. And then they will be placed right in your actual chip area and all the interconnection, all

the edge between the nodes that has to be connected physically in your within the chip layout area.

So, that is what is called physical synthesis; in the physical synthesis you try to place those nodes or the basic units of your design into the physical area and also you try to we try to connect them properly. And your objective is always try to find out the minimum area to pack all of your gates in a some in another say layout and you try to make the interconnection cost as low as possible right; so, this is the basic overview.

Once this is done, we will go for fabrication and you also remember that at this point this gate level design will be converted to transistor level circuit which is very obvious transformations because it just replacement of equivalent circuit representation of each gate right. So, that is not a big task of physical synthesis. So, we can easily convert that gates to the transistor level circuit, but what is important here is that making a physical placement of those gates and that making physical interconnections right.

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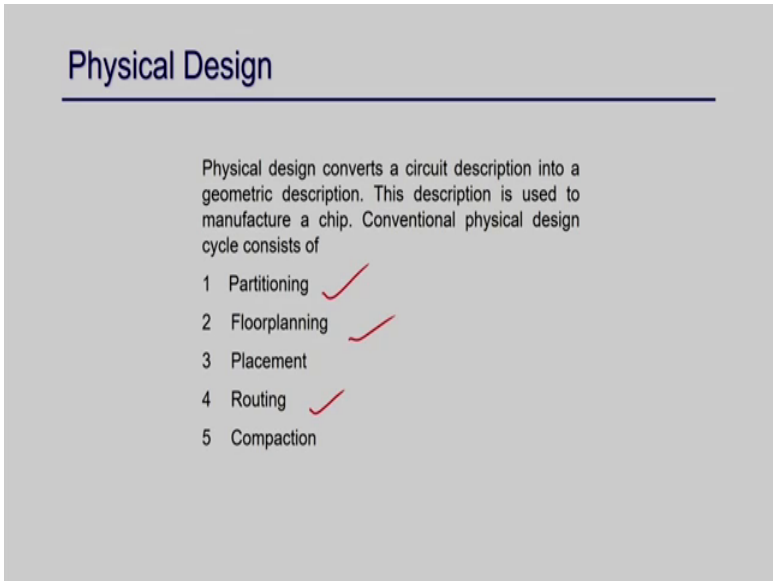

So, let us go into this physical design steps. So, in physical design the sub steps are partitioning, floor planning, placement, routing and final the compaction. So, we are going to talk about this partitioning, floorplanning, placement and routing what is then what is the objective of a sub steps right?.

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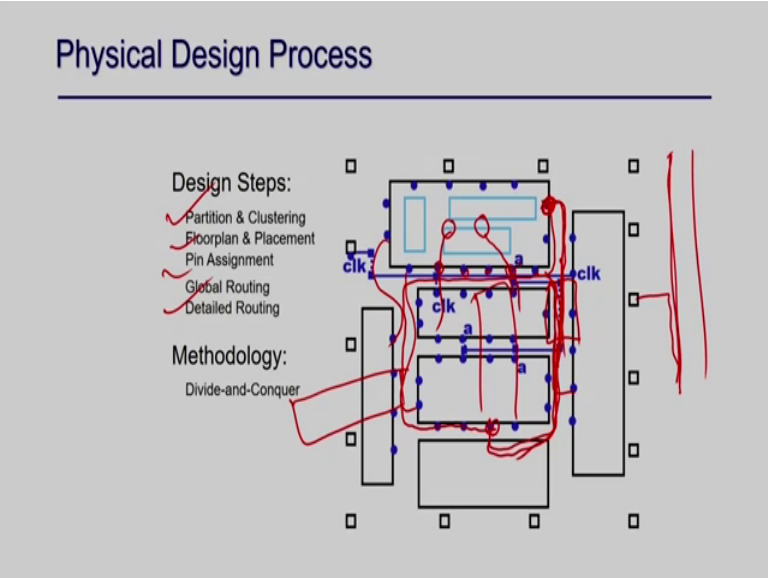

So, if you look into this designs when you have big design. So, first thing you have to we want to do our objective is to suppose your design has say 1 million gates. So, we want to place them, but a we try to placing all this 1 million at a time is kind of impossible job right what is the basic approach we usually following in every life. So, whenever we have big task we try to make it; we partition it we try to make it sub task and we try to solve the sub task and then we try to combine the results.

So, the same approach is happening here we want to place the whole thing together into that layout area. So, we instead of doing that we try to partition the whole thing right; we make the small small component we want to place the each component at a time. And also it is kind of hierarchical or recursive approach.

So, suppose if you want the big circuit we want to play partition in say 10 components. So, then I place this 10 components in the layout then each component you again break it and you again try to place the each sub component of a component again right, it is a kind of recursive approach. So, the first thing of this process is that you partition your big design into small small component so, that you can place those each partition right. So, that is what is call the partitioning right or class study.

And then what is the floor planning and placement is that when you have this each component that has to be also placed right. So that each component has to be placed in your area right; so, this is what is called placement floorplan and placement the floorplan

and placement I am going to talk about detail. So, basically you plan your floor first of all if you have say 10 components, how should place; this can be placed this way or this can be place this way also right. I mean you can think about either vertically or horizontally right. So, similarly this can be placed this way in the or the vertically as well.

So, you can have lot of possibilities and maybe the some other organization give you a compact area instead of this organization. So, this floor planning and placement take care of that once you have the most small small component; the partition those has to be placed properly; so, that your total area is minimum.

And then this pin assignment is something; so, as you understand that from this component that will be many interconnection going to some other places right; it may go to this places, this may go to this places this may go here this may go some other places right; so, there is lot of interconnections. So, that is what is; so, basically if you have a gate that will try to communicate right. So, you have to assign some pin because now you have a make a interface for this module right. So whatever the interconnection from here is going out that go through some pins right; so, these are the port kind of.

So, you have to assign pin for each component which is called pin assignment and then you have to make the actual connections right. So, then once you have this then you have to make the global routing. So, for example, you want to make the connection from this node to this node. So, you decided that this will go through this part or you may be in some scenario it might go through this also right; it might go through this also because of some reasons.

So, that is what is call routing; so, you know that I have to make a connection from this port to this port. And you can understand for a bigger layout there may be multiple such possibilities right you have to make this connection exact right. So, which through which part of the channel it should go that you have to decide that is what is call global routing right.

So, then once the global routing is done then you have to make the detail routing what is that? So, detail routing is something is once you have decided that there are 4 wire will go through this portion of the design, then you have to decide which there may be some track right. So, this track this will go and the second track this will go there maybe some

track which can be shared by two components; so, we will discuss about those detail; so, which is called detail routing.

So, that you; so, you understand the basic essence of this whole process that you break your big design to multiple component which is partitioning. And then you decide for each component what is the exact area and then how to place them optimally so, that your interconnection cost will be less. And then you make the actual connection in the ok the previous that is pin assignment you make the point of your how many pin you require to make the interconnections for each component.

And then you go for global routing; global routing means you try to make the actual through which region your particular wire will go that you will decide. And then you make the actual detail routing exact track through which that particular connection will go. So, that is what is call detail routing and this is the overall steps of your physical design process ok.

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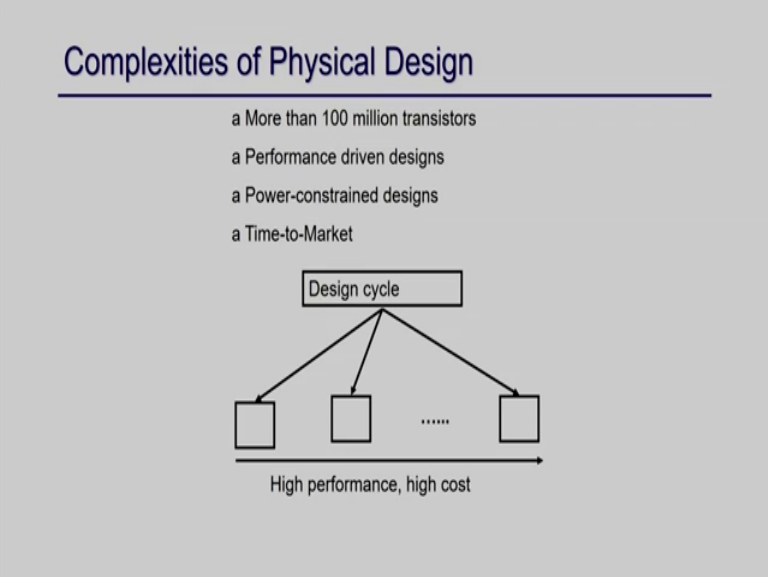

So, what is the problem or the difficulties in physical synthesis is basically; you can see that the number of transistor may be 100 million, 10 million; it is a huge right and handling such scale design is not easy right. And also sometime you have that performance driven design something like you want to achieve this timing like this your power or dissipation should not go beyond this, your area should not go beyond this particular.

So, you have to always meet a target right; so, this performance depend and also as I mention power constraint also there is we cannot use arbitrary powers, if you have very long interconnection that will consume low power; so, I mean lot of power. So, you have to always also think about that your power constraint also meet and also the time to market. So, you cannot just take infinite time to just do the physical to get a generate a physical; physical chip is optimal. See you always have a time to market or constraint or the pressure always from the marketing to you to finish your things within the time budget.

So, that is what why this physical synthesis is very a complex process and when it has to be and we will discuss all the sub steps and there is a lot of methods are there. And also one more important point has to be noticed here that all this subtask that I talked about this placement, floor planning, global routing, detail routing all are most more are most of them are kind of a n p complete problem; n p complete problem in the sense they have did not have a polynomial times, they are not polynomial times; however, they are kind of experiment with they if you are try to find a optimal solution for them you need a exponential algorithm right.

But physically you can understand with the 100 million transistor; it just will not work right. So, most of the cases you have lot of heuristic; so, that is why basically this in physical synthesis you find lot of approach; they all are kind of heuristic base approach. Because all exact solution is not scalable, you always have to think about some heuristic which is logical; which works for most of the cases right. So, that is why they are lot of variations of the algorithm available for this is each subtask. And it might cover the whole semester to just to discuss the physical design right.

So, that is a or some other part of this a the complexity of this physical design right.

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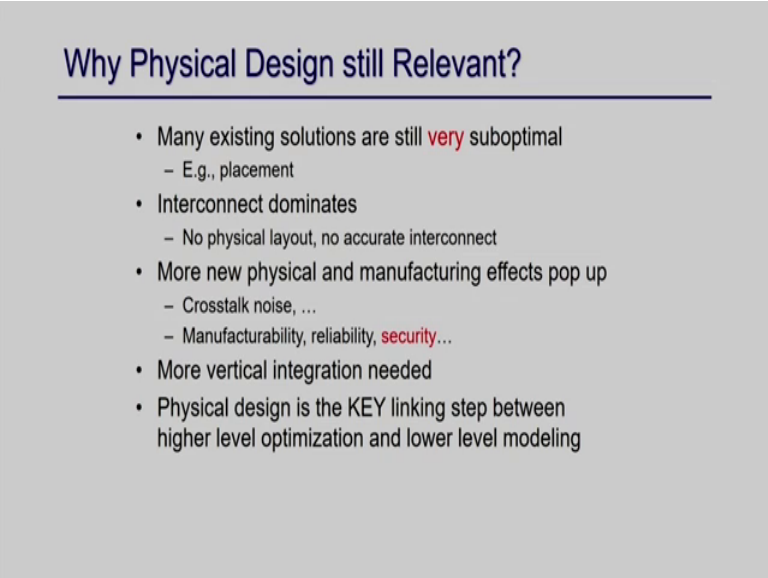

So now, if you move on why and we can see that this physical synthesis all the tools are available industry tools are available right. So, they are already matured their working fine and then why moving to think about more on this physical design why this is still relevant?.

So, the point here is that yes the placement all those things are available, but since the you understand there are a sub optimal they may not work always right. And most importantly the new whenever this the as the things as time move on, the new complexities are coming up right. For example, this reliability of yours chip, you try to interconnections are going very high nowadays and your and also this crosstalk you want to minimize.

So, new reliability of your design and securities also may big concern nowadays. So, all this new aspects are coming q key aspects are coming new design you have to develop or you have to emerge it some new placement algorithm or partitioning algorithm that should that should actually support this kind of new requirements of your design.

So, for example, the securities something is very very important part in in important issue now-a-days. We you can think about the the recent news on that processor a the processor that almost all for Intel processor sorry a MD processor are not they are vulnerable to attack right because of the branch prediction; you might be aware of that that they might leak some information from the power which can be which can be about

the software that were are running on that and some attack can occur when attack can happen to your processor also.

So, ah; so, basically the kind of algorithm that so, far developed those are not concern about that. So, just to this is just to give in highlight that you might have to think about new kind of placement or new kind of partitioning approach that maybe some new security concern will come because of the existing approach; that is we have to always that you think of evolving new kind of technology or the algorithm or the technique that can support this new kind of constraints right. So, this is also that is why still this physical design is relevant and we always is still talk about those this synthesis steps right ok.

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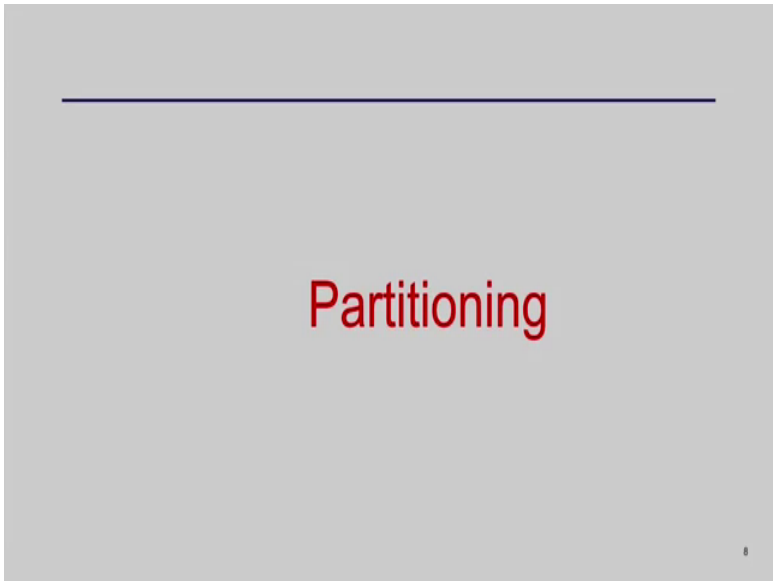

Now, I will move on to each sub steps in each sub steps; what I am going to do? I am just going to define the problem and discuss the issues and then I will without going into each I mean all this existing algorithm on that ok.

So we will start with partitioning; so, partitioning is something very common in every approach right.

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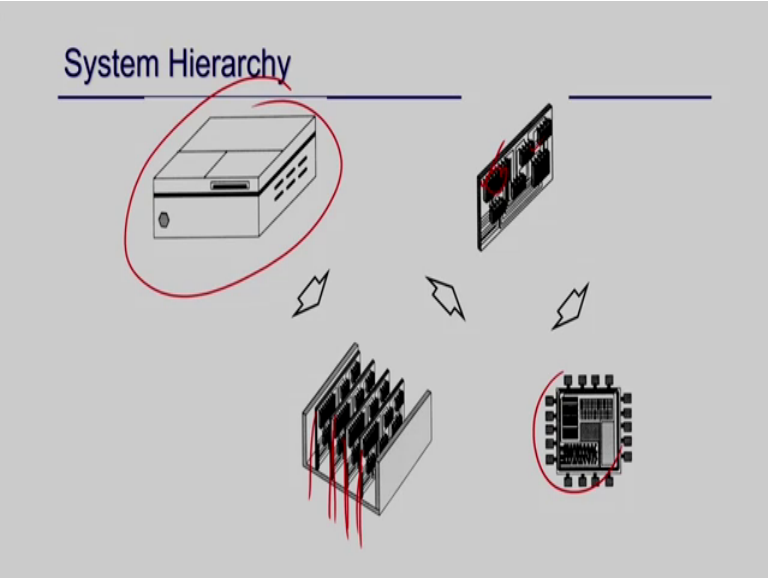

If you just think about key it is just the ASIC prototyping, what we do actually we have a big system at this might be haps board right and. So, where we just stack multiple FPGA there are multiple stack right. So, I want to map a big processor in a FPGA board and its not fit in one FPGA; it might need 100 FPGA. So, that is how we stack right; so, we have some multiple layer and then each layer you have multiple FPGA.

And then a probably and each of them is kind a FPGA right; this is just an example. So, similarly whenever you have a big problem we try to partition it and then we try to march to get the solution and that is what is also the same approach, you are going to solve in this partitioning of a circuit right.

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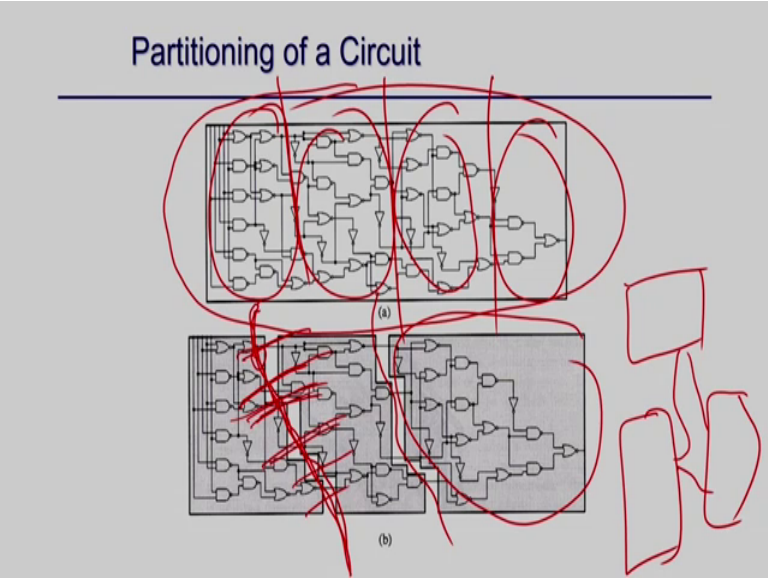

So, whenever you have big circuit or objective is finally, place all this for example, here this is a big circuit is given our objective is to place all this gates in a chip area in in minimum possible area. So, one approach is that you take one by one and you place them which is not physically possible that I have already discuss. So, basic idea is a process partition your design right.

So, you partition your design in small small component and you try to place this together, you to try to place this together, you try to place this together, you try to place this together something like this right. So, similarly this is what you are shown is there; so, we have a partitioning here, we have a partitioning here and we have these are the three partition. And I try to place this partition independently right and once we have done we can again recursively do the same partition within this component or see this component they unless I have a module which is actually easy to handle right.

So, this is what is the partitioning of the circuit means we have to partition and what about the things you have to take care here? Is that this cut whatever the number of wire crossing this car right. So, if you make a partition here we have to identify a how many wire is crossing insides.

Because those are wire has to be routed later right. So, because you understand when you have this break these things and you have a say there are 3 component and they shown here. And now all the connection that are coming from this crossing this cut has to be

routed here right. So, they have to routed here so; that means, you are objective visible you have to a try to find a cut which has minimum number of such routing logic right. So, that actually give you the benefits that you have a lot of less interconnections and that is a good partitioning of your algorithm.

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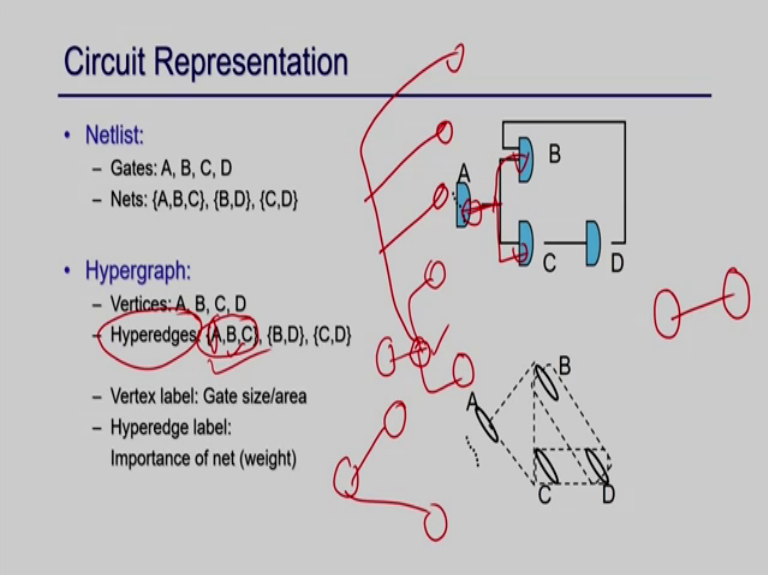

So, that is what is; what is important. So, if you just formulate the circuit partitioning problem.

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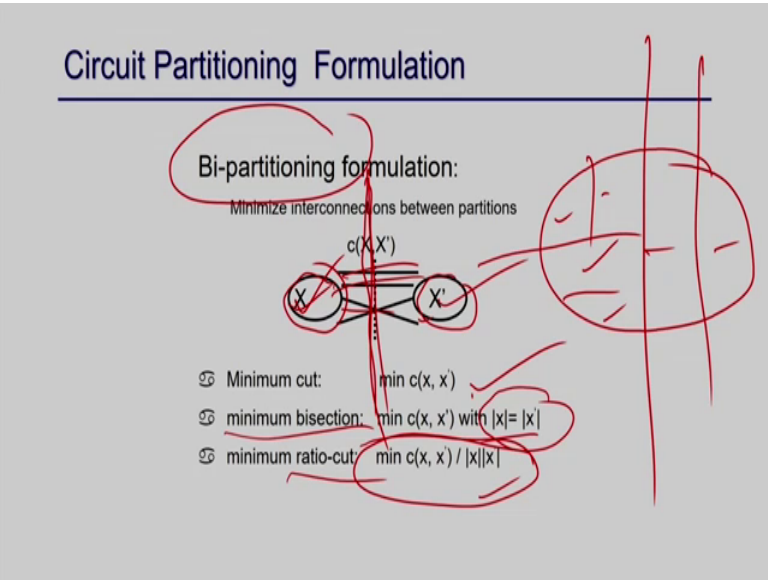

. So, our objective is something to try to bi partitioning. So, basically if you think of the partition can be anywhere right; it can be k partition you can do part in k components, then will be is a k partition if it is bi partitioning you try to make it bi. So, you can do a recursive that I break the whole circuit into 2, then the other thing will be again split into two and this is kind of a bi partitioning right. So, this is the whole circuit I make it by 2, then this component again I make a by 2; this component I make a by 2 then this component I make a by 2, this also I make a by 2 and so, on.

So, this is what is call bi partitioning where I am going to partition the whole design recursively right and. So, if this is say partition into two component X and X bar and this is my cut. So, what will be our objective? Our objective is to min cut the number of line crossing here should be minimum that may be your objective. Or it may be that you try to make a bi partition then two partition where the number of nodes in this component and number of component is same which is call minimum bisection that is actually the bisection where the number of element in the both partition exactly same right.

Or it might have a minimum cut ratio where the what does it mean? It may be that the number of wire component of crossing here divided by the number of node here into number node here is the minimum right. So, this the your objective might be different, but apparently the main objective is something you try to reduce the number of wire crossing that. So, crossing in the this cut which is something will be finally, has to be taken care of by the routing algorithm; so, that will be your primary objective right.

So, that is something this is how you can define the partitioning problem. So, one point here to be noted that your graph I mean usually we usually in a graph we considered the node between edges right. So, what we have discussed that, but whenever you have (Refer Time: 18:36) right this AND gate output is going here and here. So, then how do you represent this node right? This is something call hyper edges right there is one source and multiple output.

So, this kind of edges is call hyper edges where you have to a represent the edge is between set of nodes right, where the first start node is the source and the rest are the destinations right. So, here A B C means a is a source node and B and C is there right; so, this is something like this. So, this is what how we can replace the hyper edges.

So, you can argue that I can actually put two edges here like this is also represents the same thing, but it will create number of edges is more and it will create things complicated right. So, usually we handle this hyper edges usually standard graph right.

So, you actually think about this I can put a node here and this will become the same thing this is a standard node. And it will be standard graph and if it is only two wire it might have 100 right. So, then it is actually this is something we can represent like this as a standard will did a discuss about this more detailed at.

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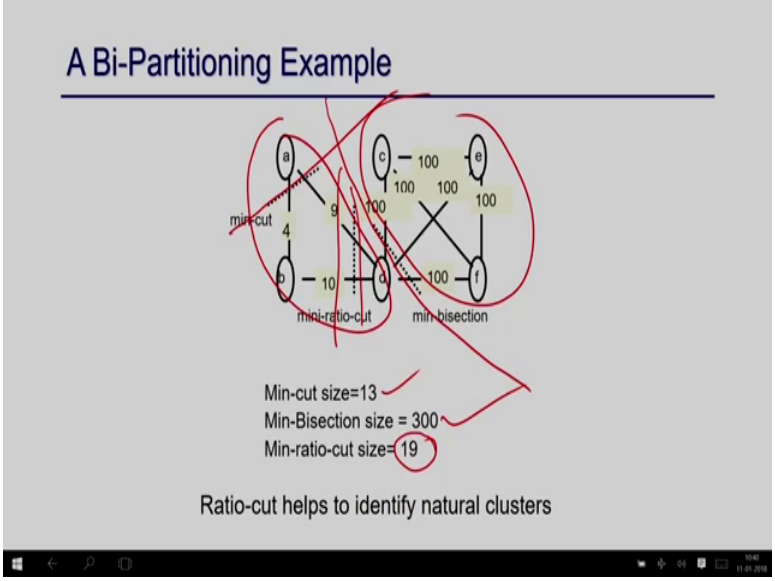

So, now here as I mentioned that formulation is that I want to make it find a cut such that between two partition either may have it will be minimum cut the number of crossing is less or the bisection have exactly bisections at the both component has equal number element with minimum number of cut here or I can have a minimum cut ratio.

So, here is an example suppose this is my graph where this 4 means the number of edges between these two this is 4 right there may be more number of edges I just pick the count. This is 100 means the number of interconnection between d and f is 100 right. So, min cut is this right; so, if you just think about a cut here how many node are causing 100 plus 100 is 300. If I am make a cut here the number of node are crossing 4 plus 9; 13.

So, this is a minimum cut right and this is a minimum bisection because. Now, if I make a cut here the number of node is that is 3 this is number of node is 3 right and. And this is what is the minimum cut ratio because here the number of node here is see if you make a mid cut this part of the circuit has 5 nodes and this part of the circuit has is only 1 nodes right. Whereas here if you if you make a cut here I have number of node in this size is 4 this is size 4 right.

So, as I mentioned here is that min cut why this is min cut? Because the number of node is crossing here two you can think about this is also a min cut number of node is crossing here is two number of edges is crossing is 2, but the weight is 19 here this is 13. So, this is the min cut right these no other cut where we have only two node passing right this is min cut ratio because in this case the number of node is 19.

So, this is this is 19 and this is this is the bisection why because V this bi side is also have 3 nodes this side is also have 3 nodes and the number of node is crossing 100 plus 100 plus 100 three three 100 right. So, there are 300; so, your partitioning is something like this you always try to partition it maybe repetitive or it may be try you may in general you may actually partition into k partition as a example here given formulation here you may have to try to partition into at a exactly is in the same time in k partition.

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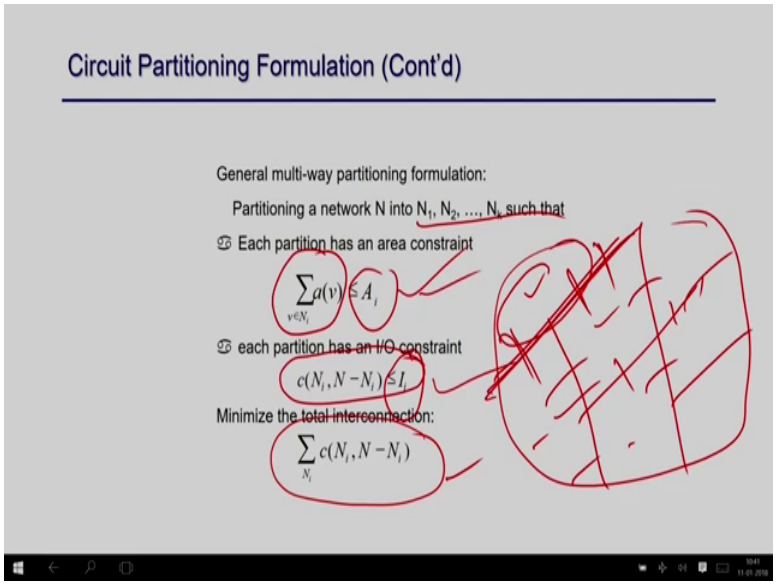

Such that each component area there may be some area requirement that each component area is within the permutable size and the number of edge crossing there the cut size is

always also the crossing that each connect cut should have at least this I mean it should not go beyond this particular number of the cut size should not go beyond some I. So, that constraint has to minimize and also you try to minimize the total cut size right it is something like this if you are a big circuit you try to break into k partition like this.

So, this is partition 1, this partition 2, partition 3 and something like this and each part of the partition should satisfied area constraint, each cut should V satisfy the maximum possible cut size requirement and the total number of edge crossing is cut should be minimum right. So, this is what is V in general circuit partitioning formulation right.

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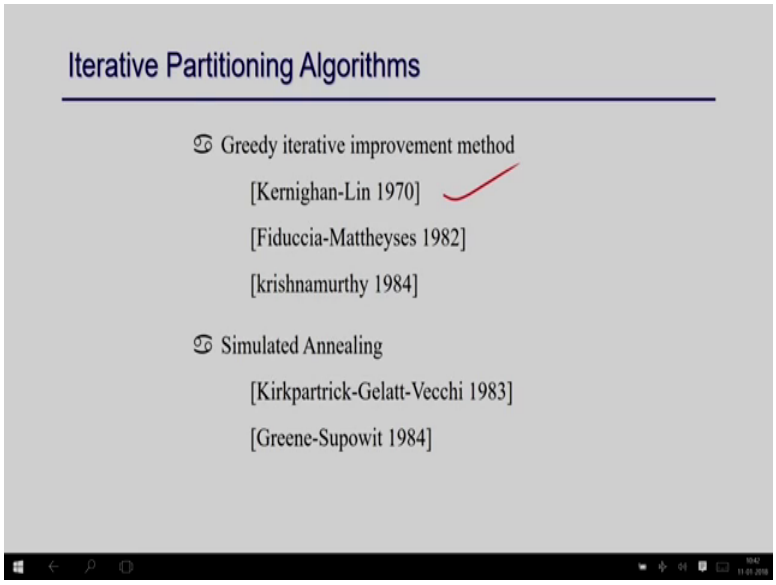

So, in partition as I mention this is n p complete algorithm you can have various kind of approach it can be iterative that you tried to do one partition at a time and then move on. Or it can be module partitioning verse a net partitioning or it can be multi way partitioning, multi level partitioning or it can have a timing driven partitioning or so, there are maybe various kind of techniques are there and also if you just going to this approach like iterative improvement algorithm like Kernighan algorithm Fiduccia-Mattheyses algorithm krishnamurthy's algorithm.

Similarly, simulated annealing approaches are there. So, there are various kind of a approaches are there it is not possible to discuss all of them here I just give you a brief overview of the scale algorithm. So, that you understand the how this practical k and this is the most simplest version of the algorithm will give compared to the other one right.

So, that will give you some brief idea how the partitioning works right. So, if you just move on; so, in this is actual to the bisection right.

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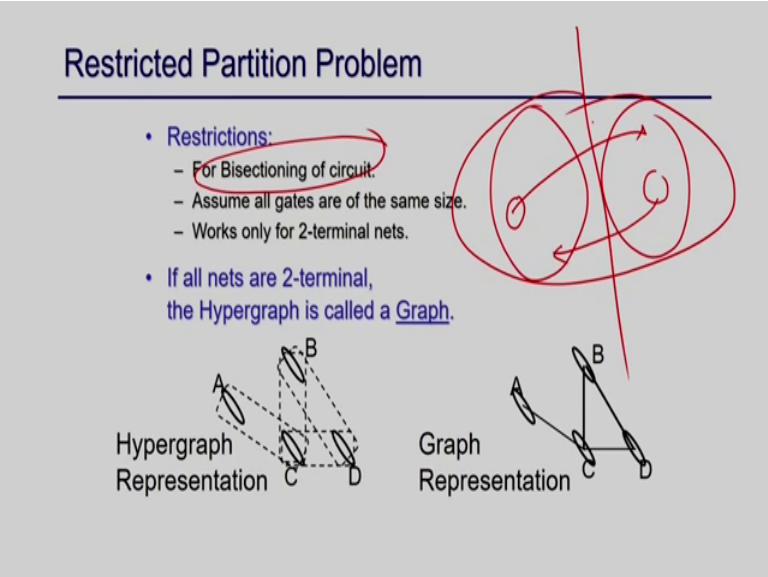

So, basically you try to make the circuit into by 2 right and the idea is that you start with the initial any arbitrary partitioning; you take a just any arbitrary partition, you try to bi partition the circuit and then in each iteration you try to take a node here and you try to (Refer Time: 24:20) here and you move it here and you try to move it here.

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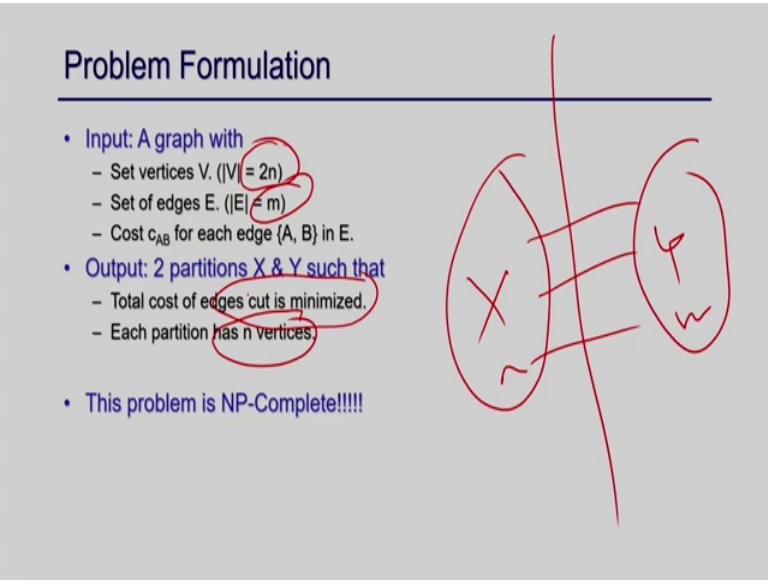

So, that every after every iteration the number of node here and the number of node here is remain same right. So, here is; so, basically if you think about initially my graph has 2 n nodes after the partitioning each component has each partition have a n nodes and every and if there are m number of edges.

So, that there are it actually define into two partition into this is X component this is Y component this is also n nodes this is also at nodes and. So, and then you try to minimize the cut cost right this is what is something that total edge cost is minimize right this is how the whole thing works.

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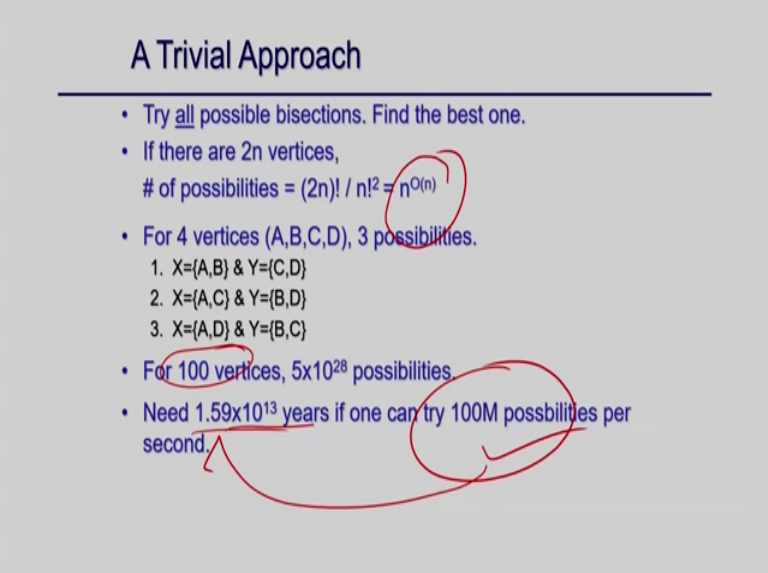

So, if you just think about the how it should work you might try to all possible partitioning right if you make it trivial approach you just make all possible bisection of your circuit and then you will find the best one right that will be very trivial approach.

Now, you think about there are two n vertices. So, all possible combination is n to the power n right which is huge n to the power n possible bisection is possible and then you just think about 4 vertices is fine there are 3 possibilities, but if there are if you are node has 100 vertices only if the possibilities is 10 to the power 28; 5 into 10 to the power 8. So, which is huge you can understand the element.

So, even for only for a 100 vertices it will take 10 into 1.59; 10 power 13 years. So, which is something infeasible right; so, which is in fuss in feasible right just to if you

want try to 100 million possibilities right. So, for 100 million possibility you need this much of this much of time. So, this is just the some number just to give you the value that you cannot go for any good for approach right here. So, all possible finding all possible bisection and finding optimal one will not work right.

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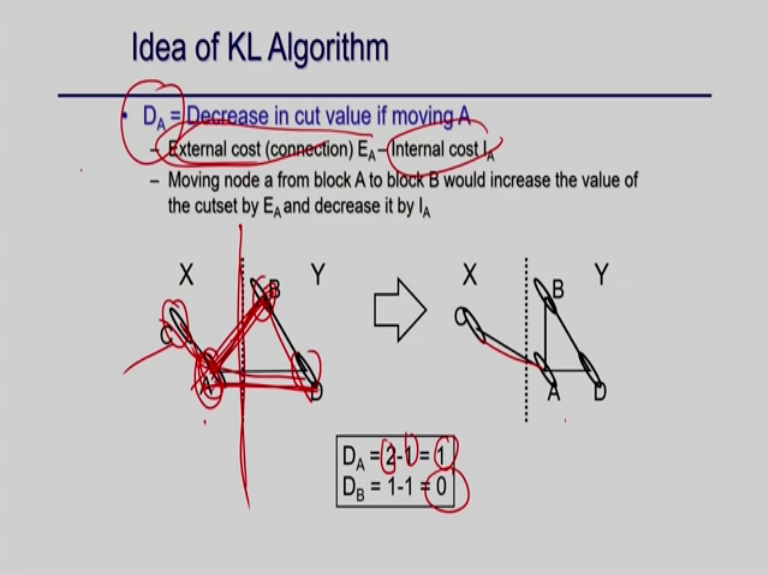

So, in this k l algorithm the idea is that you the cost you have to understand that if you. So, suppose there is a initial connection you try to move a node from here to here what will happen? So, whatever the node from this node to the other side right; so, those node will become they will not be the they will not be in the cut right. So, here I move A to here A; so, these two edges are coming here. So, they are not part of the cut, but whatever the connection from this node to this side; those will be the part of the cut now right that is the cost.

So, which is basically that the external cost that is this whatever actually crossing the other part and minus then the internal right. So, this is the gain if you move a node from this side to this side, the gain will be this right. So, for example, for A initially there are two connection to the other side. So, 2 and there is only one connection to this same side minus 1. So, if you just move A to this side you have actually cut side will be reduced by 1 your gain is positive right.

So, by as similarly if you move this B from this side to this side you can C is over B there is a connection here 1 and the connection here; so, it does not have any gain. So, if

you move B from this side to this side effectively there is no reduction in the cut size. Now if you take a two nodes; so, the gain of A is given by D A which is calculated by this equation this is the D A their cost.

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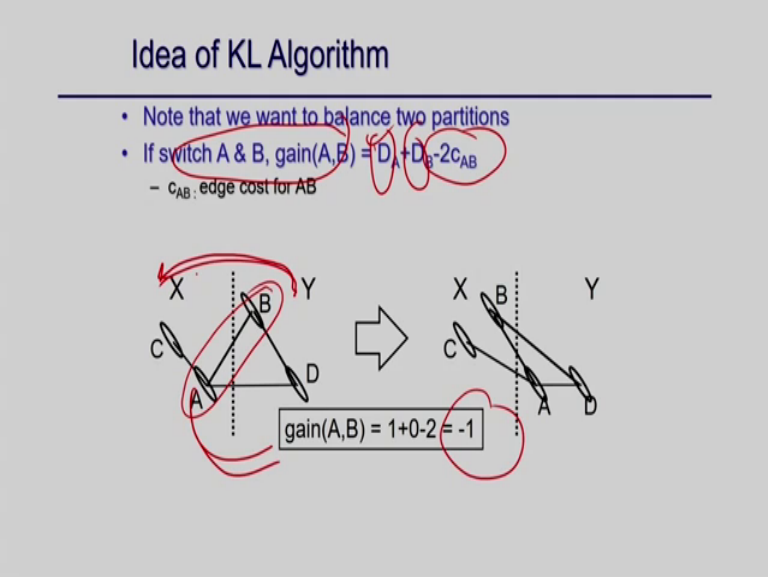

And then this cost of D B. So, that we are moving A from this side, B from this side cost of moving this plus this that will be your gain, minus the interconnection between these two node right there is a interconnection between this node. Because they are a actually counting two times here right; so, you have just remove it. So, they will be always remain the same. So, that is what is your actual switching between two nodes is the overall gain right.

So, for example, if you just swap A and B overall gain in minus 1; so, which is basically negative. So, it is it is not a good choice to swap A and B that means moving A from the left side to right side and moving B from right side to left side which is not a good move.

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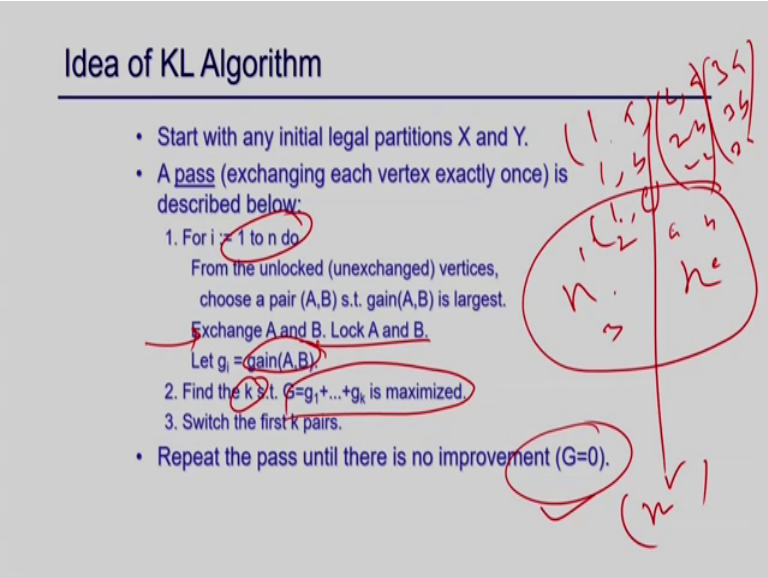

So, the idea is something you start with the initial; cut you take arbitrary cut right of the circuit that maybe high; then you that are n nodes here there are n nodes here and then you find out all possible partitioning. So, there are might be n n square pair right; so, for each there is a node. So, if suppose there 1, 2, 3 here 1, 2, a sorry 1, 2 and 3 here; here A, B and C the three nodes; so, for the possible partitioning is into this n into n 3 into 3; 9 right.

So, you can take 1 a, 1 b, 1 c similarly 2 a, 2 b, 2 c and 3 a, 3 b, 3 c; these are the all possible possibility of pair right because our objective is now is to swap two pairs. So, you find out all this n square possibility and then you choose the best one right you take the best one which has a maximum gain. So, for each pair you calculate the gain and you actually swap the has the best gain right and then you will lock that two. So, that is the gain of the particular move; so, then you just do this for n times you actually met n moves.

So, that at least some n nodes are from here to will move here and n nodes from moving there; some happening here and then may be some of them are actually have a negative gain right, after sometime your gain may be negative. So, you try to find out some k value ah; so, you make a n moves, but you take the first k here gain iteration which actually have a positive impact.

So, you make those them fixed other you just other swapping that you done you just undo them right. So, that will not be actually have done. So, this is after this iteration you have another solution right and then you will keep doing this until I do not find any even no improvement right. So, this is one iteration.

So, the what algorithm will I make a initially by can partition then I do n n swapping right; based on the maximum gain maximum gain to minimum gain. And then I took only k gain which is k swapping which actually have a total summation is positive and then other side just discard and after that I will give another solution right.

So, the cut size will be improved and then I am going to do the same process k times or sometime unless I do not find any much improvement. So, this is just an idea of this k l algorithm which actually kernel gambling algorithm just doing by bisection or bi partitioning by by swapping these two node; this is just one approach there may be various approach and there are various kind of technique.

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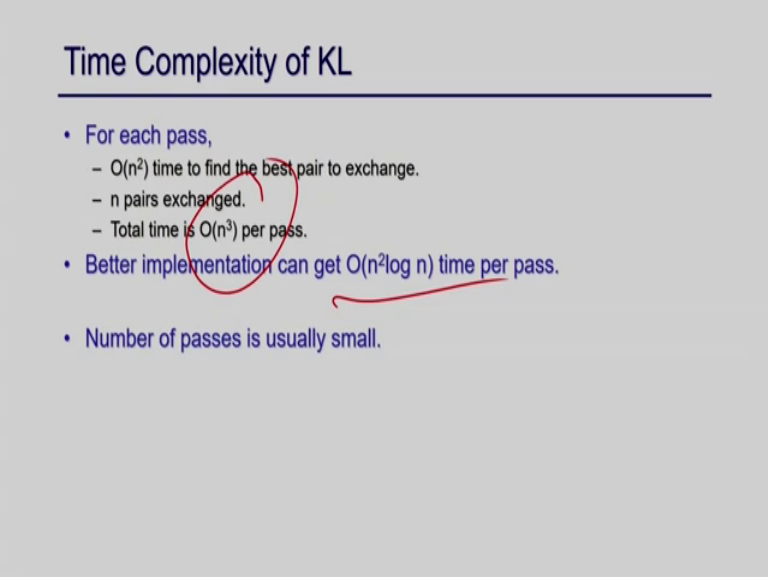

As I discussed here the complexity will be n square compare to the n to the power n. So, which is and for better implementation you can have a n square log n. So, ah; so, this is also one we are doing the partitioning bi partitioning and a we as I mention that various approach I mean I am not going to combine all of them. Now I will move on to the floorplanning; so, what you see after that. So, after partitioning you have some components right some partitioning component like this.

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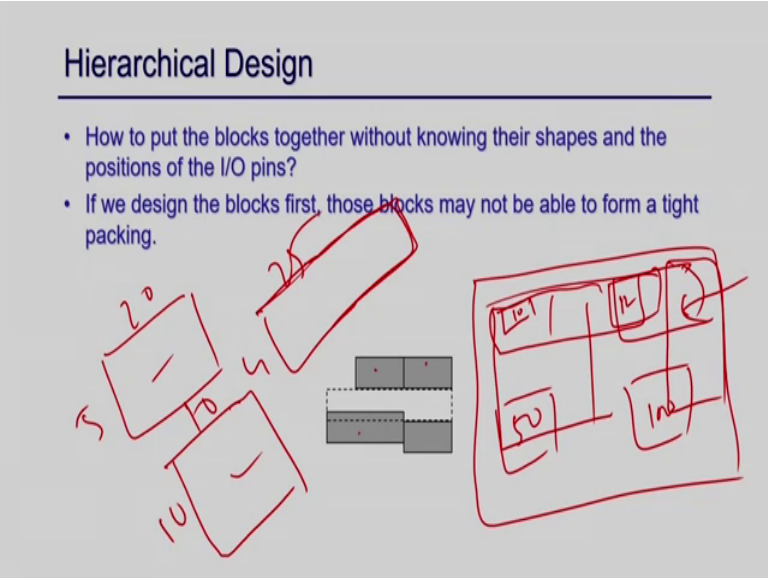

And now you have to think about the planning your layout area right. So, you have say 4 component now we have to physically place those components here right. So, that there; so, that your total area is minimum right. So, you have replace those components here and you understand their area is not always same; this may be only say 10 unit and this may be 100 unit, this may be 12 unit, this may be 15 unit and so, on.

So, they are area may be different different right and I have I am so; that means, size is not exactly all square right. So, this may be a small small (Refer Time: 31:42) 10 means is this is small this is a small one and this is 100 mean this is a big one. So, their size ratio is also different and most importantly their aspect ratio is not fixed here.

So, you I just give you say 100, 100 you can actually construct if obtained into 10 right this maybe say 5 into 20 or maybe exactly square where is 10 10 or maybe 4 into 95; you can have a different aspect ratio right because I just tell you [FL] I have a block which has only 100 unit. So, now you have to fix this aspect ratio so, that for 100 should I choose 10 into 10 1 is better, or 5 5 10 is better or 4 into 25 is better and other options are also there right.

So, you have to always have to decide the aspect ratio of each component based on the total area. So, that you can actually compact those all the component in a minimum possible area right; Because if you just think when you if you take this kind of which is basically rectangular one that will cover this portion of the say area. And then you can

probably you are not able to fix a another component here; instead of if you take this say 10 cross around if you place this way probably the component can be placed here right if you do not place anything this portion will remain vacant right.

So, you try to and that is called dead space you try to reduce those dead space. So, in partition this floorplanning what we do? We try to finalized the aspect ratio of each component and then it and our objective is try to pack everything in minimum possible area. So, that your total area is minimum and total dead space is also minimum right.

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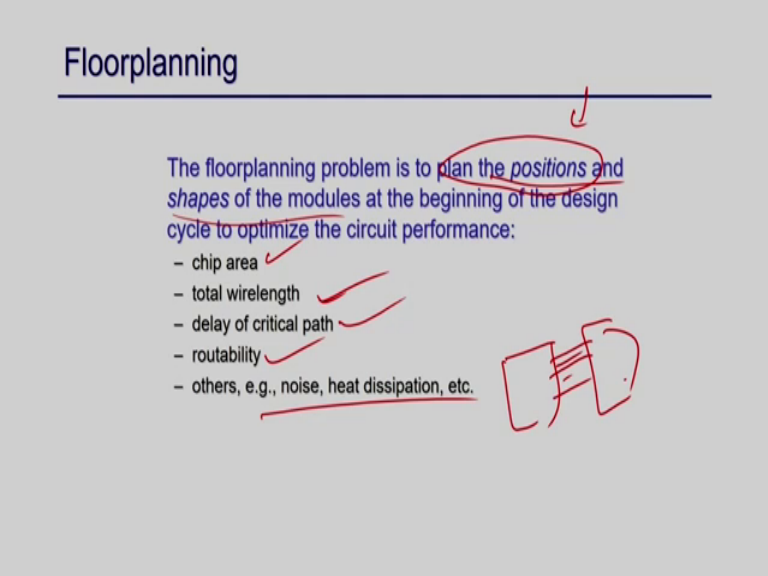

So, if you just move on so, floorplanning is the problem of positions; finding the plan the position not exact plan fixing the block that is important because I am just planning the positions right and then shape is finalized at the beginning of the design right, where your object will be optimize the area, total wire length also. Because you try to because I know that now what is the connection between two component based because that is given by the cut size.

So, that if you have a say this blocked here and there a lot of connection to this block you should place this block as close as possible. So, that this wire length will be less right you try to place very connected two component which very close by. So, the your total length is optimized or delay of the critical process minimize, routability is possible that actually physically all the connections can be made in the physical (Refer Time: 34:15).

So, that maybe also your objective or other objective that you reduce the noise or the heat dissipation or cost stock between the router wires; So, those can be also your objective right; so that is what is floorplanning.

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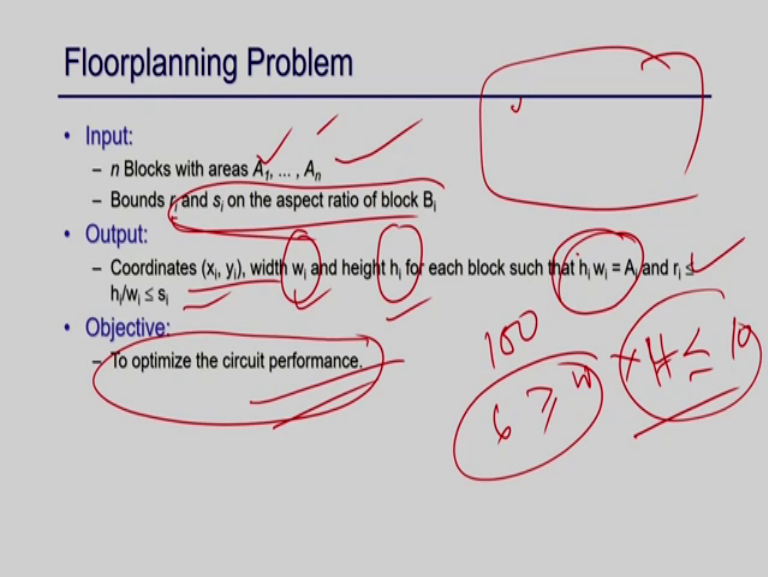

So, if you just define the problems you have n blocks of size area I know the only area and I also have some aspect ratio bound that if you have say 100 10 is the your length be the minimum say 6 right. So, you have to find the W and L right within height high W and H. So, your width should be greater than 6 as a height less than 10 right.

If you have given those kind of ratio constraint on the aspect ratio that you cannot just take a very long or very short; I mean in short height or short width kind of things we should have some minimum constraint on the ratio right this aspect ratio. And then what is the output? You try to actually they find out some location of this particular block such that the two. And you also find the width and height of the block is block such that total area is minimum and also all this height and width satisfy the aspect ratio constraint given to you. And your objective is something to optimize a circuit performance, the performance maybe one of the one of them right.

So, this is what is the problem you are given A component for the area is given you can also and the aspect ratio of height and width not fixed, but there are some restriction might be there your height and width should not go beyond these or should not be at least this kind of thing. And you try to find out the try to place all the blocks in a physical

area. So, width and we so, coordinate of each block and you also find out the aspect ratio that mean width and the height of each block we try to finalize.

So, that total area actually fit into this area target and you have optimizing goal like optimizing the total area or optimizing the routability interconnection cost and other others right. So, this is what is the floor planning problem.

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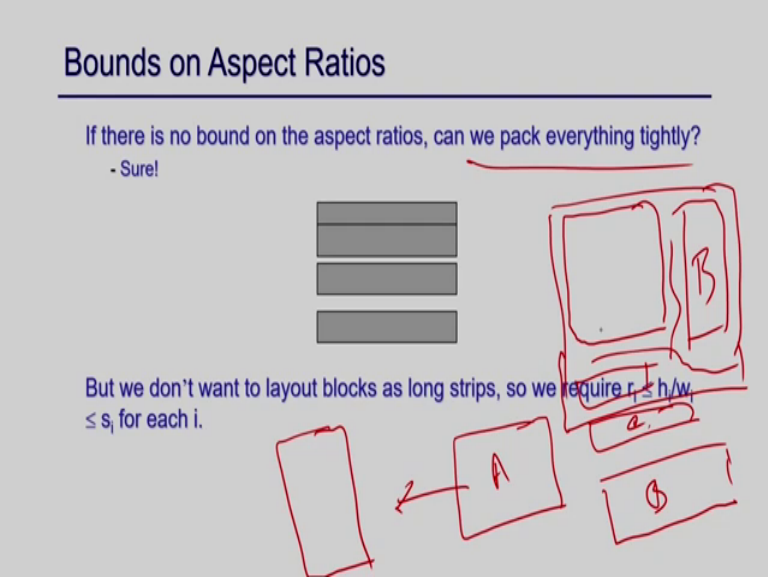

So, as I mentioned this I mean bound on expect this is something that we can always pack everything tightly right. Because the problem I just discard I was suppose this is your component blocks are like this I; suppose there is one block like this one block like this and one block like this ok; there are three such blocks ok.

So, now, if you try to suppose this your chip area; so, know if you just place this one say this will take this sorry; if this will takes a you this is a you try to place this a here; what will happen here. Now suppose these this will take a such a way that now this is cannot fit in here and this may not fit in here also if you just place one of them here say suppose this I.

So, this is say this block is something like this; so, their length is more than this. So, they can replace this way; so, suppose this is B I want to place this way right so. So, now, what happened now there is no way to place C because is all fix that this there is no place

then basically have to just increase the area of your area of your design A chip area just to place this C here right C here and many many space are even vacant right.

Whereas; if you just say instead of taking these if you just take another person of A which is little bit of this shape then probably what we can do? You can probably feed the whole thing into the old area. So, so this will be your, A this will be your B and this will be your C right A, B, C.

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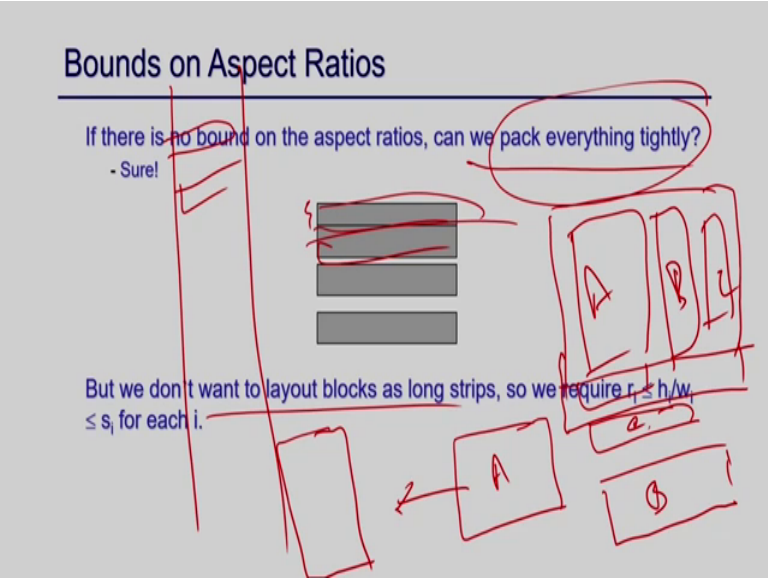

So, this is what is the problem right. So, you might have a different aspect ratio for which you can actually place them in a smaller area, but if you just in a different aspect ratio then you might need more area right; this is a perfect example to highlight the problem. So, one thing always think I just make a the with is one and the length is like this right.

So, then the problem is that your chip will be just a series of block right which is basically this length and which is not visible light with this is not this is not something you are because your layout cannot be a just a long strip which is not is allowed. So, that is why we have some bound on the aspect ratio ok

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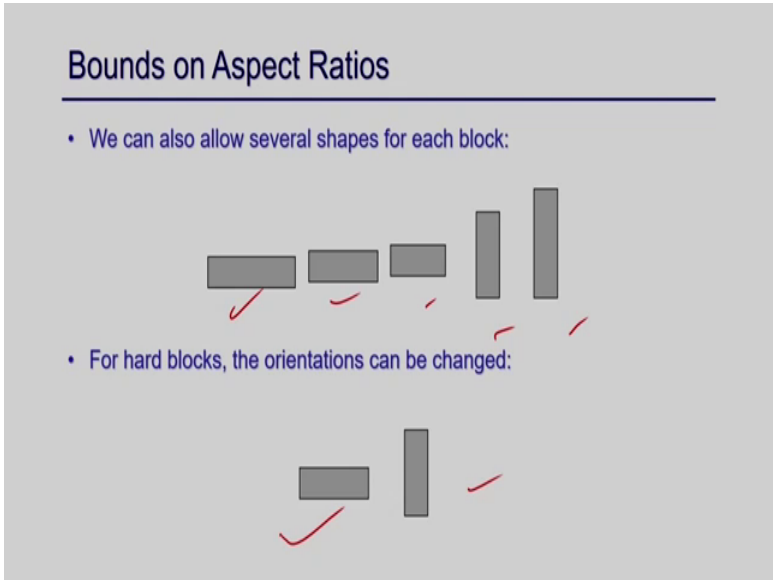

So, as I mentioned that given if the same size can be like this right for a same size your you can generate different kind of block right and also orientation maybe this way that way. So, you have to consider all possible such orientation given on that aspect ratio of constraint and then you try to place all those block in area. So, that your total area primary objective is to reduce the areas size. So, that you can actually place all of them in a smaller possible area right this is what is floor planning.

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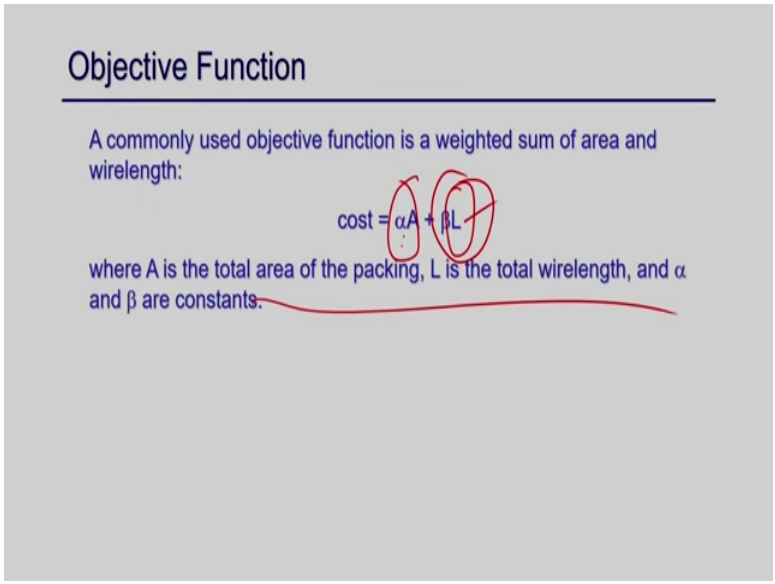

And also a; so, in general the objective function is the minimization area plus objective length right A is the area and B is the L is the length and alpha and fera beta is some constraint factor right this is overall objective of floorplanning ok. And this wire in the estimation is something because now I do not have the exact placement. So, how we can how can I estimate the wire length is basically just the distance between in this.

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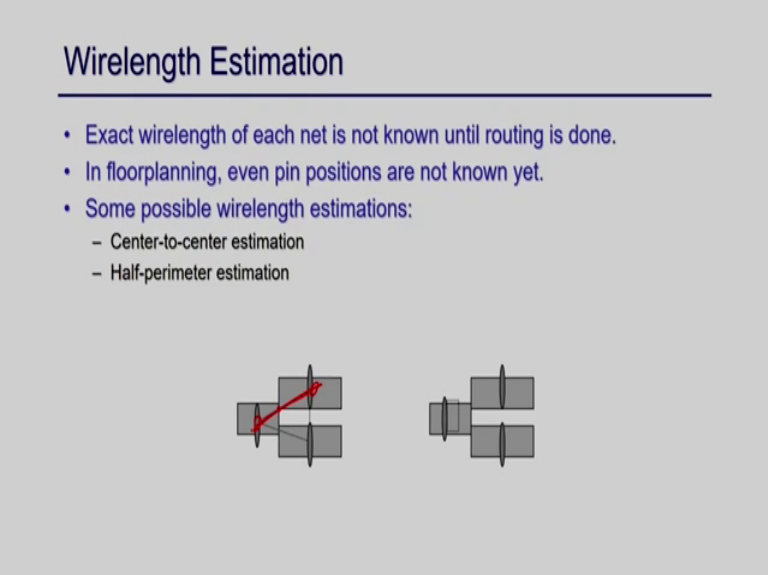

This to suppose there is a wire from this to this I can find thus the distance from the centre point right this may be your or wire length because it is just kind of a estimation ok.

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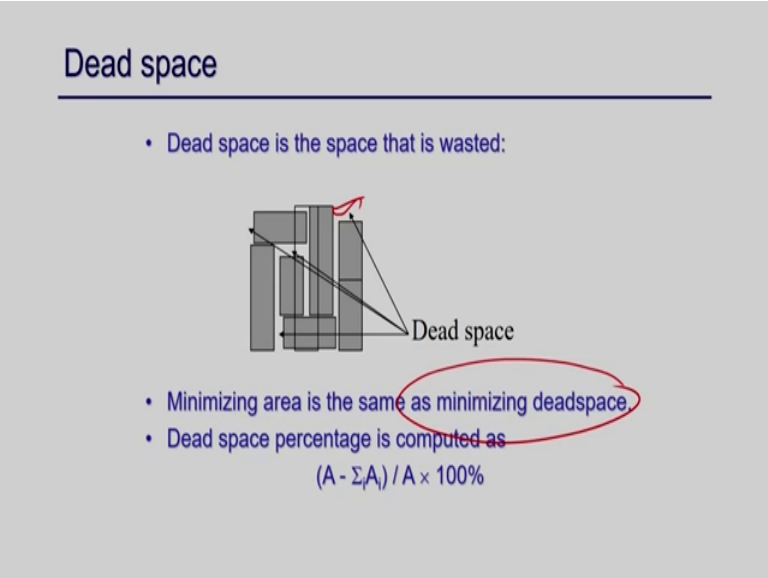

So, as I also mentioned that because of your different aspect ratio it will create lot of dead space here and there also your objective is try to minimize the dead space as well right. So, this is also be an object during programming.

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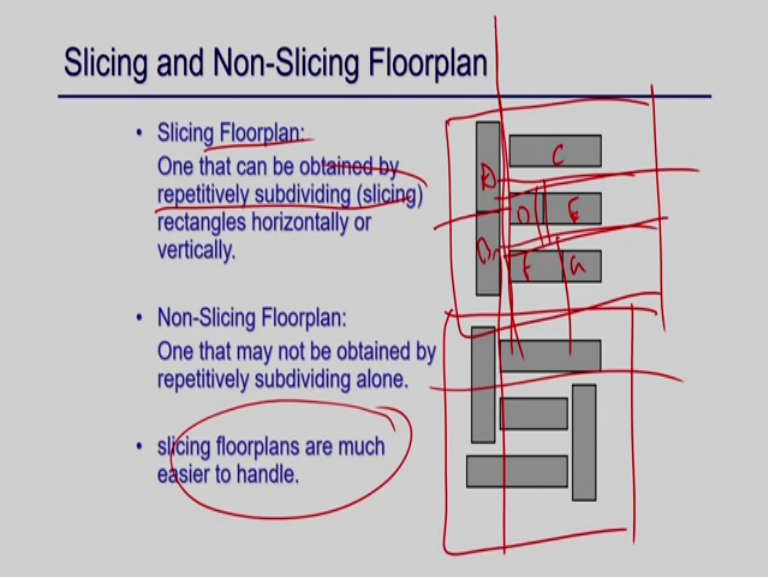

So, and also there is another concept here is sliceable non sliceable floorplan; what is that? Sliceable floorplan is something; so, you finalize your as per your aspect ratio and finalize your block height and width right and then you place them. So, after placing one is one is sliceable means what? You can actually can obtain the your floorplan can be

obtained by repeatedly just slicing the things horizontally or vertically. Suppose this is how you are placing the or designers this is A, this is B, this is C, this is D, this is E this is F and this is G right this your placement. So, then what is slicing?

So, I make a slice here, then I make a slice here, I make a slice here, then I make a slice here, then I make a slice here and I make a slice here. So, I just bipartition each component totally and then this is sliceable; on the other end if you just look into this one. So, this is not a sliceable one because you can see that I cannot make it this kind of a partition; if I try to make it this will partition here. So, this is my component now this is also not a sliceable. So, I cannot make a this kind of bipartition here right; so, here I just make a bipartition like this, but here I cannot make something; so, this is non sliceable.

So, it is generally good practice to make a sliceable floorplan. So, such way you actually make the connection. So, that you can make a sliceable floorplan and will see that is actually helpful in a that ah; we can we can see that this sliceable floorplan actually is easy to handle for placement routing and all other components. So, you usually the kind of floorplanning that will generate that is a sliceable right. So, what is sliceable I just repeat again is something we can bipartition likes sub component at a time to generate your layout plan right.

So, this is how I can do. So, any order right by horizontally or vertically ok. So, these are the some temporary that is should aware of during floorplanning.

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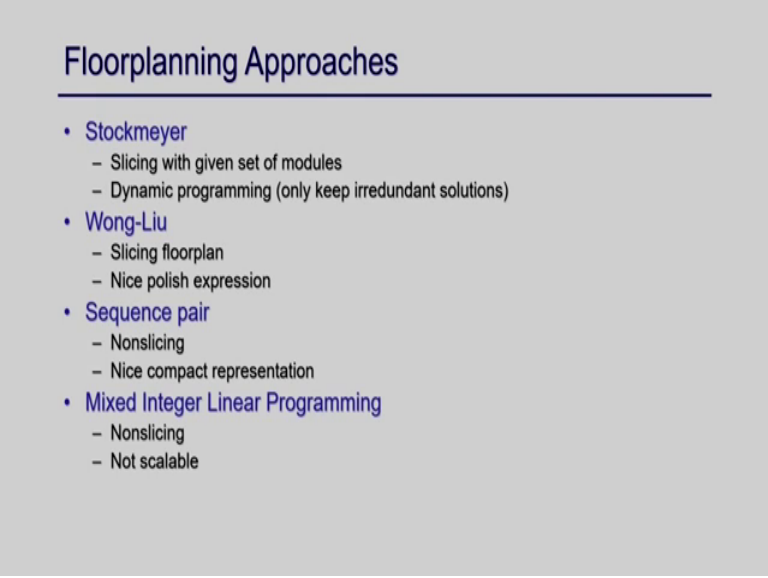

So, again this floor planning you understand that a lot of such approach various approaches there. And when because this again this is n p complete problem and you cannot have even optimal solution cannot be obtained by some optimal algorithm. So, you have various kind of heuristic approach is also available for this step as well ok.

So, I move on to the next step which is placement. So, what is you have; so, basically in what is the placement problem now we actually physically going to place those blocks in your layout area.

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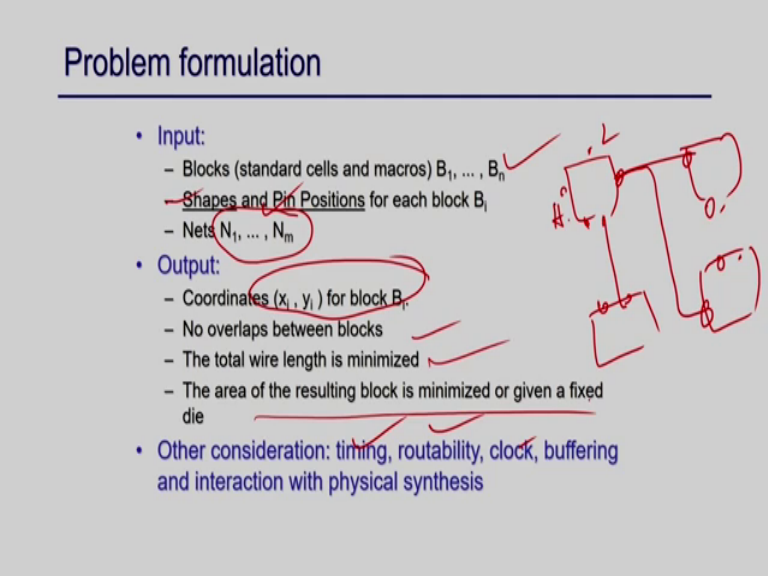

So, the problem input of this block is there are say n blocks and I know because now the shape is fixed by the floorplanning pin positions also fixed by the floorplanning because the pins exactly had the pin will be there that is also fix by then. And the nets also given because you have now let the blocks; so, each block fire exactly the pin pins are there that is finalize. And for each block is given and exactly the connections among developed from pin to pin the connections are also given to you right.

So, this all are given to you now; so, these are all the inputs, all blocks, their pin configuration, their exact safe, the height and width also given for is blocked because now is the fixed size is already fixed by the floorplanning. And all the nets exact net provider accept the connection for the given right. Now you try to find out the exact position of these each block coordinator with block.

So, that no block overlaps total wire length is minimized and area of the resulting block also minimized for a given time right. This is something is the placement problem and you can see and you can have other objective is like this condition like the timing routability clock similarly like the floorplanning also this have can be also your optimization criteria ok.

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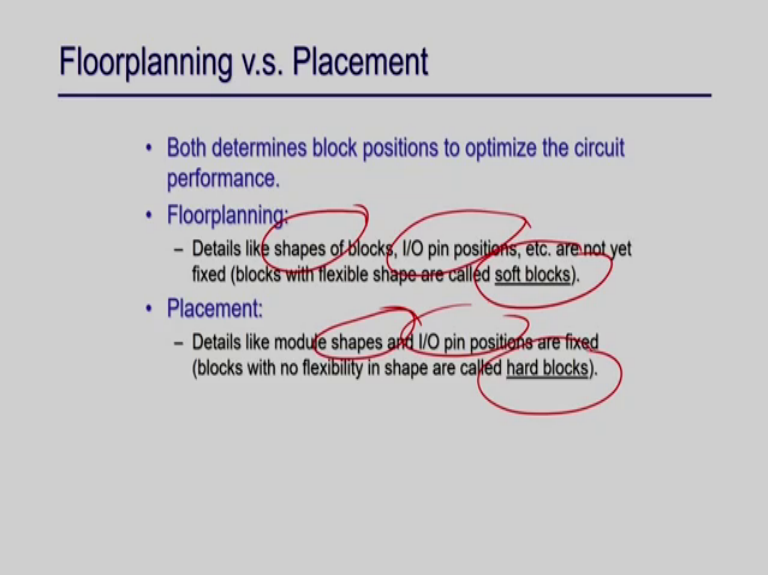

So, you can see that floor planning and placement is very closely because in floorplanning also try to find the position of each block and here also that finals what is the difference right. So, basic difference is the during floor planning the shape is not given only the number of block is given, I O pin positions is also not given right. So, your kind of the block are soft blocks, whereas in the placement I know they are some in same position is given by the floorplan, but that is not the fix position right. So, the but they safe is fixed I O positions are fixed right.

So, this is kind hard block; so, in soft block I have other options like I can take a different aspect ratio and try to fit in, but in case replacement time all the blocks of fixed height and weight. So, I can I kind of a hard block I cannot make the any change in the aspect ratio.

So, that is the difference between both are actually try to find the position of the circuit. So, it may be that the what about the floor planning given by generated the position of the block that may be the final one, but placement you try to actually see if they can be

some other moment can be done without changing the aspect ratio. And finalize it may it may accept the floor planning positions or it may try to find out a better placement of this blocks right.

So, floorplanning as also I mentioned that this is also in block and you try to find out the coordinates. So you can see the input is almost same for right set of block output is coordinates, but the only difference is that I O pin is aspect ratio those things are not mentioned here. And whatever the floorplan positions find out for each block that may be the final one; Placement try to relook to that positions and try to optimize the area that may be some little bit of moment of the block can be done.

So, that your total wire length is minimum or you can you can access also new wire total area. But after placement all the position of this block is finalized then you cannot have any other change, then only things to be done here is the maximum the physical interconnection right. So, after floorplanning there is possibility just to exchange some block position or moving to other places is possible without the die area with an objective to reduce the number of interconnection total area. But after placement you cannot have any option to move your position right this is what is after placement.

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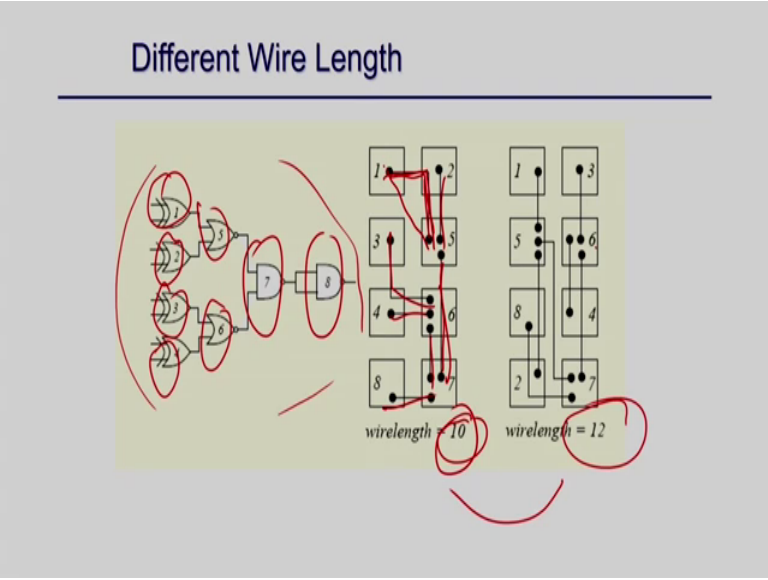

So, you just think about I just give an example here suppose this is your circuit and suppose this each component is a block (Refer Time: 46:25) just for a simplicity. And say floorplanning a decide this decide this particular size and the total wire length is. So, if

you just place them here like this way; so, the total wire length is like this right if you the make this connection here.

So, if you have to make connection from 1 to 5, you can make a connection like this right because it has to go either vertically and horizontally. So if you just think about the length of this is 2; 1 and 2 if you counter 1, 2, 3, 4; 4 and 5, 6, 7, 8, 9, 10; so, the total wire length is 10. Now I just have a another placement because all are of same size here. So, I have all the size make a connection like this 1, 3 here instead of the I just for 2 and 3 and this 5 and 6; 5 and 6.

So, this is 6 here and 5 here. So, I make some interconnection changes here and there now the total length is 12. So we can see that even of the same block size same area, but I can make some swapping some exchange here and there. So, that your total area remain same the total wire length may reduced right from this to this is what the placement try to do right it. So, same size block can we swapped or can be moved to other places are some dead space are there. So, those kind of things can be done during placement.

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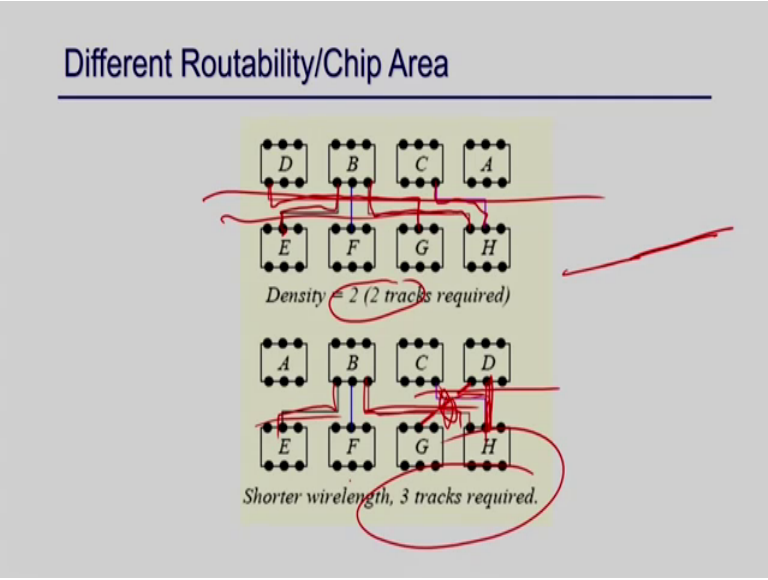

And also sometime this if you just try to make the connection you have to see that you cannot have the two interconnection two connection can cross in the same line.

So, if you just cross this block like B C C A and E F G H then you to make the all the connection you need only 2 tracks right; you can make a connection like this. And you

have a connection and they are not overlapping. So, they can be put in the same track this connection and disconnection can be put in the another track. So, you need 2 track right whereas if you have the some different placement A B C D E F G H; now this connection and this connection cannot be placed in the same because there is a over lapping portion.

So, they have to be into tracks similarly this has to be make here. So, I need 1 track 2 track 2 tracks and then just to B B 2 you now I cannot make B 2 B 2 is there B 2 F is there D 2 H; D 2 H D 2 H I cannot make the connection now, I need another kind of layer right. So, this is something I need three tracks to give an example here is something that even after floorplanning, there is a lot of opportunity to just do somebody organization of your block. So, that you can actually but you reach the total wire length as well as total number of track will comment right.

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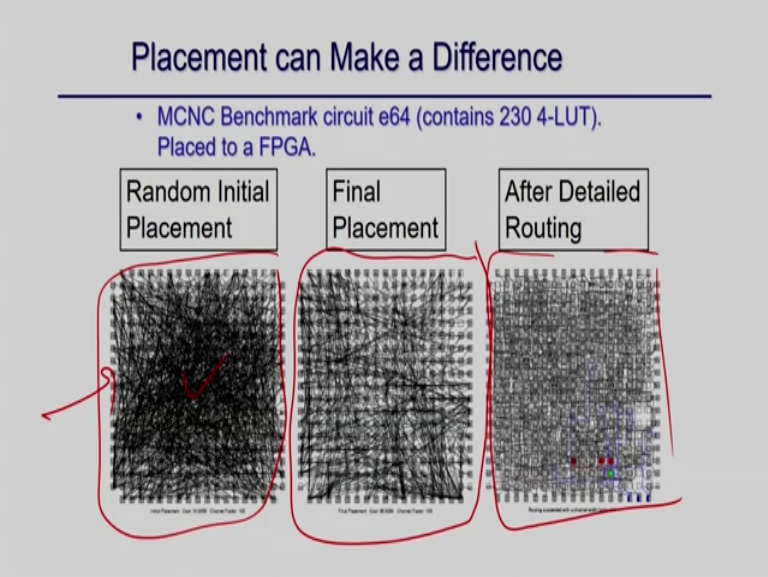

This is what is the objective or the placement step. So, we can see there is a some random initial placement what is generated by floorplan; effectively the placement looks like this right this is just the snapshot of the your layout. But you can make some modification you see the number of wire length become very less here right.

So, you have there this is very parts compare to this dense placement to right and this is the after final routing. So, you can see that you can actually make lot of interconnections less, you just moving your blocks right by doing placements, so the replacement has a huge impact on 5 generating the final round interconnection cost right.

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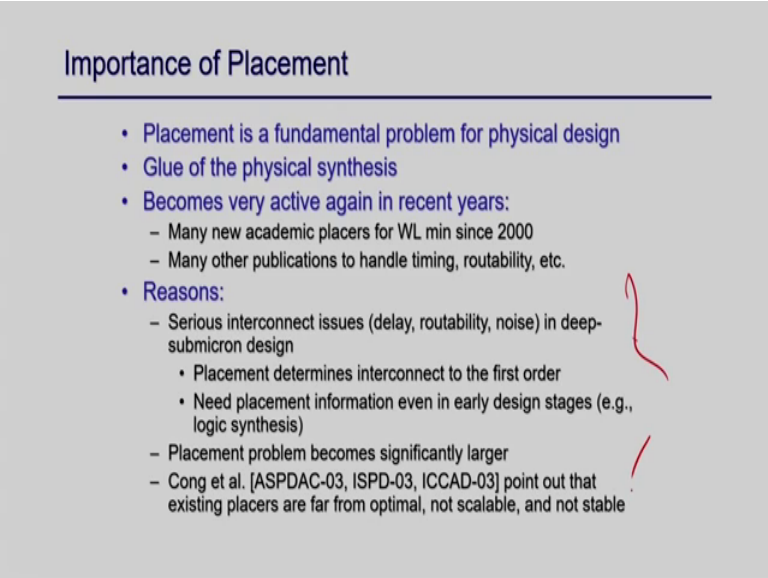

So placement as I mentioned it has a min a many reason. So, basically as I mentioned that rout interconnection cost is going more day by day right. So, when the placement become important just to reduce the total over interconnection cost right.

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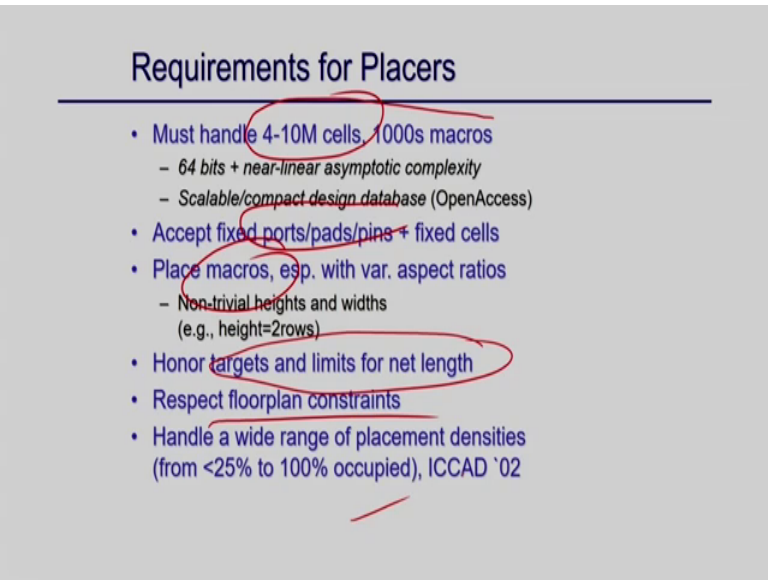

So, this is something is important and the problem in the pressure is that now is the number of 100 million cells right, we have maybe 10 million cycle. And we have to also place this macros like this dsp's and all those and you also where to place the ports, pads everything have to find out. You have to also find out the limit and the owner the target

and limit of its length net length respect the floorplan constraint and all those things. So, we have to placement has to satisfy all these kind of constraint ok.

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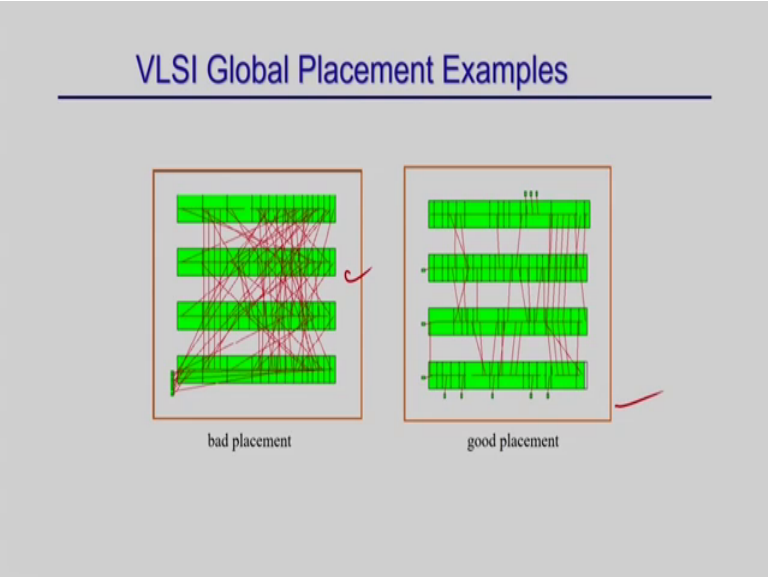

So, here is also an another example that bad placement. So, these are all components are placed and this is the interconnection you just see there lot of crossing right. And here if you just reorganize them you can have a good placement the number of wire length is less. So, placement does this make a good placements so, that is your total wire length is reduced.

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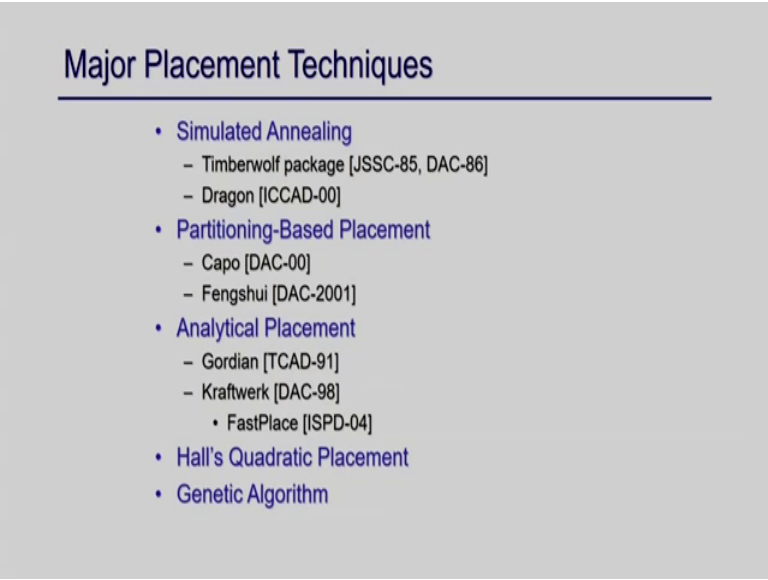

So, again in placement also since an it is a also another n p complete problem you have various approaches like simulated annealing, partition based approach analytical approach and so, on. And we again I am not going to detail of discussion of them, but the basic objective is understood here just to reorganize your placement; I mean repositioning a block; So, that you can reduce your total area and primary total wire length.

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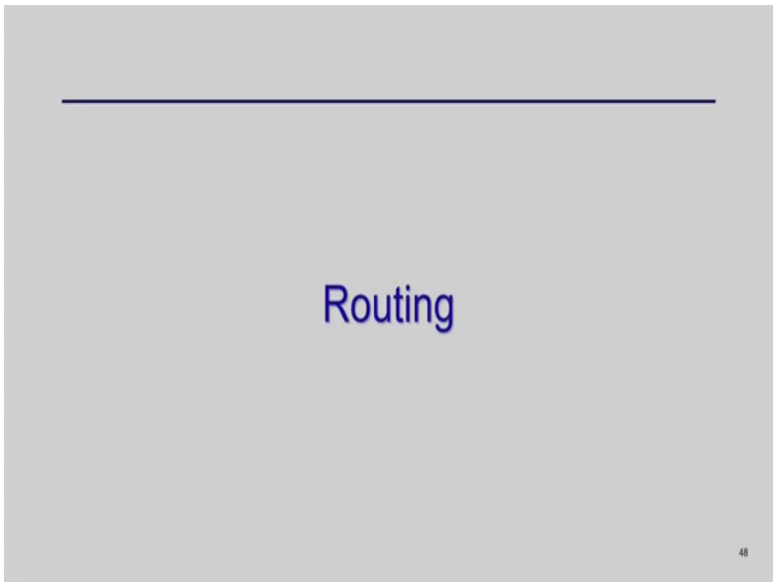

So, I will move on want to routing now. So, I know the positions of each block is fixed; they are final I cannot change the position now, but I have to make the physical connection. So, I know this block are placed here, this block is placed here, this block is placed here and I have to make this connections now right and this is what is routing. And you can see here I make this connection like this; so to remember that finally, this connection cannot go like this right.

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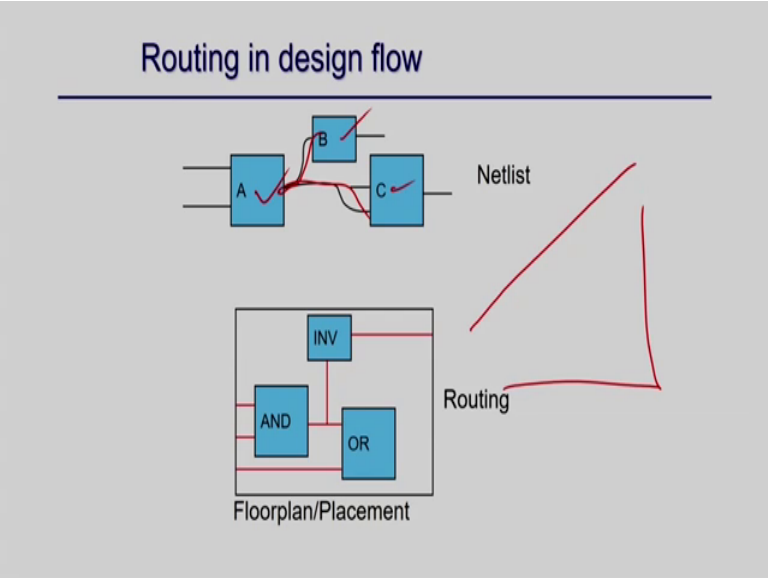

It has to be go vertically, or horizontally you have track vertical and horizontal track you have to make the connection through this right. So, ah; so, the routing problem is that is after floorplanning or placement.

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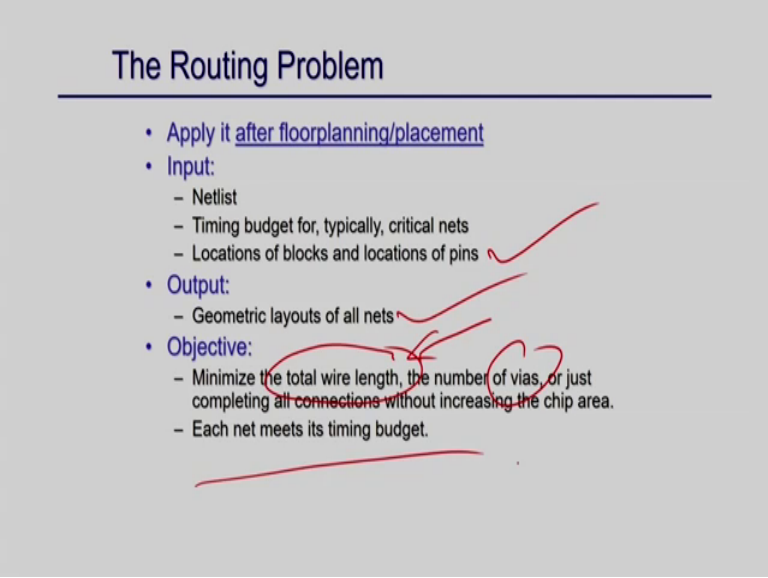

So, you have an Netlist; that means, is component positions and the timing budget that is this for each net it should meet this much of timing and the location of block location of pins and output is the actual geometric layout of all nets ok. And your objective is to actual this is how when the actual interconnection happening.

So, your actual objective is to minimize the total wire length right and also the number of vias I will just discuss now and your also each net should meet timing budget. So, that is what is the routing problem.

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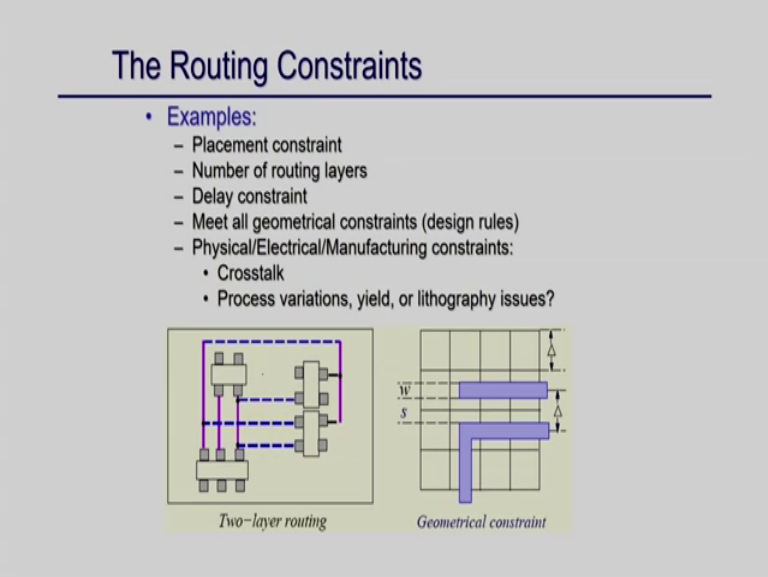

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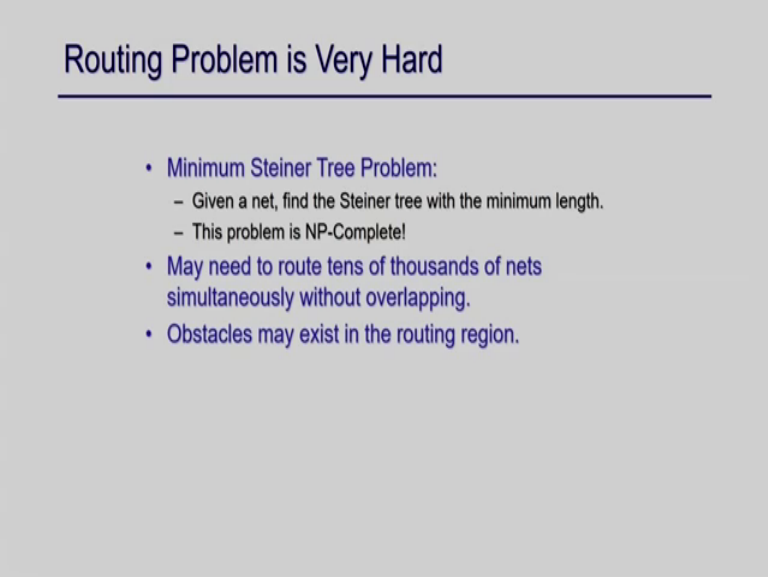

So, routing this routing problem has to be handled here.

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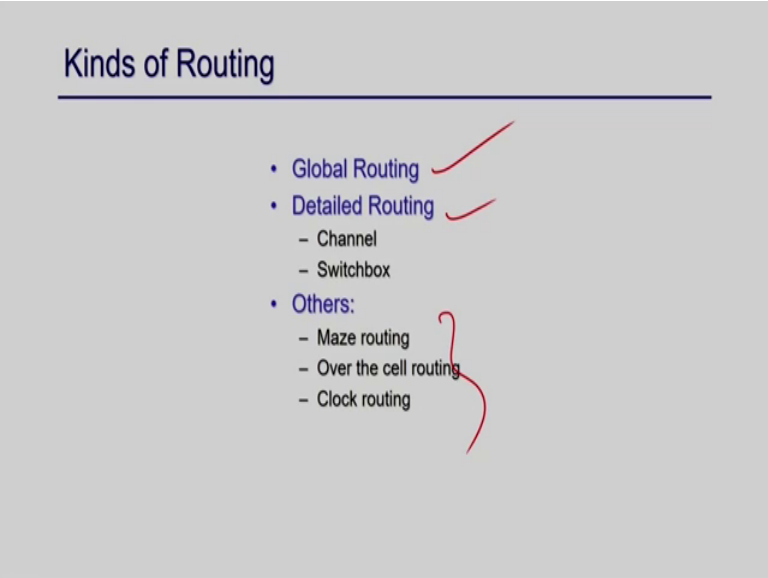

So, the routing has two types first is global routing, the second is detailed routing and the other kind of techniques are there like clock routing or cell routing maze routing which I will not cover here. So, primary; so, initially what is happening here; so, here is this things is there the routing is has two phase.

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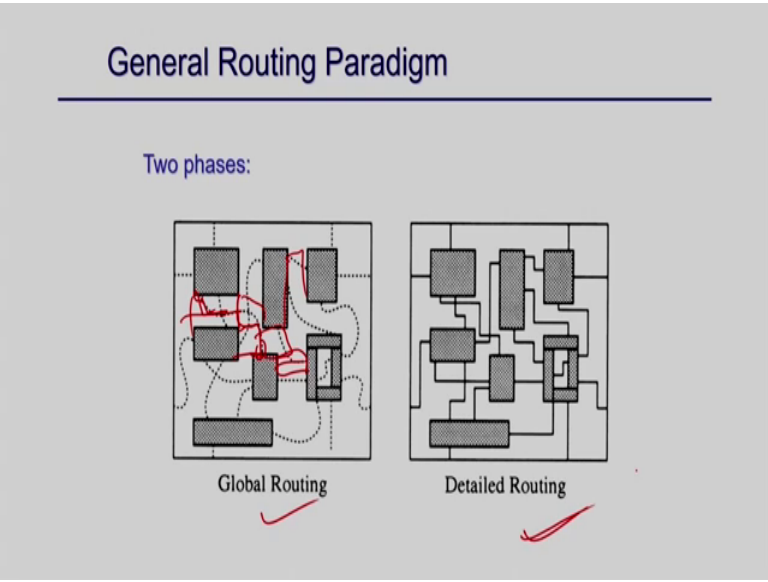

First is global routing the second is the detailed routing so; that means, what I just decide keep from this connection to this connection this will go through this part of the circuit and through this part of the circuit and through this part of the circuit; this is I decide not

exactly the track through exact which tracks will go through which is called global routing.

In global routing I just decide through which part of the circuit of which are the channels through which to go that I decide. For examples thus the for example, say for these I just decided to go through this track plus this track something like this. So, that is what I, but I do not finalize exact track number here and what is done in the detail routing. So, it has two faces global routing and detailed routing.

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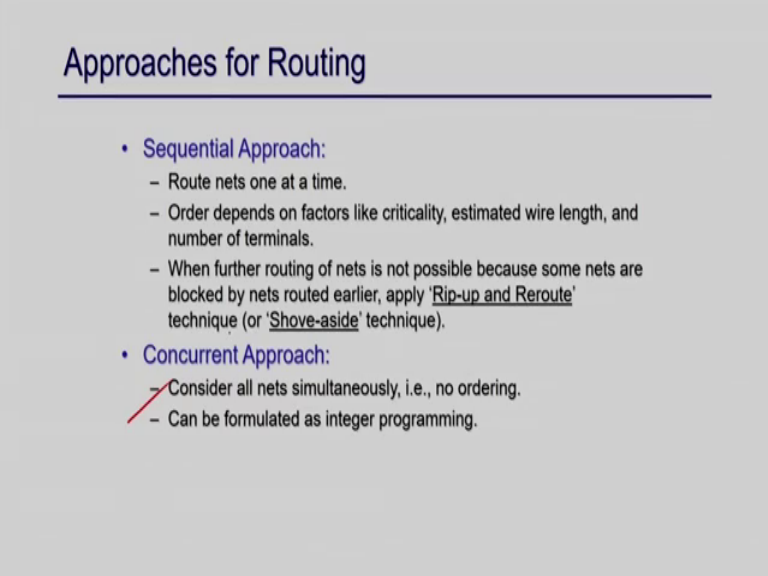

So, again this routing can a two approach in sequential approach you take a one net and you try to rout that one at a time and maybe after some day you find a situation that is the router routing is not possible maybe one of the channel is over congested you cannot put another signal through that.

So, you can actually rip up and reroute; that means, you ignore some of the things you draw move back and again restart on placing to somewhere else. So, this is a sequential approach or in conquer concurrent approach also, you can take all the net simultaneously I will try to do them at the same time ok.

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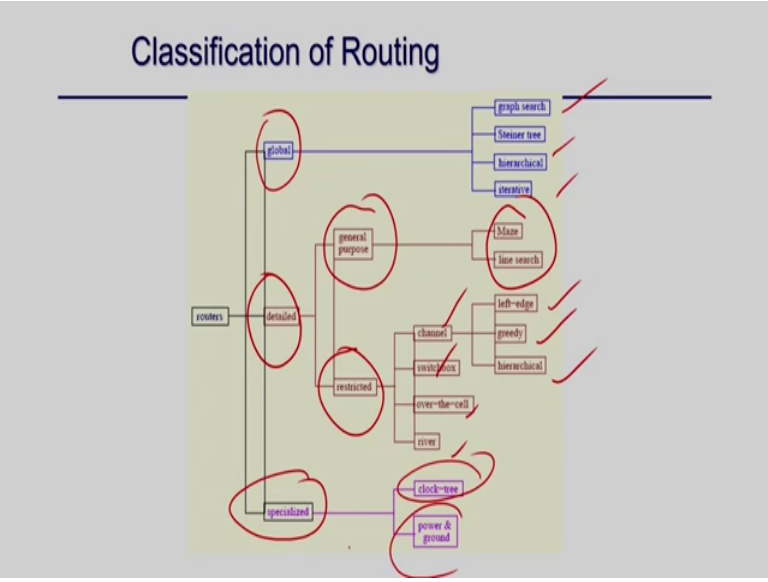

In the routing as I mentioned is the primaries global routing and then detail routing; global routing has different kind of a approach. In a detail routing also general purpose in smaller case usually have a maze routing or line such; in restricted one I can have a channel routing switch box over the channel river and so, on.

And for channel routing we usually apply left edge of algorithm greedy algorithm or hierarchical you know I am not going to detail of them. And the specialized one like routing the clock your or the power is after circuit right. So, if you just go into the; I will just define the global routing problem now.

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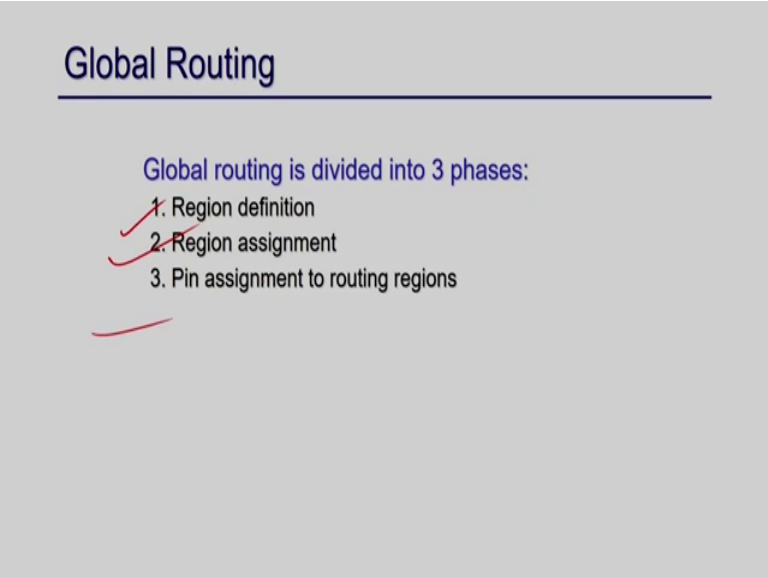

Basically the global routing has three phase that the region definition, region assignment and pin assignment ok.

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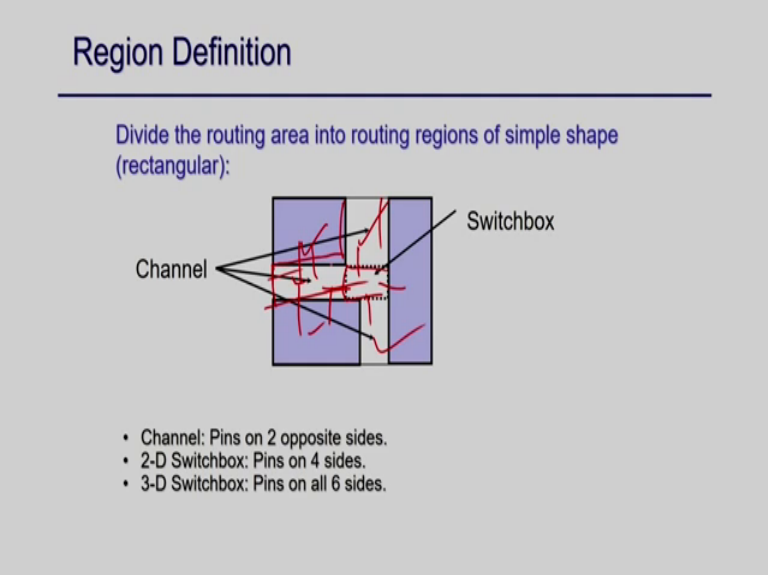

So, what is the region definition? So, basically when your channel between; So, there is a part of the circuit which is basically between two blocks which is called channel. So, this is also a channel and you have this is also a channel and this is a switchbox because this has a multiple (Refer Time: 55:19) data can come from this side, this side, this side as

well as this side. So, which have a more 4 input; so, it has only if data can come only from this portable have only in a two side that is channel and that is switchbox.

So, based on that routing area you decides the channel number you have to basically define the reason that I have in this graph I have basically a three channels; I have three channel and one ride. Because after this detail routing, I have to say this particular connection go through this is a channel 1, this is channel 2, this is channel 3.

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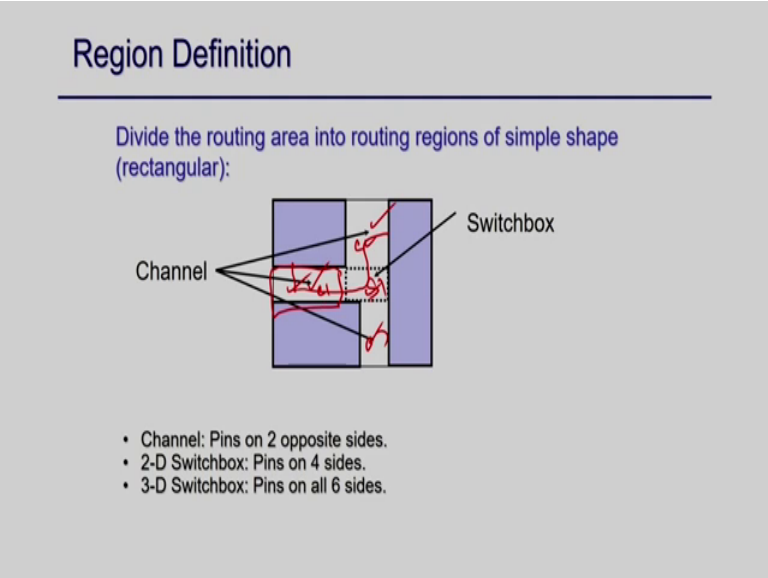

And this is a switchbox 1; I have to say that I have this connection goes through this to this; that means, is covered to C 1 switch box and C 2; then whenever I am going to detail routing of a channel C 1; I do take care of this node right this particular connection.

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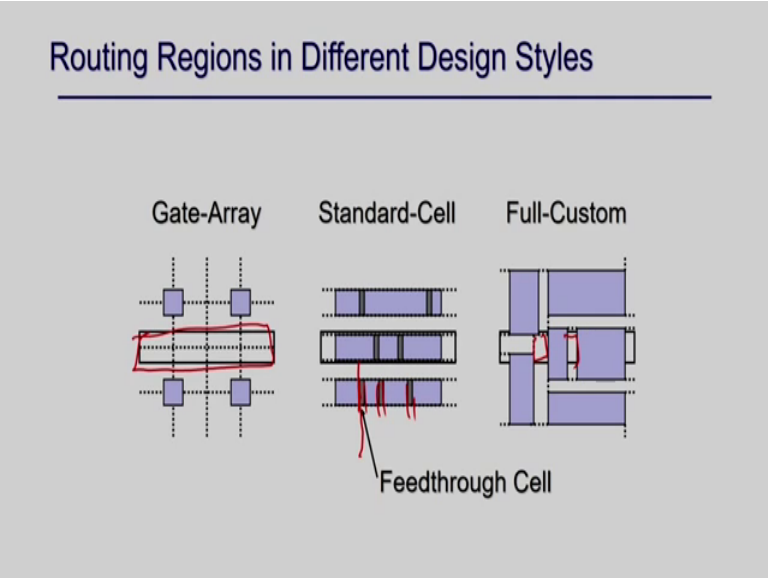

So, this is what is the something. So, basically I just assign first you have to design how many region are there, how many channels are there are, how many switch box are there that I am going to decide first which is region definition.

And then this is the and so, far this is just to say is that for get array that is FPGA; this region is something like this right. So, this is what is the regions because there they connect inter connection area is very fixed. Standard cell I have to make the I have to make a connection from this to this the feed through.

So, these are the channels right and for full custom array we have all the option you can have a switch box and channels and all the possibilities will come which is ASIC design ok.

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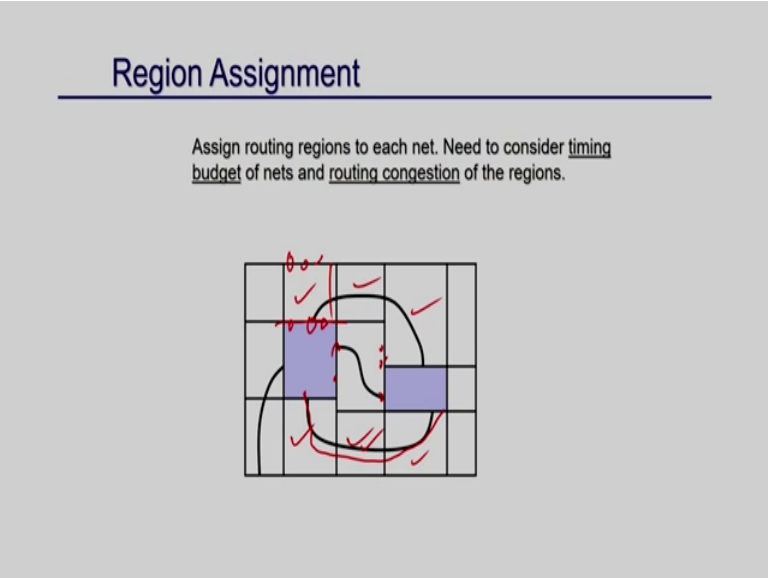

So, after that as a mention the first is reason you define how many channels are there, how many switch box are there; then you make the actual connection and you assign this region assign this particular need go through this switchbox the switchbox are the switchbox at this regions right; this go through this channel this channel or this switchbox something like this.

So, I have to assigned the channel and region or switch box to each net which is called region assignment and then this let us forget about that.

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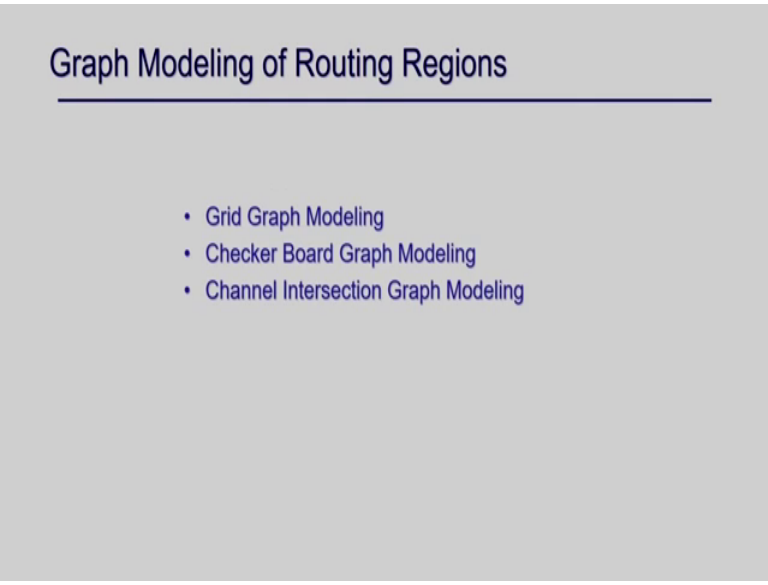

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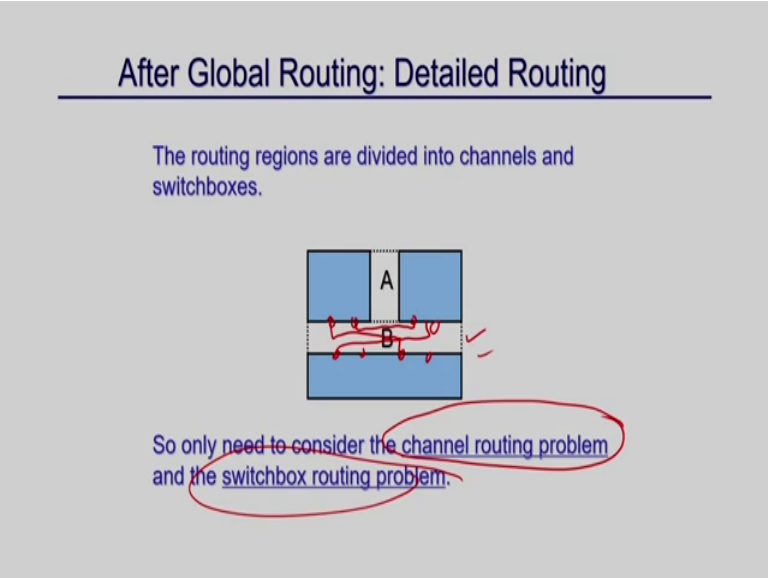

And then the finally after this is a pin assignment, pin assignment something you this then final as a mention here after that you actually make the pin assignment. Because what is happening here once you finalize one particular channel you know how many pin are there how many pins are there right.

Similarly for this I know how many inputs are coming how many pins at this side. So, that is what is called pin assignments after this is decide the pin of this pin assignment for each channel or the switchbox and once this is done I am going to go for this detail routing.

So, you can see that suppose this is one my channel I know for this particular channel 4 pin here right. So, these are the pin positions these are the pin positions and I know that I have to make a connection from this to this pin or maybe this pin to this pin and so, on right. So, I know the pin configurations and all those then I have to make actually the actual connection in this channel at a time so, that I can reduce the number of track here right that is what is called channel routing problem.

And whenever you have switch box which has connection for all 4 to side that is a switch box problem ok.

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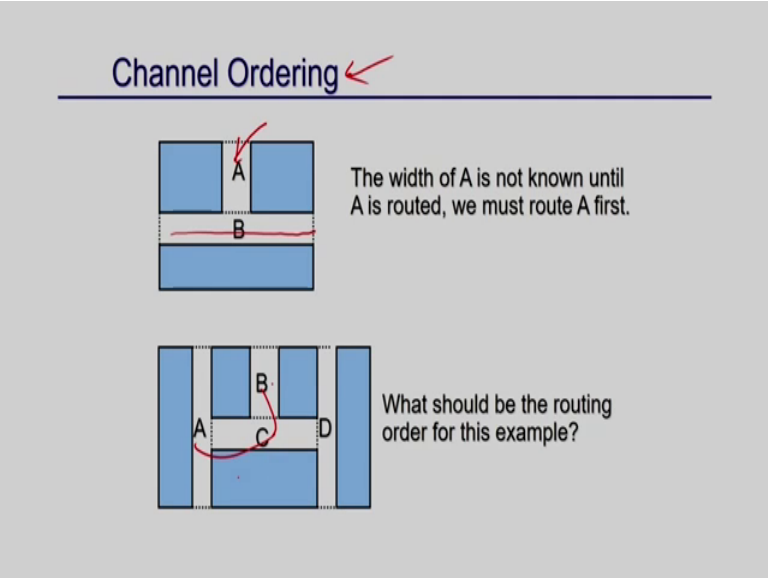

So, as I mention then again the one important concepts that is channel routing channel ordering. So, suppose; so, I have to decide the width of this; so, if you I do not know that width of A; I cannot decide the way that total width of this B right. So, I have to; so, I have to decide A first then B right so, but in some synergy may circular dependency would have to do B, then you have to do C if you are to do C A and something like this.

So, then it will be a (Refer Time: 58:58) circular dependency and there may not be a; so, you have you cannot have a basically a specific order right.

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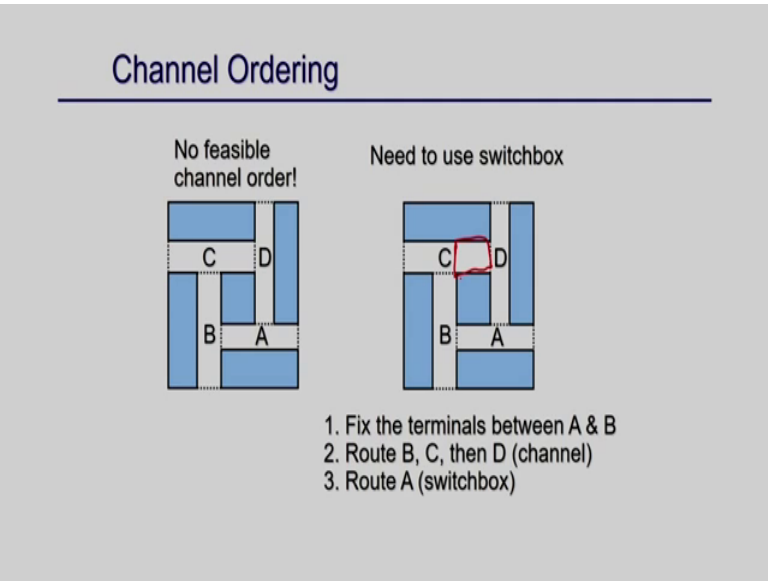

So, then in that sometime they basically you need a switch box. So, why you need a switch box? You can actually define some portion of the circuit which is basically switch box and that. So, that you can actually reduce a dependency and you can actually make it channel order ok.

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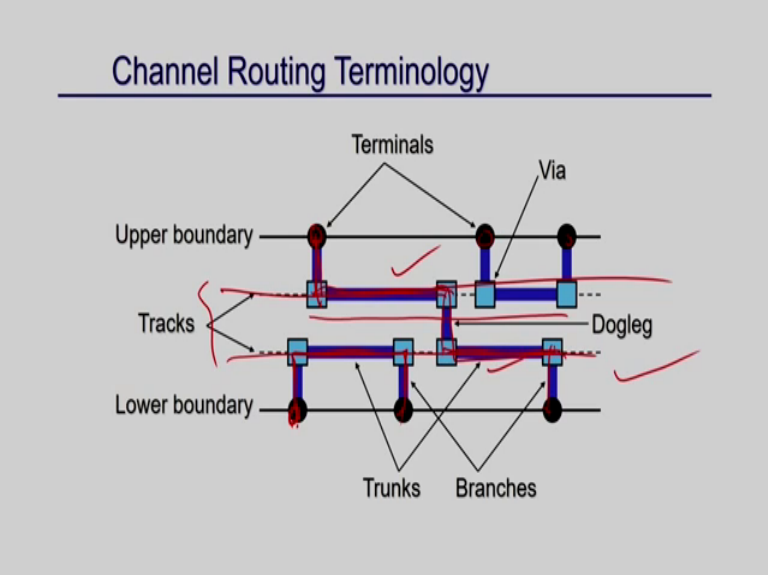

So, once this channel; so, there are some other terminology ratio now I know that terminal each side and I have to make the connection. So, you can make this connection to this is track. So, you your objective is to reduce the number of tracks and so, I suppose for example, you can make the connection only through 1 track or may be for one connection if you needed 2 track this is 1 track, this 1 track. So, that is what is called dogleg that this because you cannot go through this because I will overlapping here in the track which is not allowed.

So, you probably you have to break this the whole interconnection into two parts this is one part and this is one part through which you make this dogleg connection you break the whole connection 2 tracks ok. So, this is the kind of terminology should aware of that in the channel, the number of pin configuration is given and what are the connection I have to make that is also given. And you tried to put all this connections in minimum number of tracks and this is something and sometime you make the connection the hell whole connection in 1 track or you have to just split it and which is called dogleg ok.

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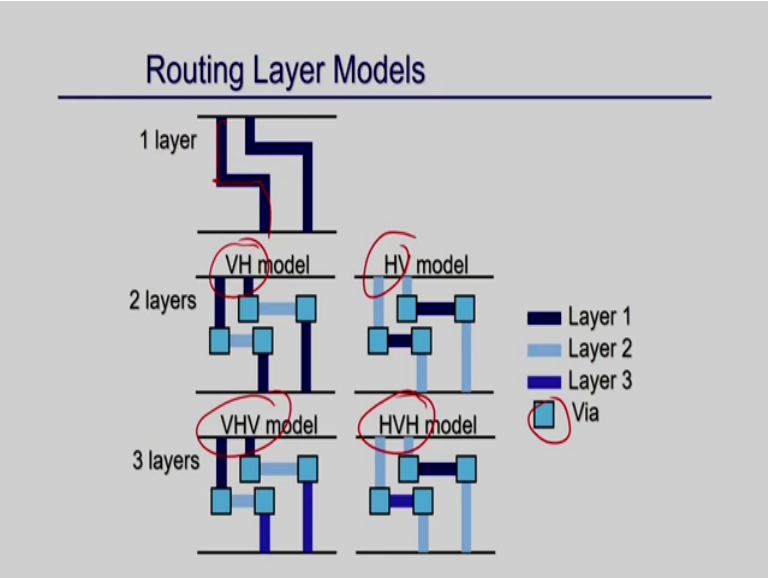

And your layer maybe the may be two layers or maybe you have to make all the connection into one layer what you have the horizontal is one layer. So, you have a one horizontal layer followed by one vertical layer. So, that whenever you are going from the horizontal to vertical you go through some via right you can understand that there is this horizontal layer. So, you make the horizontal connection here and then suppose I have to make the vertical connection in this layer. So, I have to make a connection through this which to b r to this right.

So, which is call VH or HV may be horizontal up then vertical up horizontal; horizontal and vertical like this or may be a three layer two vertical layer one horizontal layer what to horizontal on vertical layer. So, this all things are possible I am again I am not going to going into detail of this, but when you are actually working on the channel routing problem these are the terminology should come to you right.

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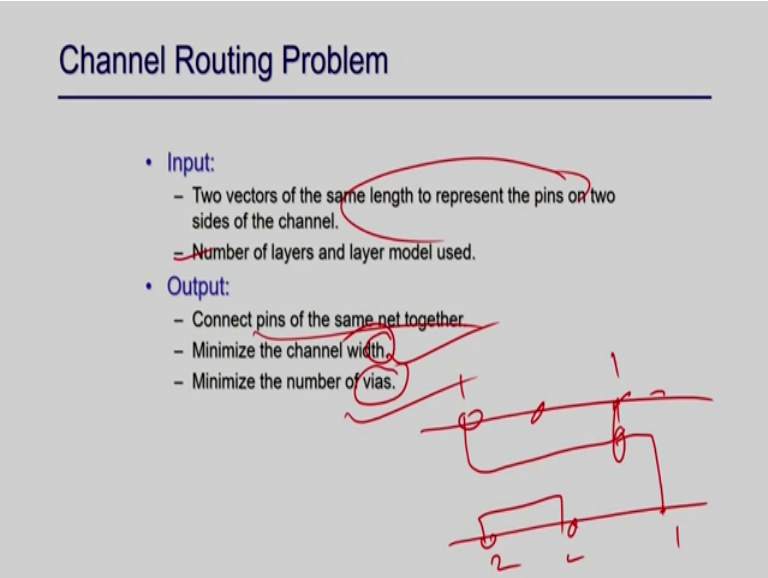

And your channel routing problem is as I mentioned there are two vector of same length pins are there the pins are given of two side of this channel. And there the number of layer is given whether is a VH model, HV model, HV H model and those that is also given and you actually and the pin number. So, this is 1, this is 1 and this is 1; that means, you have to make the connection like this right.

So, what about the pin number? That will actually have to connect those; so, this is 2, this is 2; that means, I have to connection through this right. So, this is also given to you and you have to make the connection pin together and minimize the total channel width, number of vias with means the number of tracks right, the number of channel will means number of tracks and also try to make a lot of vertical connection also this vias will may of a vertical connection who is also try to reduce hm.

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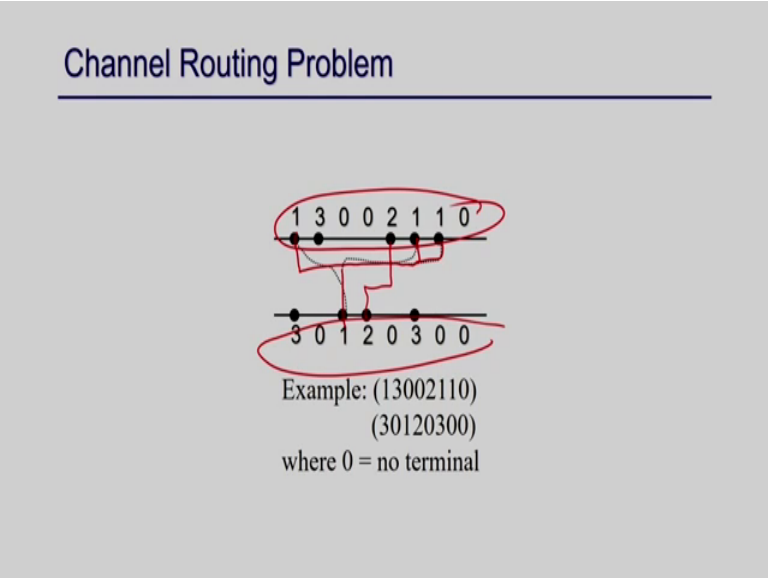

As I mention. an example; so, this is 1, this is 1, this is 1, I want to make a connection like this right. Similarly this is 2, this is 2 means I have to make a connection like this. So, this is what is how the problem is given it is as given this set and this set right this is and you have given whether it is a VH; HV on this and you have to solve this right.

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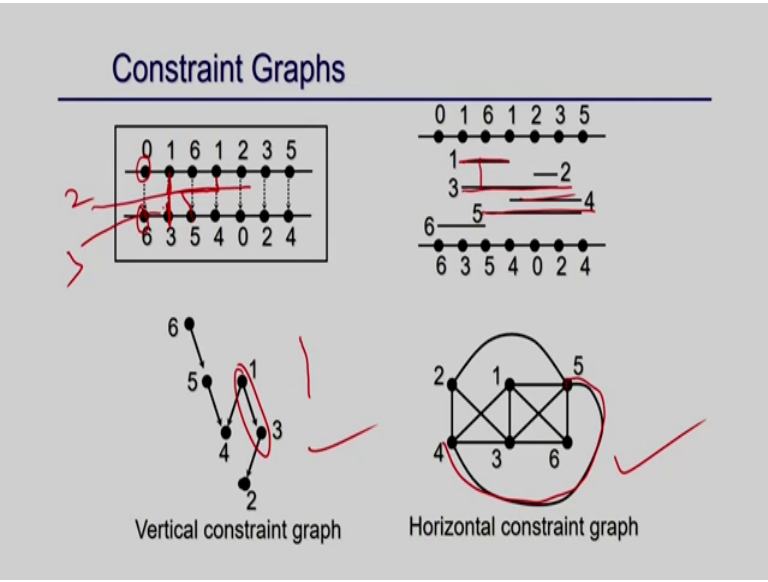

So, you can see here there can be various constraint right. So, if you have a this and this; that means, they cannot be put in the same track because they are overlapping. So, this is horizontal constraint we can construct a constraint graph like this for example, this 5 this

and this 5 and 4; they have a overlapping; so, 5 to 4 have a edge right similarly; so, this is a horizontal constraint.

Similarly if 0 of there so, you cannot they are actually do not cross in horizontal line right for a what I am try to says that if 6 is there. So, basically say 1 to 3 right, 1 to 3 there is a connection so; that means, what about the connection is happening. So, 1 to 1 ah; this 3 cannot go here right we can go cross this. So, what if this is the track say 2 the connection from 3 has to happen below this at least from 3, it cannot go crossing this right.

So, that is what is called vertical constraint. So, should have those you can actually extract all those vertical constraint and horizontal constraint.

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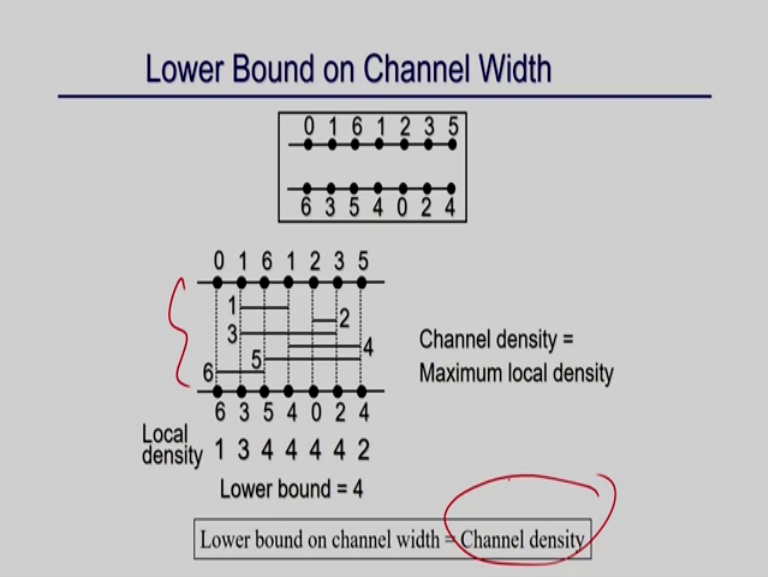

And using that actually you can solve your problem and you can actually identify the number of minimum track required using some logic also it is the channel density.

So, those kind of approach and there are lot of algorithm is also left is algorithm another kind of solving algorithm which actually can handle dogleg connections or say VH V model and all. Again I am not going to detail of those algorithms, but just to give you the problem flavor what is what is the channel routing problem and what is happening here ok.

Similarly we have a switch box routing; I just talked about switch box I mean channel because it has only two kind of side upside and downside button switch box I have connections all from all 4 sides. So, it is more complex problem; so, that is also there. So, in summary I have discussed about this physical synthesis flow.

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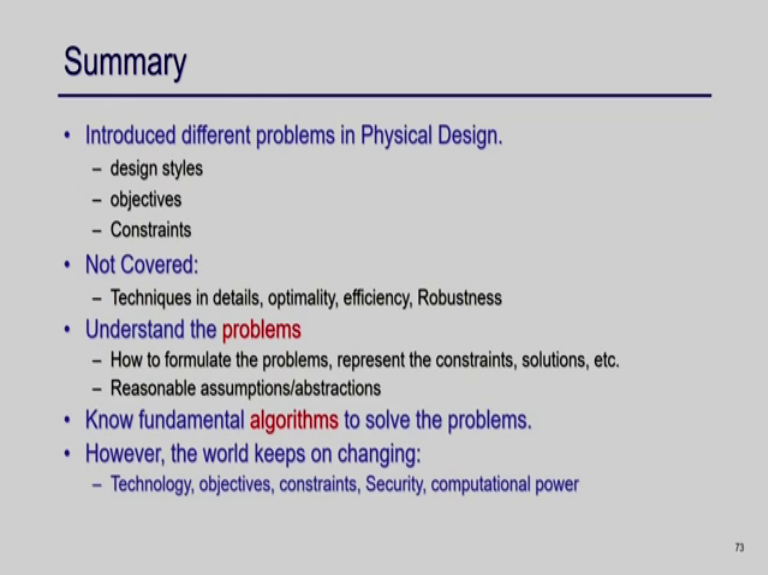

I give a very brief overview of this physical synthesis what is placement, what is floor planning, what is partitioning initially and then what is routing and how what is the problem definition there what is I have not covered is that the techniques detailed technique in detail; their efficiency, their robustness those part I have I do not covered here. So, what the objective of this particular lecture is something just to give the understanding the problem, how to formulate that problem represent that constraint and how to represent solution etcetera.

And you just think about what kind of assumption is there, what are the constraints are there and also how we can fundamental algorithm to solve this problem like this heuristics approach or sometime in left edge algorithm or those things or maybe sometime we will go for genetic algorithm or sometimes simulated (Refer Time: 65:09) algorithm.

But a but without going into detail of the solution we just talk from very over view level. And also this physical synthesis still relevant in the sense that the value changing you the new kind of constraints are coming like this, you have security constraint nowadays, you

can have reliability, you can have other new new constraints like the criticality of your power of those things.

So, there is always a scope to revolve some new kind of placement floor planning or routing algorithms which can actually satisfy this kind of new new strategies ok. So, with this I conclude this particular module and.

Thank you.