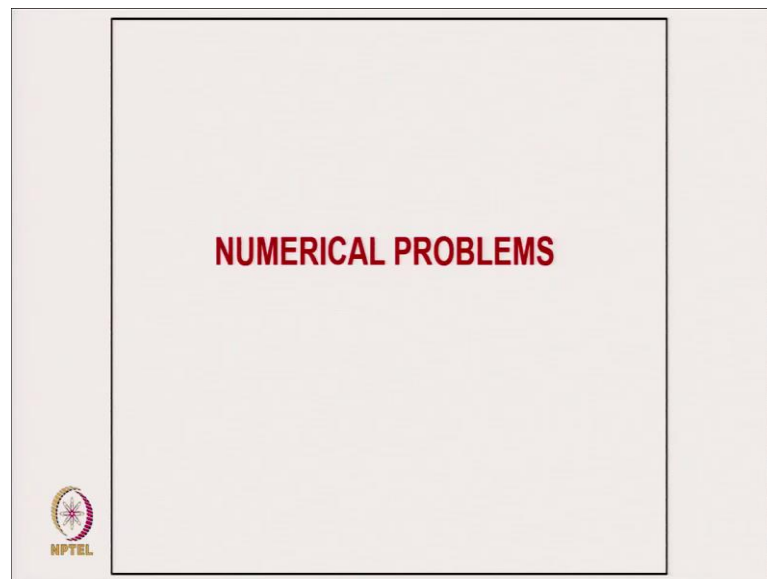


Power Quality
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Numerical Problem
Lecture - 35
Improved Power Quality Converters - AC-DC Buck-Boost Converters (Contd.)

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Welcome to the course on Power Quality. We will discuss the numerical examples on the single-phase power factor corrected buck-boost converter.

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1. Design a single-phase power-factor corrected AC-DC non-isolated buck-boost converter in CCM (continuous current mode of conduction approach) operating at 20 kHz with following specifications: input: $V_s=220$ V rms, 50Hz, single-phase AC supply, DC output: $V_{dc}=180$ V, $P_o=900$ W with output voltage-ripple less than 2%.

The diagram shows a single-phase buck-boost converter in CCM. It consists of an AC input V_s connected to a filter with capacitor C_f and inductor L_f . The filtered AC is connected to a diode bridge rectifier (DBR). The output of the DBR is connected to a boost stage with inductor L and diode D . The output of the boost stage is connected to a buck stage with MOSFET S and capacitor C . The output of the buck stage is connected to a load. The output voltage is V_o and the output current is I_o . The MOSFET gate voltage is V_{sw} and the MOSFET current is I_{sw} . The DC output voltage is V_{dc} . The output voltage ripple is ΔV_o . The output current ripple is ΔI_o . The output voltage ripple is less than 2%.

Starting with the first problem. Design a single-phase power-factor corrected AC-DC non-isolated buck-boost converter in continuous conduction mode operating at 20 kHz with the following specifications: Input voltage = 220 V RMS, frequency of 50 Hz, single-phase AC supply, the DC output of 180 V and power output 900 W with the output voltage-ripple less than 2 %.

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Solution-
 The output voltage V_{dc} of the buck-boost converter is given as,

$$V_{dc} = \frac{D}{1-D} V_{in}$$

The converter input voltage is given as,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$$

Therefore the value of duty ratio D can be given as,

$$180 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.476$$

The input current

$$I_{in} = \frac{P_o}{V_{in}} = \frac{900}{198} = 4.55A$$

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- Considering the 30 % current ripples **Design of Inductor (L)** for continuous Current Conduction


$$L_{\min} = \frac{D \cdot V_m}{0.3 \cdot I_m \cdot f_s} = \frac{0.476 \cdot 198}{0.3 \cdot 20000 \cdot (900 / 198)} = 3.5 \text{mH}$$

The inductor is selected greater than the above calculated value **is 4 mH** i.e. to ensure **CCM** of operation.

- Considering the condition of maximum ripple at minimum output voltage the **design of DC link capacitor** is made as,

$$C_d = \frac{I_{dc}}{2\omega \Delta V_{dc}} = \frac{P_o / V_{dc}}{2\omega \delta V_{dc}} \quad C_d = \frac{P_o}{2\omega \delta V_{dc}^2} = \frac{900}{2 \times 314 \times 0.02 \times 180^2} = 2.21 \text{mF}$$

The maximum ripple voltage across C_d is considered as 2% of V_{dc} . The value for DC link capacitor is selected **as 2.4 mF**




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- The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics. **Therefore LC filter is designed as,**

$$C_{\max} = \frac{I_m}{\omega_s V_m} \tan(\theta) = \frac{(P_o \sqrt{2} / V_s)}{\omega_s V_m} \tan(\theta) = \frac{(900 \sqrt{2} / 220)}{314 \times 220 \sqrt{2}} \tan(1^\circ) = 1.1 \mu\text{F}$$

Where V_m and I_m are the supply voltage and current. θ is the displacement angle between supply current and supply voltage. The filter capacitor is selected **as 440 nF**.



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While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. Therefore, an accurate filter design is essential for PFC converter. Higher order harmonics introduced in input side by high switching frequency of IGBT switches is eliminated by using LC filters. The filter inductor design can be given as,

$$L_s = 0.05 \left(\frac{1}{\omega_c} \right) \left(\frac{V_s^2}{P_o} \right)$$

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.05 \left(\frac{1}{\omega_c} \right) \left(\frac{V_s^2}{P_o} \right)$$

$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 440 \times 10^{-9}} - 0.05 \left(\frac{1}{314} \right) \left(\frac{220^2}{900} \right) = 5.83mH$$

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$. The filter inductor is selected as 6 mH.

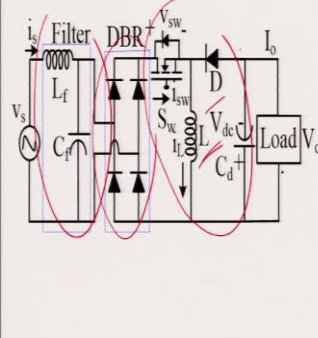
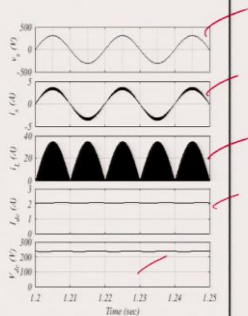



While the designing the filter inductor, the source inductor is taken into consideration. An accurate filter design is essential for power factor correction converter, as the higher order harmonics induced at supply by the switching of solid state switch is eliminated by the LC filter.

The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 06:03)

2. Design a single-phase power-factor corrected AC-DC non-isolated buck-boost converter in DCM (Discontinuous Current Mode of operation also known as voltage follower approach) operating at 20 kHz with following specifications: input: $V_s=220V$ rms, 50Hz, single-phase AC supply, DC output: $V_{dc}= 240V$, $P_{rated}=500 W$ with output voltage-ripple less than 2%.

Coming to the 2nd example. Design a single-phase power factor corrected AC-DC non-isolated buck-boost converter in discontinuous current mode operation, operating at 20

kHz with the following specifications: Input voltage of 220 V, 50 Hz, single-phase supply, and DC output of 240 V, and power related is 500 W with the output voltage-ripple of less than 2%.

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Solution-

The output voltage V_{dc} of the buck boost converter is given as,

$$V_{dc} = \frac{D}{1-D} V_m$$


The converter input voltage is given as,

$$V_m = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$$

Therefore the value of duty ratio D can be given as,

Also,

$$240 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.547$$

$$I_m = \frac{P_o}{V_m} = \frac{250}{198} = 2.53A$$


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• **Design of Inductor (DCM)**


$$L = \frac{V_m D}{2I_m f_s} = \frac{R_m D}{2f_s} = \left(\frac{V_s^2}{P_i} \right) \frac{D}{2f_s}$$

In the above expression, a high switching frequency is considered i.e. $f_s = 20$ kHz where R_m gives the input side resistance.

The **design of inductor** at rated operating condition is given as

$$L = \frac{V_m D}{2I_m f_s} = \frac{198 \times 0.547}{2 \times 2.53 \times 20000} = 1.07mH$$

The inductor is selected as the one tenth of the calculated value
i.e. 100 μ H to ensure DCM of operation.



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• Selection of DC link Capacitor

Considering the condition of maximum ripple at minimum output voltage the design of DC link capacitor is made as,

$$C_d = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_{rated}/V_{dc}}{2\omega\Delta V_{dc}} \quad C_d = \frac{P_{rated}}{2\omega\Delta V_{dc}^2} = \frac{500}{2 \times 314 \times .02 \times 240^2} = 0.7mF$$


The value for DC link capacitor is selected as **1 mF**.

• Design of Filter Capacitor

The design of filter capacitor is given as,

$$C_{max} = \frac{I_m}{\omega L_m} \tan(\theta) = \frac{(P_{rated} \sqrt{2}/V_s)}{\omega L_m} \tan(\theta) = \frac{(500\sqrt{2}/220)}{314 \times 220\sqrt{2}} \tan(1^\circ) = 574.3nF$$

Where V_m and I_m are the supply voltage and current. Filter capacitor is selected as **320 nF**.



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• Design of Filter Inductor


While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. Higher order harmonics introduced in input side by high switching frequency of IGBT switches is eliminated by using LC filter. Therefore, an accurate filter design is essential for PFC converters, **filter inductor design** can be given as.

$$L_s = 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 320 \times 10^{-9}} - 0.05 \left(\frac{1}{314} \right) \left(\frac{220^2}{500} \right) = 4.37mH$$

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

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3. Design a single-phase power-factor corrected AC-DC non-isolated **Cuk converter in CCM** (all components are in CCM) operating at 20 kHz with following specifications: input: $V_s=220V$ rms, 50Hz, single-phase AC supply, DC output: $V_{dc}=300V$, $P_{rated}=1900W$ with output voltage-ripple less than 2%.

The diagram shows a Cuk converter circuit with a DBR (Diode Bridge Rectifier) and a filter. The input is a single-phase AC supply V_s . The circuit includes an inductor L_s , a diode bridge, a filter capacitor C_f , a boost inductor L_{11} , a Cuk inductor L_{12} , a diode D , and a load inductor L_{load} . The output is a DC voltage V_{dc} . Waveforms show the input current i_s , the capacitor voltage V_{C1} , the inductor current i_{L1} , and the output voltage V_o . A THD plot shows the fundamental current I_{11} is 13.21A with THD=3.96%.

Coming to the 3rd example. Design a single-phase power factor corrected AC-DC non-isolated Cuk converter operating in continuous conduction mode at 20 kHz with the following specification: Supply voltage = 220 V/50 Hz, single-phase AC supply, and DC output voltage 300 V, and power is 1900 W with output ripple of 2%.

(Refer Slide Time: 13:06)

Solution-

The output voltage V_{dc} of the boost-buck converter is given as

$$V_{dc} = \frac{D}{1-D} V_{in}$$

The converter input voltage is given as,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$$

Therefore the value of duty ratio D can be given as,

$$300 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.602 \quad I_n = \frac{P_o}{V_{in}} = \frac{1900}{198} = 9.6A$$

Design of Inductor (L_{11}) for continuous Current Conduction, for 40% ripple in current

$$L_{11} = \frac{V_{in} D}{\Delta I_{L1} f_s} = \frac{0.602 \times 198}{0.4 \times (1900 / 198) \times 20000} = 1.55mH$$

The inductor is selected greater than the above calculated value **i.e. 2 mH** to ensure CCM of operation.

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Design of Inductor (L_{o1}) for continuous Current Conduction, for 30% ripple in current

$$L_{o1} = \frac{V_{dc}(1-D)}{\Delta I_o f_s} = \frac{300 * (1 - 0.602)}{0.3 * (1900 / 300) * 20000} = 3.14mH$$

The inductor is selected **as 3.5 mH** to ensure CCM of operation.


The voltage across the capacitor C_1 is given as,

$$V_{C1} = \frac{V_m}{(1-D)} = \frac{198}{0.4} = 495$$

Considering the condition of 10% ripple, the design of intermediate capacitor C_1 is made as,

$$C_1 = \frac{I_m(1-D)}{\Delta V_{C1} f_s} = \frac{9.6 * (1 - 0.602)}{0.1 * 495 * 20000} = 3.9\mu F$$

The value for intermediate capacitor is selected **as 4 μF**



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Considering the condition of maximum ripple at minimum output voltage the **design of DC link capacitor** is made as,

$$C_d = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_{rated}/V_{dc}}{2\omega\delta V_{dc}} \quad C_d = \frac{P_{rated}}{2\omega\delta V_{dc}^2} = \frac{1900}{2 * 314 * .02 * 300^2} = 1.68mF$$


The maximum ripple voltage across C_d is considered as 2% of V_{dc} . The value for DC link capacitor is selected **as 2 mF**.

The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics.

Therefore **design of this LC filter** can be given as,

$$C_{max} = \frac{I_m}{\omega_L V_m} \tan(\theta) = \frac{(P_{rated} \sqrt{2}/V_s)}{\omega_L V_m} \tan(\theta) = \frac{(1900 \sqrt{2}/220)}{314 * 220 \sqrt{2}} \tan(1^\circ) = 2.2\mu F$$

Where V_m and I_m are the supply voltage and current.
Filter capacitor value is taken **as 800nF**.



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While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. Higher order harmonics introduced in input side by high switching frequency of IGBT switches is eliminated by using LC filter. Therefore, an accurate filter design is essential for PFC converters, filter inductor design can be given as,

$$L_s = 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 800 \times 10^{-9}} - 0.05 \left(\frac{1}{314} \right) \left(\frac{220^2}{1900} \right) = 3.86mH$$

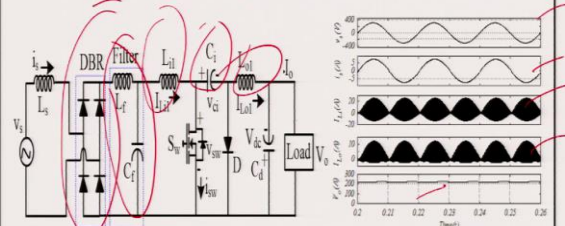

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

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4. Design a single-phase power-factor corrected AC-DC non-isolated Cuk converter in DCM (input inductor, output inductor, and intermediate capacitor are in DCM) operating at 50 kHz with following specifications: input: $V_s=160-270V$ rms, 50Hz, single-phase AC supply, DC output: $V_{dc}=200-260$ V adjustable with nominal value of 220 V, $P_{rated}=850$ W with output voltage-ripple less than 2%.

Coming to the 4th example. Design a single-phase power factor corrected AC-DC non-isolated Cuk converter in discontinuous conduction mode operating at 50 kHz with following specifications: Supply voltage = 160-270 V RMS, 50 Hz, single-phase supply, DC output voltage = 200 to 260 V adjustable with the nominal of 220 V, power output is 850 W with the output voltage-ripple of less than 2 %.

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Solution-

The output voltage V_{dc} of the Cuk converter is given as,


$$V_{dc} = \frac{D}{1-D} V_{in}$$

Design of Inductor (L_1) for Discontinuous Current Conduction,

$$L_{ic} = \frac{V_{in} D}{2f_s} = \frac{R_{in} D}{2f_s} = \left(\frac{V_s^2}{P_i} \right) \frac{D}{2f_s}$$

At minimum supply voltage and maximum DC link voltage, the critical value of L_1 is calculated as,

$$L_{ic200} = \frac{1}{2f_s} \left(\frac{V_{smin}^2}{P_{rated}} \right) \left(\frac{V_{dcmax}}{\sqrt{2V_{smin} + V_{dcmax}}} \right)$$

$$= \frac{1}{2 * 50000} \left(\frac{160^2}{850} \right) \left(\frac{260}{\sqrt{2 * 160 + 260}} \right) = 161 \mu H$$


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At minimum supply voltage and minimum DC link voltage, the critical value of L_1 is calculated as,

$$L_{ic200} = \frac{1}{2f_s} \left(\frac{V_{smin}^2}{P_{rated}} \right) \left(\frac{V_{dcmin}}{\sqrt{2V_{smin} + V_{dcmin}}} \right)$$

$$= \frac{1}{2 * 50000} \left(\frac{160^2}{850} \right) \left(\frac{200}{\sqrt{2 * 160 + 200}} \right) = 141.3 \mu H$$

In the above expression, a high switching frequency is considered i.e. $f_s = 20$ kHz where R_{in} gives the input side resistance. As per the required design the rated input power and rated DC link are considered at minimum supply voltage (i.e., $V_{smin} = 160$ V).

Therefore, the critical value of input inductor is selected lower than L_{ic200} . The inductor is selected as **100 uH** to ensure **DCM** operation.



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The output inductor is calculated at the peak of supply voltage and maximum DC voltage is given as,

$$L_{oc260} = \frac{V_{smin}^2}{P_{rated}} \frac{V_{dcmax}}{2\sqrt{2}V_{smin}f_s} \left(\frac{V_{dcmax}}{\sqrt{2}V_{smin} + V_{dcmax}} \right)$$


$$L_{oc260} = \left(\frac{160^2}{850} \right) \frac{260}{2\sqrt{2} * 160 * 50000} \left(\frac{260}{\sqrt{2} * 160 + 260} \right) = 185 \mu H$$

The output inductor is calculated at the peak of supply voltage and minimum DC voltage is given as,

$$L_{oc200} = \frac{V_{smin}^2}{P_{rated}} \frac{V_{dcmin}}{2\sqrt{2}V_{smin}f_s} \left(\frac{V_{dcmin}}{\sqrt{2}V_{smin} + V_{dcmin}} \right)$$

$$L_{oc200} = \left(\frac{160^2}{850} \right) \frac{200}{2\sqrt{2} * 160 * 50000} \left(\frac{200}{\sqrt{2} * 160 + 200} \right) = 124.9 \mu H$$

Therefore, the value of input inductor is selected lower than L_{oc200} . The inductor is selected as $80 \mu H$ to ensure DCM of operation.



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The critical value of intermediate capacitance C_{1c} is as,

$$C_{1c} = \frac{V_{dc} D}{2V_{cr} R_L} = \frac{P_{rated}}{2 * f_s * (V_{in} + V_{dc})^2}$$


The critical value of intermediate capacitance C_{1c} at minimum DC link voltage, is calculated as,

$$C_{1c200} = \frac{P_{rated}}{2 * f_s * (\sqrt{2}V_{smax} + V_{dcmin})^2} = \frac{850}{2 * 50000 * (270\sqrt{2} + 200)^2} = 25.12 nF$$

The critical value of intermediate capacitance C_{1c} at maximum DC link voltage, is calculated as,

$$C_{1c260} = \frac{P_{rated}}{2 * f_s * (\sqrt{2}V_{smax} + V_{dcmax})^2} = \frac{850}{2 * 50000 * (270\sqrt{2} + 260)^2} = 20.63 nF$$

The capacitor is selected less than the calculated value of C_{1c260} i.e. $15 nF$ to ensure DCM of operation.



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Considering the condition of maximum ripple at minimum output voltage the **design of DC link capacitor** is made as,

$$C_{dc} = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_{rated}/V_{dc}}{2\omega\Delta V_{dc}}$$


The design of DC link capacitor at **maximum DC link voltage**, is made as,

$$C_{d200} = \frac{P_{rated}}{2\omega\Delta V_{dcmax}^2} = \frac{850}{2 \times 314 \times .02 \times 260^2} = 1mF$$

The design of DC link capacitor at **minimum DC link voltage**, is made as,

$$C_{d200} = \frac{P_{rated}}{2\omega\Delta V_{dcmin}^2} = \frac{850}{2 \times 314 \times .02 \times 200^2} = 1.7mF$$

The maximum ripple voltage across C_{dc} is considered as 2% of V_{dc} . The value for DC link capacitor is selected **as 2mF**.



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The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics. Therefore **design of this LC filter** can be given as,

$$C_{max} = \frac{I_m}{\omega_s V_m} \tan(\theta) = \frac{(P_o \sqrt{2}/V_s)}{\omega_s V_m} \tan(\theta) = \frac{(850\sqrt{2}/220)}{314 \times 220\sqrt{2}} \tan(14^\circ) = 976.26nF$$

Where V_m and I_m are the supply voltage and current. The filter capacitor is selected **as 470 nF**.


Filter inductor design can be given as,

$$L_f = 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.05 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

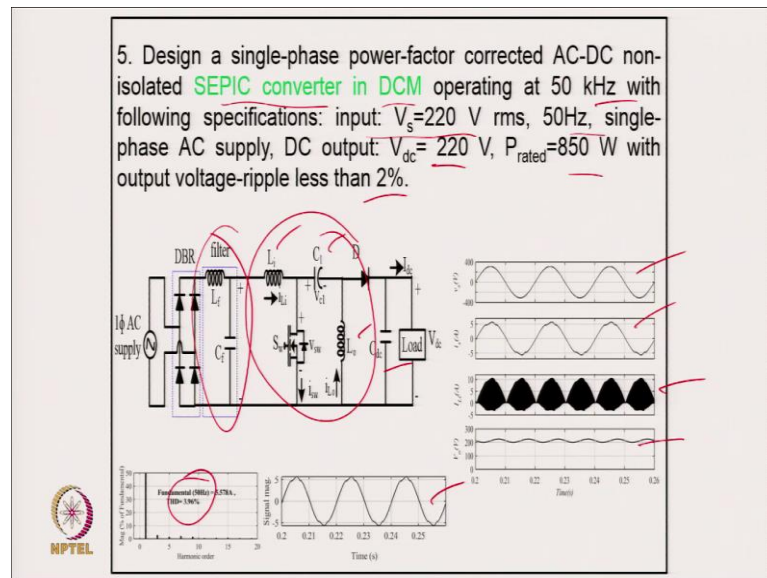
$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 470 \times 10^{-9}} - 0.05 \left(\frac{1}{314} \right) \left(\frac{220^2}{850} \right) = 4.4mH$$

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

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Coming to 5th example. Design a single-phase power factor corrected AC-DC non-isolated SEPIC converter operating in discontinuous conduction mode at 50 kHz with the following specifications: Supply voltage = 220 V RMS/ 50 Hz, single-phase supply, and output voltage is 220 V, and rated power is 850 W with the output voltage-ripple of less than 2 %.

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Solution- The output voltage V_{dc} of SEPIC converter is given as

$$V_{dc} = \frac{D}{1-D} V_{in}$$

The converter input voltage is given as, $v_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$

Therefore the value of duty ratio D can be given as,

$$220 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.526$$

$$I_n = \frac{P_o}{V_n} = \frac{850}{198} = 4.3A$$

Equivalent Inductance (L_{eq}) for DCM,

$$L_{eq} = \frac{V_n \cdot D^2}{2 \cdot I_n \cdot f_s} = \frac{198 \cdot 0.526^2}{2 \cdot 4.3 \cdot 50000} = 0.127mH$$

The input inductor (L_1) operates in DCM and calculated as,

$$L_1 = \frac{V_n \cdot D}{2 \cdot I_n \cdot f_s} = \frac{198 \cdot 0.526}{2 \cdot 4.3 \cdot 50000} = 0.242mH$$

The selected value of input inductor is taken as **0.15mH**.

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Design of Output Inductor (CCM) is carried out as


$$L_{eq} = L_1 L_o / (L_1 + L_o)$$
$$L_o = L_{eq} L_1 / (L_1 - L_{eq}) = (127 * 150 * 10^{-12}) / ((150 - 127) * 10^{-6})$$
$$L_o = 0.83 \text{ mH}$$

The selected value of output inductor is taken **as 1.2 mH** to ensure its operation in CCM.

By **considering 20 % voltage ripples**, the **intermediate capacitor** is designed as

$$C_i = \frac{P_{med}}{k * f_s * (\sqrt{2} V_s + V_{dc})^2} = \frac{850}{0.2 * 50000 * (220\sqrt{2} + 220)^2} = 0.3 \mu\text{F}$$

Hence, the capacitor of **0.44 uF** is selected.



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Considering the condition of maximum ripple the **design of DC link capacitor** is made as,


$$C_d = \frac{I_{dc}}{2\omega \Delta V_{dc}} = \frac{850 / 220}{2 * 314 * .02 * 220} = 1.4 \text{ mF}$$

The maximum ripple voltage across C_{dc} is **considered as 2% of V_{dc}** . The value for DC link capacitor is selected **as 1.8 mF**.

The **design of this LC filter** can be given as,

$$C_{max} = \frac{I_m}{\omega L V_m} \tan(\theta) = \frac{(P_{rated} \sqrt{2} / V_s)}{\omega L V_m} \tan(\theta) = \frac{(850\sqrt{2} / 220)}{314 * 220\sqrt{2}} \tan(1^\circ) = 976.3 \text{ nF}$$

Where V_m and I_m are the supply voltage and current. Hence, the capacitor of **150 nF** is selected.



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While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. **Filter inductor design** can be given as,

$$L_s = 0.02 \left(\frac{1}{\omega_l} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_f = L_{req} + L_s \rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.02 \left(\frac{1}{\omega_l} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_{req} = \frac{1}{4\pi^2 \times 5000^2 \times 150 \times 10^{-8}} - 0.02 \left(\frac{1}{314} \right) \left(\frac{220^2}{850} \right) = 3.13mH$$

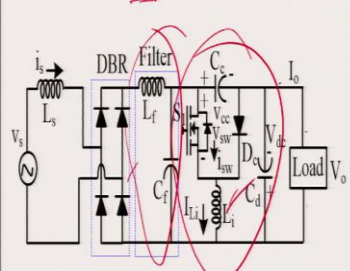
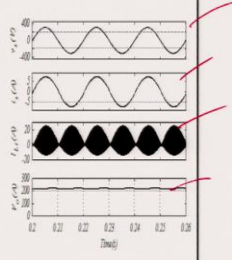

Hence, the inductor of **3.3mH** is selected. The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 29:17)

6. Design a single-phase power-factor corrected AC-DC non-isolated **CSC (Canonical Switching Converter) converter in DCM** (Discontinuous Current Mode of operation also known as voltage follower approach) operating at 20 kHz with following specifications: input: $V_s=220$ V rms, 50Hz, single-phase AC supply, DC output: $V_{dc}=220$ V, $P_{rated}=950$ W with output voltage-ripple less than 2%.

Coming to the 6th example. Design a single-phase power factor corrected AC-DC non-isolated CSC converter operating in discontinuous current mode at 20 kHz with the following specifications: supply voltage = 220 V/ 50 Hz, single-phase AC supply, and output is 220 V, power is 950 W with output voltage-ripple of 2 %.

(Refer Slide Time: 30:23)

Solution-

The output voltage V_{dc} of the CSC converter is given as,

$$V_{dc} = \frac{d_n}{1-d_n} V_m$$

The converter input voltage is given as, $v_m = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$


Therefore the nominal value of duty ratio d_n can be obtained from,

$$d_n = \frac{V_{dc}}{V_{dc} + V_m} = \frac{220}{220 + 198} = 0.526 \quad I_n = \frac{P_{rated}}{V_m} = \frac{950}{198} = 4.8A$$

Design of Inductor (L_c) for Critical Conduction,

$$L_c = \frac{V_m d_n}{2f_s I_n} = \frac{198 \times 0.526}{2 \times 4.8 \times 20000} = 0.54mH$$

The inductor is selected as **0.15 mH** to ensure **DCM** operation.



(Refer Slide Time: 31:49)

An **intermediate capacitor is designed** for permitted ripple voltage of across it and it is taken as **10%** of V_c [where is the voltage across intermediate capacitor, i.e., $(V_m + V_{dc}) = 198 + 220 = 418V$] and is given as,


$$C_1 = \frac{V_{dc} d_n}{f_s R_s \Delta V_{c1}} = \frac{220 \times 0.526}{20000 \times 51 \times 0.1 \times 418} = 2.72\mu F$$

Hence, the capacitor **of 3 μ F** is selected.

Considering the condition of **maximum ripple at minimum output voltage** the **design of DC link capacitor** is made as,

$$C_d = \frac{I_{dc}}{2\omega V_{dc}} = \frac{P_{rated}/V_{dc}}{2\omega \Delta V_{dc}} = \frac{950/220}{2 \times 314 \times 0.02 \times 220} = 1.56mF$$

The maximum ripple voltage across C_{dc} is considered as **2%** of V_{dc} . The value for DC link capacitor is selected as **1.8 mF**




(Refer Slide Time: 32:43)

The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics. Therefore **design of this LC filter** can be given as,

$$C_{\max} = \frac{I_m}{\omega_s V_m} \tan(\theta) = \frac{(P_{\text{rated}} \sqrt{2} / V_s)}{\omega_s V_m} \tan(\theta) = \frac{(950 \sqrt{2} / 220)}{314 \times 220 \sqrt{2}} \tan(1^\circ) = 1.1 \mu\text{F}$$

Where V_m and I_m are the supply voltage and current. The value for **filter capacitor** is selected **as 650 nF**.

While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. Higher order harmonics introduced in input side by high switching frequency of IGBT switches is eliminated by using LC filter. Therefore, an accurate filter design is essential for PFC converters, **filter inductor design** can be given as,




(Refer Slide Time: 33:44)

$$L_s = 0.03 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{\text{rated}}} \right)$$

$$L_f = L_{\text{req}} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{\text{req}} + 0.03 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{\text{rated}}} \right)$$

$$L_{\text{req}} = \frac{1}{4\pi^2 \times 2000^2 \times 650 \times 10^{-9}} - 0.03 \left(\frac{1}{314} \right) \left(\frac{220^2}{950} \right) = 4.88 \text{mH}$$

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 34:11)

7. Design a single-phase power-factor corrected AC-DC non-isolated Luo converter in DCM (input inductor DCM mode) operating at 20 kHz with following specifications: input: $V_s=220V$ rms, 50Hz, single-phase AC supply, DC output: $V_{dc}=300V$, $P_{rated}=250 W$ with output voltage-ripple less than 2%.

NPTEL

Coming to 7th example. Design a single-phase power factor corrected AC-DC non-isolated Luo converter operating in discontinuous conduction mode at 20 kHz with the following specifications: supply voltage = 220 V/50 Hz, single-phase AC supply, DC output voltage of 300 V, rated power of 250 W, and output voltage-ripple 2 %.

(Refer Slide Time: 34:49)

Solution-

The output voltage V_{dc} of Luo converter is given as

$$V_{dc} = \frac{D}{1-D} V_{in}$$

The converter input voltage is given as, $v_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$

Therefore the value of duty ratio D can be given as,

$$300 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.602$$

$$I_{in} = \frac{P_o}{V_{in}} = \frac{250}{198} = 1.262A$$

Design of Inductor (L_c) for Critical Conduction,

$$L_c = \frac{V_{in} D}{2f_s} = \frac{198 \times 0.602}{2 \times 1.262 \times 20000} = 2.36mH$$

The inductor is selected as the one tenth of the calculated value **i.e. 0.25 mH** to ensure **DCM** of operation

NPTEL

(Refer Slide Time: 35:57)

An **intermediate capacitor** is designed for permitted ripple voltage of across it and it is taken as 50% of V_c [where is the voltage across intermediate capacitor, i.e., $(V_{in} + V_d) = 198 + 300 = 498V$] and is given as,

$$C_1 = \frac{V_c \cdot D}{2R_L \cdot f_s \cdot \Delta V_c} = \frac{498 \cdot 0.602}{2 \cdot 360 \cdot 20000 \cdot 0.5 \cdot 498} = 83.61nF$$


Hence, the capacitor of **100nF** is selected.

Considering the condition of maximum ripple at minimum output voltage the **design of DC link capacitor** is made as,

$$C_d = \frac{I_{dc}}{2\omega \Delta V_{dc}} = \frac{P_{rated}/V_{dc}}{2\omega \Delta V_{dc}}$$

$$C_d = \frac{P_{rated}}{2\omega \Delta V_{dc}^2} = \frac{250}{2 \times 314 \times .02 \times 300^2} = 221.16\mu F$$

The maximum ripple voltage across C_{dc} is considered as 2% of V_{dc} . The value for DC link capacitor is selected as, **250 uF**.



(Refer Slide Time: 36:51)

Considering 20% current ripple. The expression for **output inductors (L_o)** is given as,


$$L_o = \frac{D \cdot I_{Lo}}{16 \cdot f_s^2 \cdot C_1 \cdot \Delta I_{Lo}} = \frac{0.602 \cdot (250 / 300)}{16 \cdot 20000^2 \cdot 100 \cdot 10^{-9} \cdot 0.2 \cdot (250 / 300)} = 4.7mH$$

Hence, the inductor of **5 mH** is selected.

The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics. Therefore **design of LC filter** can be given as,

$$C_{max} = \frac{I_m}{\omega_s V_m} \tan(\theta) = \frac{(P_{rated} \sqrt{2} / V_c)}{\omega_s V_m} \tan(\theta) = \frac{(250 \sqrt{2} / 220)}{314 \times 220 \sqrt{2}} \tan(1^\circ) = 287.13nF$$

Where V_m and I_m are the supply voltage and current. Hence, the **filter capacitor of 220nF** is selected.



(Refer Slide Time: 37:46)


While designing the inductor (L_f) for LC filter, the source inductor (L_s) is taken into consideration. Higher order harmonics introduced in input side by high switching frequency of IGBT switches is eliminated by using LC filter. Therefore, an accurate filter design is essential for PFC converters. **filter inductor design** can be given as,

$$L_s = 0.03 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.03 \left(\frac{1}{\omega_s} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$

$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 220 \times 10^{-9}} - 0.03 \left(\frac{1}{314} \right) \left(\frac{220^2}{250} \right) = 10\text{mH}$$

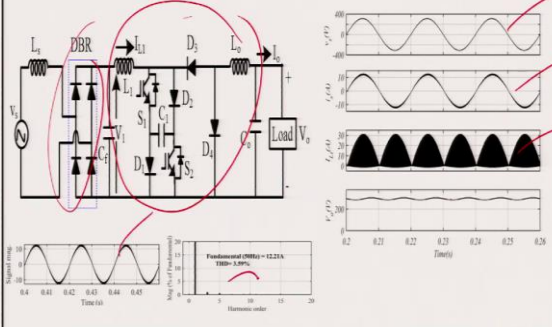
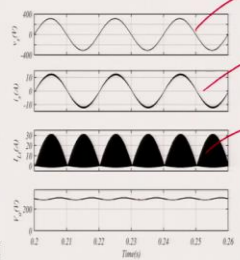
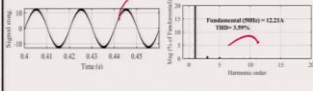

Hence, the inductor of **10mH** is selected.
The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 38:26)

8. Design a single-phase power-factor corrected AC-DC non-isolated **Sheppard-Taylor converter in (input and output inductor) DCM** operating at 20 kHz with following specifications: input: $V_s=220\text{V rms}$, 50Hz, single-phase AC supply, DC output: $V_o=300\text{V}$, $P_o=1900\text{W}$ with output voltage-ripple less than 5%.

Coming to 8th example. Design a single-phase power factor corrected AC-DC non-isolated Sheppard Taylor converter in DCM operating at 20 kHz with the following specifications: supply voltage = 220 V/50 Hz, single-phase AC supply, DC output voltage of 300 V, and power is 1900 W, with output ripple of less than 5%.

(Refer Slide Time: 39:31)

Solution- The output voltage V_o of Sheppard-Taylor converter is given as

$$V_o = \frac{D}{1-D} V_m$$

The converter input voltage is given as,

$$V_m = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198V$$

Therefore the value of duty ratio D can be given as,


$$300 = \frac{D}{1-D} \times 198 \Rightarrow D = 0.602$$

$$I_m = \frac{P_{rated}}{V_m} = \frac{1900}{198} = 9.6A$$

Design of Inductor (L_1) for discontinuous Current Conduction,

$$L_c = \frac{V_m * D}{2 * I_m * f_s} = \frac{198 * 0.602}{2 * 9.6 * 20000} = 0.31mH$$

Hence, the input inductor is selected as **0.1 mH** to operate in **DCM**.



(Refer Slide Time: 40:42)

An **intermediate capacitors** are designed for permitted ripple voltage of across it and it is taken as **45% of V_c** [where is the voltage across intermediate capacitor, i.e., $(V_m + V_d) = 198 + 300 = 498V$] and is given as,


$$C_f = \frac{V_o * D}{k * R_L * f_s * (V_o + V_m)} = \frac{300 * 0.602}{0.45 * 47.4 * 20000 * 498} = 0.85\mu F$$

Hence, the capacitor of **1 μ F** is selected.

Design of Output Inductor (L) (DCM Mode)

$$L_{oc} = \frac{V_o * (1-D)}{2 * I_o * f_s} = \frac{300 * (1-0.602)}{2 * 6.33 * 20000} = 0.472mH$$

Hence, the output inductor is selected of the order of **1/3rd of L_{oc}** as **0.16mH** to operate in **DCM**.



(Refer Slide Time: 41:46)

Considering the condition of maximum ripple at minimum output voltage the **design of DC link capacitor** is made as,


$$C_o = \frac{I_{dc}}{2\omega\Delta V_o} = \frac{1900/300}{2 * 314 * .05 * 300} = 0.67mF$$

The maximum ripple voltage across C_o is considered as 5% of V_o . The value for DC link capacitor is selected as **1 mF**.

The DBR output is fed to a low-pass filter tuned for one tenth of the switching frequency to suppress higher order harmonics. Therefore **design of this LC filter** can be given as,

$$C_{max} = \frac{I_m}{\omega_L V_m} \tan(\theta) = \left(\frac{P_{rated} \sqrt{2}/V_s}{\omega_L V_m} \right) \tan(\theta) = \frac{(1900\sqrt{2}/220)}{314 * 220\sqrt{2}} \tan(1^\circ) = 2.18\mu F$$

Hence, the capacitor of **780 nF** is selected.




(Refer Slide Time: 42:49)

Filter inductor equation is given by

$$L_s = 0.03 \left(\frac{1}{\omega_L} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$
$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.03 \left(\frac{1}{\omega_L} \right) \left(\frac{V_s^2}{P_{rated}} \right)$$
$$L_{req} = \frac{1}{4\pi^2 \times 2000^2 \times 780 \times 10^{-9}} - 0.03 \left(\frac{1}{314} \right) \left(\frac{220^2}{1900} \right) = 5.66mH$$

The cut-off frequency f_c for filter design is considered as 1/10 of the switching frequency i.e. $f_s/10$.

Hence, the inductor of **6mH** is selected.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 43:13)

9. Design a 300W PFC **BL-Zeta converter operating in CCM** to maintain a DC link voltage of 300V with percentage ripple of 1%. The permitted ripple in the input and output side inductor and intermediate capacitor is given as 20%. The PFC converter is to be operated at 220V/50Hz input with switching frequency as 40kHz. Calculate the value of input and output inductors, intermediate capacitor and the DC link capacitor.

Solution: The average input voltage appearing to input of converter,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{ V}$$

Now, the duty ratio is calculated as,

$$V_o = \left(\frac{D}{1-D}\right)V_{in}$$

$$\Rightarrow D = V_o / (V_o + V_{in}) = 300 / (300 + 198) = 0.6024$$

Coming to 9th example. Design a 300 W power factor corrected bridgeless zeta converter operating in continuous conduction mode to maintain the DC link voltage of 300 V with a percentage ripple of 1%. The permitted ripple in the input and output side inductors, and intermediate capacitor is 20%. The power factor correction converter is operated at 220V/50 Hz input, and the switching frequency is 40 kHz. Calculate the value of input and output inductors, intermediate capacitor and DC link capacitor.

(Refer Slide Time: 44:28)

The value of input current I_{in} $I_{in} = \frac{P_o}{V_{in}} = \frac{300}{198} = 1.515 \text{ A}$

Input Inductors Operating in CCM

For the 20% current ripples in input inductors, the design is given as,

$$L_{i1} = L_{i2} = \frac{V_{in} D}{f_s \Delta I_{L1}} = \frac{198 \times 0.6024}{40000 \times 0.2 \times 1.515} = 9.8411 \text{ mH}$$

Therefore, the L_{i1} and L_{i2} are selected as 10 mH to ensure CCM.

Output Inductors Operating in CCM

Considering 20% current ripples, the minimum value of output inductors is calculated as,

$$L_{o1} = L_{o2} = \frac{V_o (1-D)}{f_s \Delta I_{L_o}} = \frac{300(1-0.6024)}{40000 \times (0.2 \times 300 / 300)} = 14.9 \text{ mH}$$

Hence L_{o1} and L_{o2} are selected as 15 mH.

(Refer Slide Time: 45:44)

Design of Intermediate Capacitors

Considering **20% voltage ripples in intermediate capacitor**, the design is given as,


$$C_1 = C_2 = \frac{V_o D}{R_f \Delta V_{C1}} = \frac{300 \times 0.6024}{\frac{300^2}{300} + 40000 \times 0.2 \times (198 + 300)} = 151.2 \text{ nF}$$

Therefore, the C_1 and C_2 are selected **as 250nF** to ensure **CCM**.

DC Link Capacitor Design

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_o}{2\omega \Delta V_{dc}} = \frac{300 / 300}{2 \times 314 \times 0.01 \times 300} = 530.78 \mu\text{F}$$

DC link capacitor is selected as **660 uF**.



The solution of this problem is given in the abovemention slides.

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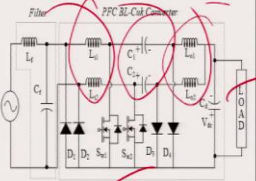

10. Design a 500W PFC **BL-Cuk converter operating in DCM (Output Inductor)** to maintain a DC link voltage of 300V with percentage ripple of **4%**. The permitted ripple in the input side inductor and intermediate capacitor is given as 20%. The PFC converter is to be operated at **220V/50Hz** input with switching frequency as **40kHz**. Calculate the value of input and output inductors, intermediate capacitor and the DC link capacitor.

Solution: The average input voltage appearing to input of converter,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{ V}$$

Now, the duty ratio is calculated as,

$$V_o = \left(\frac{D}{1-D}\right) V_{in}$$

$$\Rightarrow D = V_o / (V_o + V_{in}) = 300 / (300 + 198) = 0.6024$$



Coming to 10th example. Design a 500 W power factor corrected (PFC) bridgeless Cuk converter operating in discontinuous conduction mode (for output inductor only) to maintain the DC link voltage of 300 V with the percentage ripple of 4%. The percentage ripple in the input inductor and intermediate capacitor is 20%. The PFC converter is operating at 220 V/50 Hz, and switching frequency is 40 kHz. Calculate the value of input and output inductors, intermediate capacitor, and the output DC link capacitor.

(Refer Slide Time: 48:11)

The value of input current I_{in} $I_{in} = \frac{P_o}{V_{in}} = \frac{500}{198} = 2.525A$

Input Inductors Operating in CCM

For the **20% current ripples in input inductors**, the design is given as,

$$L_{i1} = L_{i2} = \frac{V_{in} D}{f_s \Delta I_L} = \frac{198 \times 0.6024}{40000 \times 0.2 \times 2.525} = 5.904mH$$


Therefore, the L_{i1} and L_{i2} are selected **as 6 mH** to ensure **CCM**.

Output Inductors Operating in DCM

The boundary value of output inductors is calculated as,

$$L_{o1} = L_{o2} \ll L_{oc} = \frac{V_o (1-D)}{f_s (2\%)^2} = \frac{300 \times (1-0.6024)}{40000 \times 2 \left(\frac{500}{300}\right)^2} = 894.6\mu H$$

Hence L_o is selected as $2/3^{rd}$ of L_{oc} i.e. **596.4 μ H**



(Refer Slide Time: 49:47)

Design of Intermediate Capacitors

Considering **20% voltage ripples in intermediate capacitor**, the design is given as,


$$C_1 = C_2 = \frac{V_o D}{R f_s \Delta V_{C1}} = \frac{300 \times 0.6024}{300^2 / 500 \times 40000 \times 0.2 \times (198 + 300)} = 252nF$$

Therefore, the C_1 and C_2 are selected **as 350nF** to ensure **CCM**.

DC Link Capacitor Design

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_o}{2\omega \Delta V_{dc}} = \frac{500 / 300}{2 \times 314 \times 0.04 \times 300} = 221.16\mu F$$

DC link capacitor is selected as **440 μ F**.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 50:57)

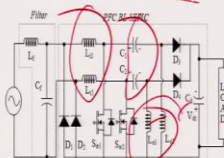
11. Design a 300W BL-SEPIC PFC converter operating in DCM (Output Inductor) to maintain a DC link voltage of 300V with percentage ripple of 4%. The permitted ripple in the input side inductor and intermediate capacitor is given as 20%. The PFC converter is to be operated at 220V/50Hz input with switching frequency as 40kHz. Calculate the value of input and output inductors, intermediate capacitor and the DC link capacitor.


Solution: The average input voltage appearing to input of converter,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{ V}$$

Now, the duty ratio is calculated as,

$$V_o = \left(\frac{D}{1-D}\right)V_{in}$$

$$\Rightarrow D = V_o / (V_o + V_{in}) = 300 / (300 + 198) = 0.6024$$




(Refer Slide Time: 52:31)

The value of input current I_{in} $I_{in} = \frac{P_o}{V_{in}} = \frac{300}{198} = 1.515 \text{ A}$

Input Inductors Operating in CCM

For the 20% current ripples in input inductors, the design is given as,

$$L_{i1} = L_{i2} = \frac{V_{in} D}{f_s \Delta i_{Li}} = \frac{198 \times 0.6024}{40000 \times 0.2 \times 1.515} = 9.8411 \text{ mH}$$


Therefore, the L_{i1} and L_{i2} are selected as **10 mH** to ensure **CCM**.

Output Inductors Operating in DCM

The boundary value of output inductors is calculated as,

$$L_{o1} = L_{o2} \ll L_{oc} = \frac{V_o (1-D)}{f_s (2i_o)} = \frac{300 \times (1-0.6024)}{40000 \times 2 \left(\frac{300}{300}\right)} = 1.49 \text{ mH}$$

Hence L_o is selected as $2/3^{\text{rd}}$ of L_{oc} i.e. **995 μH**



(Refer Slide Time: 54:04)

Design of Intermediate Capacitors

Considering **20% voltage ripples in intermediate capacitor**, the design is given as,


$$C_1 = C_2 = \frac{V_o D}{R_f \Delta V_{C1}} = \frac{300 \times 0.6024}{300^2 / 300 \times 40000 \times 0.2 \times (198 + 300)} = 151.2 \text{ nF}$$

Therefore, the C_1 and C_2 are selected **as 250nF** to ensure **CCM**.

DC Link Capacitor Design

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_o}{2\omega \Delta V_{dc}} = \frac{300 / 300}{2 \times 314 \times 0.04 \times 300} = 132.7 \mu\text{F}$$

DC link capacitor is selected **as 220 uF**.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 55:00)

12. Design a 200W PFC **BL-isolated Flyback converter** operating in **DCM** to maintain a DC link voltage of 50V with percentage ripple 4% in DC link capacitor. The PFC converter is to be operated at 220V/50Hz input with switching frequency as 45kHz and turns ratio as $N_1, N_2 = 2:1$. Calculate the value of transformer inductance and the DC link capacitor.

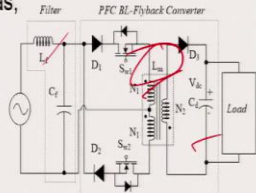

Solution: The average input voltage appearing to input of converter

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{ V}$$

Now, the duty ratio is calculated as,

$$V_o = \frac{D}{1-D} \left(\frac{N_2}{N_1} \right) V_{in} \Rightarrow$$

$$D = \frac{V_o}{\left(\frac{N_2}{N_1} V_{in} + V_o \right)}$$

$$D = 50 / (0.5 \times 198 + 50) \Rightarrow D = 0.3355$$



Coming to 12th example. Design a 200 W power factor corrected (PFC) bridgeless flyback converter operating in discontinuous mode to maintain the DC link voltage of 50 V with the percentage ripple of 4 % in DC link voltage. The PFC converter is operating with the input supply of 220 V/50 Hz, and switching frequency of 45 kHz, and the turns ratio is 2:1. Calculate the transformer inductance and DC link capacitor.

(Refer Slide Time: 56:12)

Design of Transformer Magnetizing Inductor (in DCM)

The boundary value of L_m is calculated as,

$$L_m \ll L_{mC} = \left[V_{in} \frac{N_2}{N_1} - V_o \right] \frac{DR}{2f_s V_o}$$


$$L_{mC} = \left[198 \left(\frac{1}{2} \right) - 50 \right] \frac{0.3355 \times \left(\frac{50^2}{200} \right)}{2 \times 45000 \times 50} = 45.66 \mu\text{H}$$

Hence value of inductor Operating in DCM is selected **as 30 μH** .

Design of DC Link Capacitor

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_o}{2\omega \Delta V_{dc}} = \frac{200 / 50}{2 \times 314 \times 0.04 \times 50} = 3.1847 \text{mF}$$

DC link capacitor is selected **as 3.3 mF**.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 57:08)

13. Design a 300W PFC BL-Isolated Cuk converter operating in DCM to maintain a DC link voltage of 100V with percentage ripple of 4%. The permitted ripple in the input side inductor and intermediate capacitor is given as 20%. The PFC converter is to be operated at 220V/50Hz input with switching frequency as 45kHz. The turns ratio is given as 2:1. Calculate the value of input and output inductors, intermediate capacitor and the DC link capacitor.

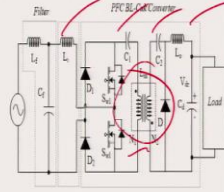

Solution: The average input voltage appearing to input of converter,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{V}$$

Now, the duty ratio is calculated as,

$$V_o = \frac{D}{1-D} \left(\frac{N_2}{N_1} \right) V_{in} \Rightarrow$$

$$D = V_o / \left(\frac{N_2}{N_1} V_{in} + V_o \right)$$

$$D = 100 / (0.5 \times 198 + 100) \Rightarrow D = 0.5025$$



(Refer Slide Time: 58:57)

The value of input current I_{in} $I_{in} = \frac{P_o}{V_{in}} = \frac{300}{198} = 1.515A$

Design of Input Inductor (in CCM)

For the 20% current ripples in input inductors, the design is given as,

$$L_i = \frac{V_{in} D}{f_s \Delta i_{L_i}} = \frac{198 \times 0.5025}{45000 \times 0.2 \times 1.515} = 7.297mH$$


Therefore, the L_i is selected as 7.5 mH to ensure **CCM**.

Design of output inductor in DCM

The boundary value of L_o i.e. L_{oc} , is calculated as,

$$L_o \ll L_{oc} = \frac{V_o (1-D)}{f_s (2i_o)} = \frac{100 \times (1-0.5025)}{45000 \times (2 \times 300 / 100)} = 184.26\mu H$$

Hence L_o is selected less than L_{oc} i.e. 150 μ H



(Refer Slide Time: 60:12)

Design of Intermediate capacitors (in CCM)

Considering 20% voltage ripples across both capacitors, the design expressions are given as,

$$C_1 = \frac{V_{in} \left(\frac{N_2}{N_1} \right)^2 D^2}{R f_s (1-D) \Delta V_{C1}} = \frac{198 \left(\frac{1}{2} \right)^2 (0.5025)^2}{(100^2 / 300) \times 45000 \times (1-0.5025) \times 0.2 \times (198)} = 422.95nF$$


$$C_2 = \frac{V_o D}{R f_s \Delta V_{C2}} = \frac{100 \times 0.5025}{(100^2 / 300) \times 45000 \times 0.2 \times 100} = 1.675\mu F$$

Thus, the C_1 and C_2 are selected as 500 nF and 1.8 μ F, respectively, to ensure **CCM**.

DC Link Capacitor Design

$$C_d = \frac{I_d}{2m \Delta V_{dc}} = \frac{P_o / V_o}{2m \Delta V_{dc}} = \frac{300 / 100}{2 \times 314 \times 0.04 \times 100} = 1.194mF$$

DC link capacitor is selected as 1.6 mF.



The solution of this problem is given in the abovemention slides.

(Refer Slide Time: 61:31)

14. Design a 500 W PFC BL-Isolated SEPIC converter operating in DCM to maintain a DC link voltage of 200 V with percentage ripple of 4%. The permitted ripple in the input side inductor and intermediate capacitor is given as 20%. The PFC converter is to be operated at 220V/50Hz input with switching frequency as 45kHz. The turns ratio (N_1/N_2) is given as 2:1. Calculate the value of input and output inductors, intermediate capacitor and the DC link capacitor.


Solution: The average input voltage appearing to input of converter,

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{\pi} = 198 \text{ V}$$

Now, the duty ratio is calculated as,

$$V_o = \frac{D}{1-D} \left(\frac{N_2}{N_1} \right) V_{in} \Rightarrow$$

$$D = \frac{V_o}{\left(\frac{N_2}{N_1} V_{in} + V_o \right)}$$

$$D = 200 / (0.5 \times 198 + 200) \Rightarrow D = 0.67$$


Now, coming to the 14th example. Design a 500 W power factor corrected (PFC) bridgeless isolated SEPIC converter operating in discontinuous mode to maintain the DC link voltage of 200 V with the percentage ripple of 4%. The permitted ripple in the input side inductor and intermediate capacitor is given 20% The PFC converter is operated with the supply of 220 V/50 Hz, and the switching frequency of 45 kHz. The turns ratio is selected typically as 2:1. Calculate the value of input and output inductor, and intermediate capacitor and the DC link capacitor.

(Refer Slide Time: 62:41)

The value of input current I_{in} $I_{in} = \frac{P_o}{V_{in}} = \frac{500}{198} = 2.53 \text{ A}$

Design of Input Inductor (in CCM)

For the 20% current ripples in input inductors, the design is given as,

$$L_i = \frac{V_{in} D}{f_s \Delta I_{L_i}} = \frac{198 \times 0.67}{45000 \times 0.2 \times 2.53} = 5.83 \text{ mH}$$


Therefore, the L_i is selected as 6 mH to ensure CCM.

Design of HFT Operating in DCM

The boundary value of L_m is calculated as,

$$L_m \ll L_{oc} = \frac{V_o (1-D)}{n f_s (2i_o)} = \frac{200 \times (1-0.67)}{0.5 \times 45000 \times (2 \times 500 / 200)} = 586.67 \mu\text{H}$$

Hence L_m is selected less than L_{mc} i.e. 150 μH



(Refer Slide Time: 63:41)

Design of Intermediate capacitor (in CCM)

Considering **20% voltage ripples across capacitor**, the design expressions are given as,


$$C_1 = \frac{\left(\frac{N_2}{N_1}\right) \frac{V_o D}{R_f S \Delta V_{C1}}}{\left(\frac{1}{2}\right) \frac{200 \times 0.67}{\left(\frac{200^2}{500}\right) \times 45000 \times 0.2 \times (198 + 200)}} = 467.62 \text{ nF}$$

Thus, the C_1 is selected **as 550 nF** to ensure **CCM**.

DC Link Capacitor Design

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_o}{2\omega \Delta V_{dc}} = \frac{500 / 200}{2 \times 314 \times 0.04 \times 200} = 497.61 \mu\text{F}$$

DC link capacitor is selected **as 660 uF**.




(Refer Slide Time: 64:35)

The solution of this problem is given in the abovemention slides.

Summary

- The Buck-Boost improved power quality converters demonstrate excellent performance characteristics over a wide range of supply voltage.
- The power circuit diagram and operational principle of several type of buck-boost derived IPQC's like Cuk, SEPIC, Zeta, Luo, and CSC, are presented.
- The bridgeless configuration of IPQC's offers lower conduction losses and fewer device count. Based on this, various bridgeless buck boost IPQC's are demonstrated.
- A number of practical examples of buck-boost derived IPQC's are given with a view of proper design exposure while considering improved power quality performance.




With this we would like to summarize. The buck-boost improve power quality converters demonstrate excellent performance characteristic over a wide range of supply voltage. The power circuit diagrams and operational principle of several type of buck-boost derive improve power quality converter like Cuk, SEPIC, Zeta, Luo, and canonical switching converter are presented. Further, various bridgeless buck-boost converters are also demonstrated. A number of practical examples of buck-boost derived improved

power quality converters are given with the view of proper design exposure while considering the improved power quality performance at the grid.

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And these are the references which we have taken into account.

Thank you.