Introduction to Embedded System Design

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Lecture No. 12

MSP430 Architecture

Hello, welcome back to a new session. In the last session we had started discussion about the MSP430 microcontroller family. We had discussed various features and one of the important features that we discussed was the various low power modes of operation. We had also discussed how very little current is required to power an MSP430 circuit.

I have a very interesting demonstration for you which consists of MSP430 circuit which is powered with the help of a lemon battery. As you can see here I have created a battery made out of lemons and two electrodes these electrodes are made out of copper and zinc and the power the voltage produced by this battery. There are 4 batteries in series each battery is producing 0.9 volts. So, roughly the voltage is 3. 6 volts, which is suitable for powering a MSP430 circuit.

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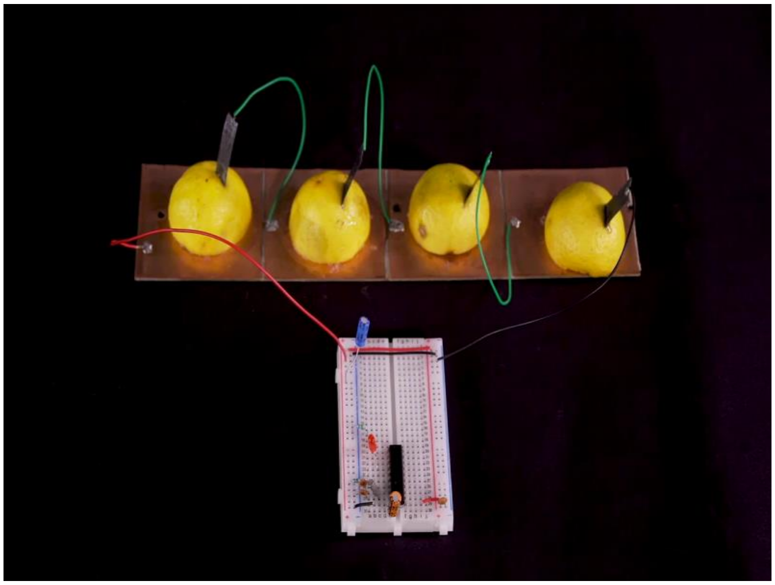

Here, you can see that the LED is blinking. I will draw the circuit for you of what we have done and you can try to create such a circuit at your at your end.

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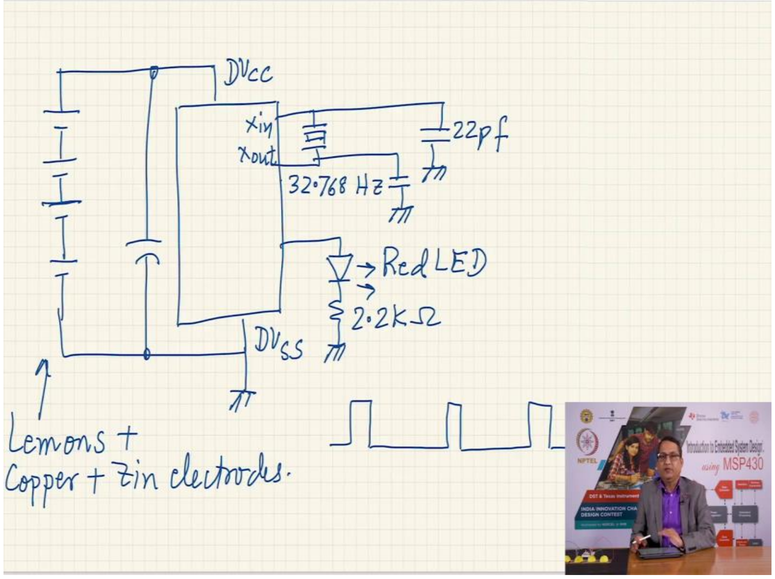

So, this circuit consists of a lemon battery which is made out of 4 lemons 4 lemon half’s. So, I am going to represent each lemon half by this 1, 2, 3 and 4. This is powering a MSP430 circuit. This is DVCC. This is DVSS and we also have connected a capacitor just so that it stabilizes and filters the voltage produced by but this is made out of lemons. Lemons plus copper electrode plus zinc.

On one of the output pins, we have connected a LED a red LED, as you saw. We also have on the X1, X in and X out pins. We have connected a crystal. This crystal is 32 kilohertz crystal 32.768 hertz crystal and there are two 22pf capacitors as required by the circuit for its operation. These are all 22pf ceramic capacitors. This is a 2.2 kilo ohm resistor and this is a red LED.

And what we have done is we have use this crystal operating at 32.768 kilo hertz to clock the internal circuit, but during the time the circuit is operating. The CPU is actually switched off. It has initially programmed the one of the timer's to produce a PWM signal where you notice that the LED was on for a short duration of time and it was off for a longer duration of time. We have achieved that with the help of a PWM signal something like this, on for short duration, off for a longer duration, again on for short duration, off for short duration and so on.

And this was applied to the LED. So, we the CPU has been shutoff. It is gone in a low-power mode and the only part of the circuit which is operating is this timer and we have all these modes under our control we can choose which part of the circuit would operate and this would be used by a programmer to optimize the available power. So, this is a very interesting demonstration that you just saw.

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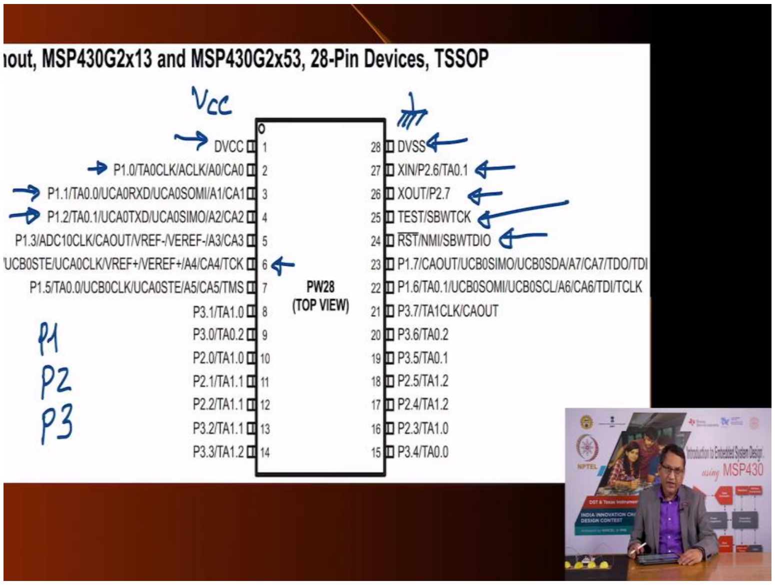

iout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP

Vcc
DVCC 1
P1.0/TA0CLK/ACLK/A0/CA0 2
P1.1/TA0.0/UCA0RXD/UCA0SOMI/A1/CA1 3
P1.2/TA0.1/UCA0TXD/UCA0SIMO/A2/CA2 4
P1.3/ADC10CLK/CAOUT/VREF-/VEREF-/A3/CA3 5
UCB0STE/UCA0CLK/VREF+/VEREF+/A4/CA4/TCK 6
P1.5/TA0.0/UCB0CLK/UCA0STE/A5/CA5/TMS 7
P3.1/TA1.0 8
P3.0/TA0.2 9
P2.0/TA1.0 10
P2.1/TA1.1 11
P2.2/TA1.1 12
P3.2/TA1.1 13
P3.3/TA1.2 14
28 DVSS
27 XIN/P2.6/TA0.1
26 XOUT/P2.7
25 TEST/SBWTCK
24 RST/NMI/SBWTDIO
23 P1.7/CAOUT/UCB0SIMO/UCB0SDA/A7/CA7/TDO/TDI
22 P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6/CA6/TDI/TCLK
21 P3.7/TA1CLK/CAOUT
20 P3.6/TA0.2
19 P3.5/TA0.1
18 P2.5/TA1.2
17 P2.4/TA1.2
16 P2.3/TA1.0
15 P3.4/TA0.0
PW28
(TOP VIEW)
P1
P2
P3
NPTEL
Introduction to Embedded System Design using MSP430

Let us resume our discussion which was to look at the pinout of MSP430 G-series microcontrollers. Because we are going to use G-series microcontrollers throughout our discussion. So, if you see here, it is a 28 pin G-series microcontroller, pin number 1 and 28 refer to the power supply pins here and here. This is VCC and this is ground this is ground.

Then most of the pins have (multi) multiple functions each pin offers multiple functions and it would depend on you the programmer the designer to write an appropriate program so as to select the functionality that you would require that you would want in your application. For example, if you look at pin number 2, it can act as port P bit number 0 or it can act as a clock for timer A.

It can also act as analogy input and it can also act as a comparator input because the MSP this particular MSP430 microcontroller has one comparator as we discussed in the previous lecture. If you notice here, let us go on the other side these two pins XIN and XOUT would be used to connect an external crystal should you choose to have that option.

If you want you could use an internal RC oscillator. A calibrated RC oscillator to power the microcontroller if you want in that way and if you wanted a more accurate source of timing, then you could connect the connect a crystal here. If you choose not to have a crystal, then these two pins, pin number 27 and 26 could also act as port pins as you see here p 2 0.6 and P 2 0.7.

This 28 pin IC has 2 ports as you see actually it has 3 ports P1, P2 and P3 and lot of functionality that is available in this microcontroller is distributed across the pins of these 3 ports. Let me show you another interesting pin. This is the reset pin and this one is the test pin the reset and test pin also serve as the Spy-Bi- Wire interface to the microcontroller.

Also if you look at pin number 3 and 4, these are one of the functions that is available on these two pins is dealing with the UART and you would use these UART pins, If you would want to program this microcontroller using the the bootloader method as I mentioned repeatedly the MSP430 Lunch Box kit uses the bootloader method of programming the this microcontroller. So, they would use pin number 2 and 3.

Apart from that across the chip you would see several functions. If you look at pin number 6 here. It is also an input for a voltage reference. If you want to have an external voltage reference for the on chip ADC. You could also use the internal reference voltages, but you can also overwrite that by writing an appropriate program. So that pin number 6, whatever external voltage that you apply would serve as the reference voltage for the on-chip ADC. Let us proceed to the next slides and discover more about this microcontroller family.

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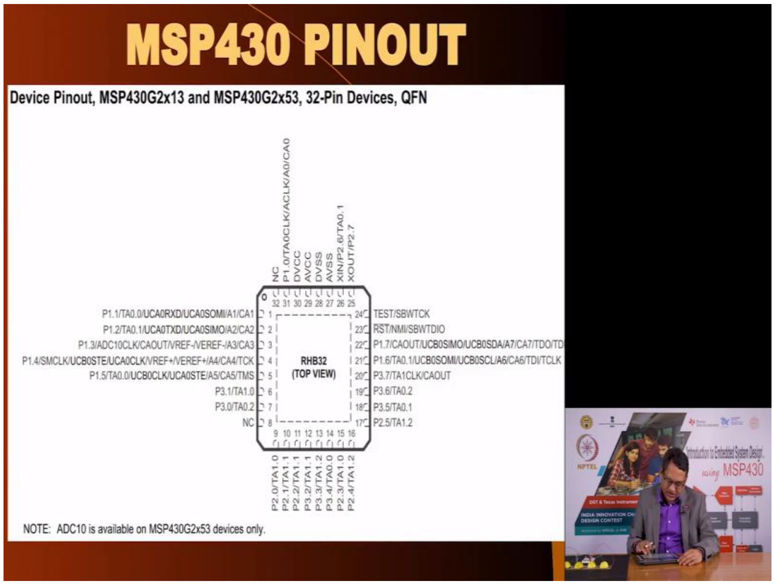

MSP430 PINOUT

Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN

NOTE: ADC10 is available on MSP430G2x53 devices only.

Here is a same microcontroller G-series microcontroller in a different footprint. This is a TQFP footprint because you see there are pins all around this IC.

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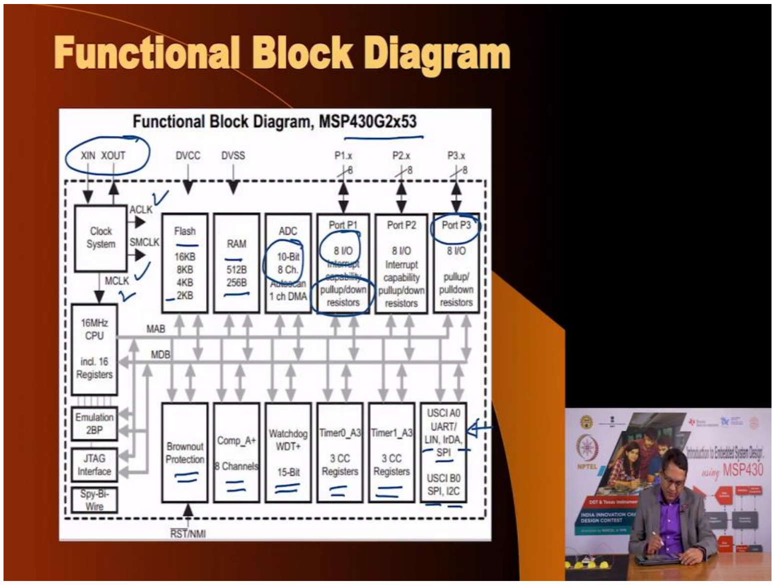

Functional Block Diagram

This is the functional block diagram of the MSP430G2x53 family. For example, the one of the numbers would be to MSP430G2553. MSP430G2553 is what we are using in our lunchbox. Now, let us start from top left. Here these are the two XIN, XOUT pins, which you as a designer could want to put a external crystal here, which would generate the system clock. It would also generate two more clocks called A clock and SM clock. A clock and SM clock are used by the peripherals which are available on the microcontroller. Whereas M clock is used to power the CPU. The CPU if you let us go down the CPU has 16 general purpose resistors will come to that.

Let us go across and now you see this microcontroller series offers flash memory for the program memory ranging from 2 kilobytes at the lowest value to 16 kilobytes. It has RAM and there are two options either you get 256 bytes of RAM or you get 512 bytes. It has a ADC here and you get 10 bit resolution ADC with 8 channels. There are 3 ports available. But depending upon the physical footprint you may get 1 port or 2 ports or all the 3 ports, each of the ports has 8 pins here.

And each of these pins have the capability to act as an interrupt input apart from that you can also choose to have pull up and pull down resistors. We have discussed the pull up and pull down resistors in our discussion on physical interfacing and we will also discuss it in future all the 3 ports P1 port 1, port 2, port 3 each having up to 8 pins has uniform capability that it has interrupt in capability as well as pull up pull down, port 3 unfortunately does not have interrupt inputs.

If we go down here, here we have the USCI that is universal serial communication interface. It has two parts to this USCI A0 and USCI B0. The USCI is A0 offers 4 modes of operation either it can act as a UART universal asynchronous receiver transmitter or it can act as LIN Local Interface Network or it can act as for a infrared communication or it can act as one of the SPI ports.

The second channel of serial communication offers two options, either you can operate it as SPI interface or you can operate it as I square C bus. So, if you look at the serial communication options, you can use the USCI to give you two channels of SPI or you can have one SPI and one I square C or you can have one UART and one SPI you can have one UART and one I square C and so on.

All the combinations that you can make with these two channels of communication, to the left of this we have timer which has 3 compare resistors. We have another timer which also has 3 compare resistors both these timers are 16 bit timers. Next to that is a Watchdog timer and as you notice here this watchdog is a 15 bit watchdog, which means the maximum count that it can it will count before it overflows and this would be used to reset the system is to 2 raise to power 15, which is 32768.

Next to that is a comparator with 8 inputs and you could select which input you would want to connect to the inputs of the comparator. And we also have Brownout protection which means this part of the circuit will provide brownout reset source. One of the reset resources that we discussed in the past. This is one of them. Towards the left most under the CPU you have JTAG interface.

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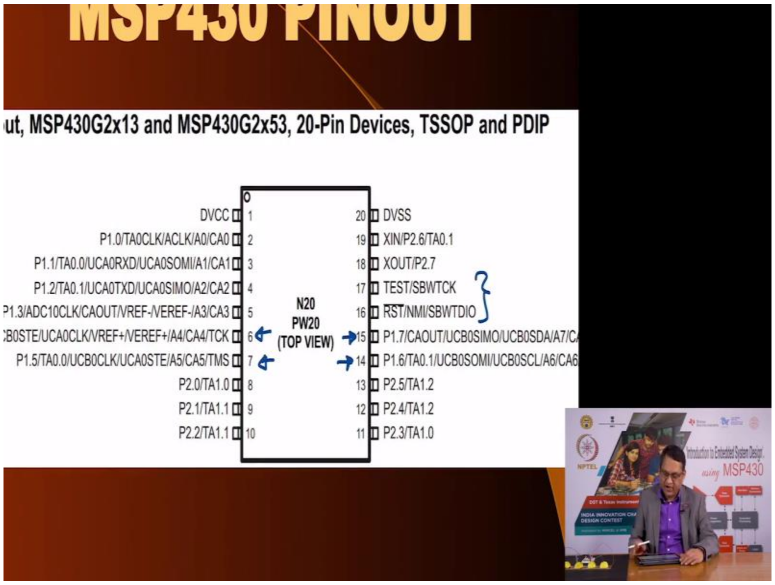

MSP430 PINOUT

ut, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP

DVCC 1
P1.0/TA0CLK/ACLK/A0/CA0 2
P1.1/TA0.0/UCA0RXD/UCA0SOMI/A1/CA1 3
P1.2/TA0.1/UCA0TXD/UCA0SIMO/A2/CA2 4
P1.3/ADC10CLK/CAOUT/VREF-/VEREF-/A3/CA3 5
B0STE/UCA0CLK/VREF+/VEREF+/A4/CA4/TCK 6
P1.5/TA0.0/UCB0CLK/UCA0STE/A5/CA5/TMS 7
P2.0/TA1.0 8
P2.1/TA1.1 9
P2.2/TA1.1 10
N20
PW20
(TOP VIEW)
20 DVSS
19 XIN/P2.6/TA0.1
18 XOUT/P2.7
17 TEST/SBWTCK
16 RST/NMI/SBWTDIO
15 P1.7/CAOUT/UCB0SIMO/UCB0SDA/A7/C
14 P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6/CA6
13 P2.5/TA1.2
12 P2.4/TA1.2
11 P2.3/TA1.0

And we saw in the pin diagram here. Let me show you hear that this pin diagram has entire 4 pins of the JTAG that is TCK here TMS and then you have TDI and TCLK. If you want to have a shorter or a smaller interface to the same JTAG, then you would use this Spy-Bi-Wire both of them give access to the JTAG controller one in a explicit form one through the Spy-Bi-Wire.

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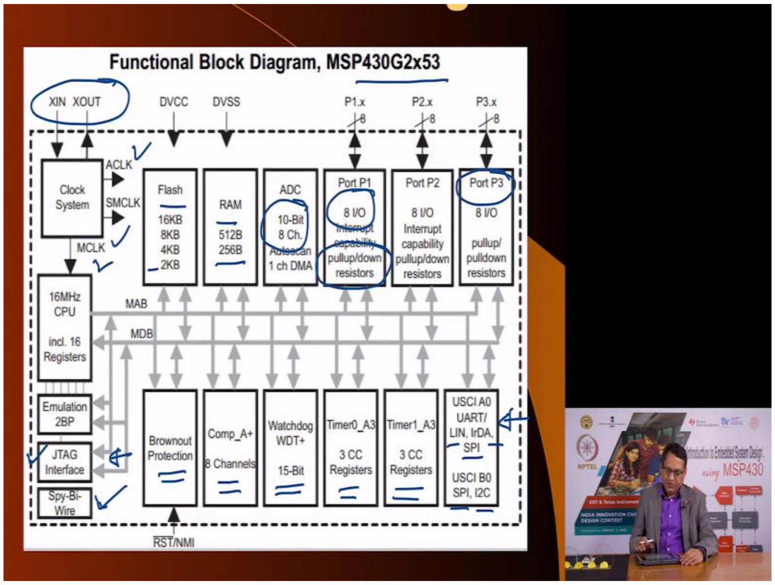

Functional Block Diagram, MSP430G2x53

So, that is what we have on the chip the JTAG interface and you could have access to the JTAG interface through the Spy-Bi-Wire communication also. So this completes the block diagram description of the MSP430 G-series of microcontrollers. Let us go further.

Now it is very important to be able to read a data sheet because data sheet is provides you wealth of information more than what a course can teach you about the course can only sensitize you that a data sheet is a wealth of information but you as the end user you as the engineer must know where to look for relevant information inside a data sheet. So, I am going to open up a data sheet and go through it so that you are able to understand.

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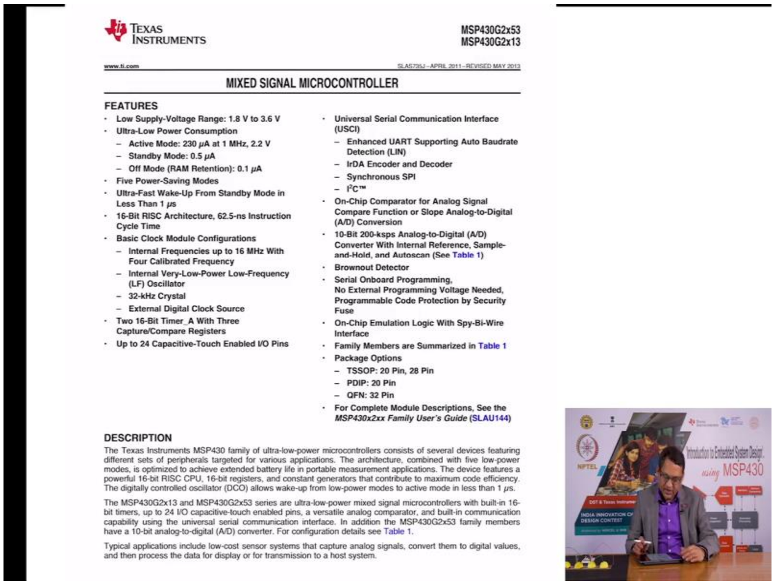

TEXAS INSTRUMENTS

MSP430G2x53
MSP430G2x13

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MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 230 μA at 1 MHz, 2.2 V
  - Standby Mode: 0.5 μA
  - Off Mode (RAM Retention): 0.1 μA
- Five Power-Saving Modes
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequency
  - Internal Very-Low-Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - External Digital Clock Source
- Two 16-Bit Timer_A With Three Capture/Compare Registers
- Up to 24 Capacitive-Touch Enabled I/O Pins
- Universal Serial Communication Interface (USCI)
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- Family Members are Summarized in Table 1
- Package Options
  - TSSOP: 20 Pin, 28 Pin
  - PDIP: 20 Pin
  - QFN: 32 Pin
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. In addition the MSP430G2x53 family members have a 10-bit analog-to-digital (A/D) converter. For configuration details see Table 1.

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

The first page of the of any data sheet whether it is about the microcontroller or it is about discrete component we will list out the silent features. So, if you see here it talks about the features. Here where it says, the low power voltage range is 1 point 8 to 3 point 6 and so on and that it has various modes of operation active mode, sleep mode, standby modes. It has serial communication protocols.

It has on chip comparator all that we have discussed. But usually it will be available in the first part of the first page of a data sheet. Then it might describe the details about it about the microcontroller.

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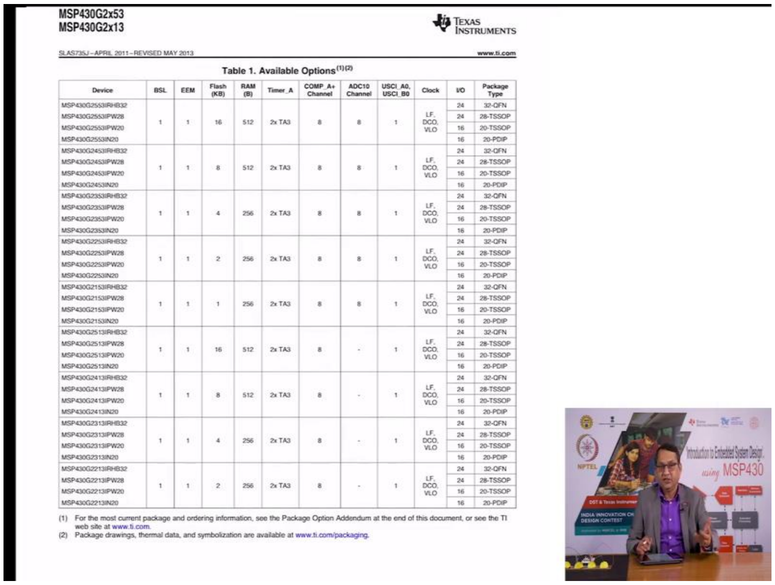

MSP430G2x53
MSP430G2x13

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Table 1. Available Options[(1)(2)]

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	COMP_A+ Channel	ADC10 Channel	USCI_A0, USCI_B0	Clock	I/O	Package Type
MSP430G2553IRHB32	1	1	16	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2553IPW28										24	28-TSSOP
MSP430G2553IPW20										16	20-TSSOP
MSP430G2553IN20										16	20-PDIP
MSP430G2453IRHB32	1	1	8	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2453IPW28										24	28-TSSOP
MSP430G2453IPW20										16	20-TSSOP
MSP430G2453IN20										16	20-PDIP
MSP430G2353IRHB32	1	1	4	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2353IPW28										24	28-TSSOP
MSP430G2353IPW20										16	20-TSSOP
MSP430G2353IN20										16	20-PDIP
MSP430G2253IRHB32	1	1	2	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2253IPW28										24	28-TSSOP
MSP430G2253IPW20										16	20-TSSOP
MSP430G2253IN20										16	20-PDIP
MSP430G2153IRHB32	1	1	1	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2153IPW28										24	28-TSSOP
MSP430G2153IPW20										16	20-TSSOP
MSP430G2153IN20										16	20-PDIP
MSP430G2513IRHB32	1	1	16	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2513IPW28										24	28-TSSOP
MSP430G2513IPW20										16	20-TSSOP
MSP430G2513IN20										16	20-PDIP
MSP430G2413IRHB32	1	1	8	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2413IPW28										24	28-TSSOP
MSP430G2413IPW20										16	20-TSSOP
MSP430G2413IN20										16	20-PDIP
MSP430G2313IRHB32	1	1	4	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2313IPW28										24	28-TSSOP
MSP430G2313IPW20										16	20-TSSOP
MSP430G2313IN20										16	20-PDIP
MSP430G2213IRHB32	1	1	2	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2213IPW28										24	28-TSSOP
MSP430G2213IPW20										16	20-TSSOP
MSP430G2213IN20										16	20-PDIP

[1] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
[2] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Then in this case it has available options in terms of the peripheral feature that this microcontroller has.

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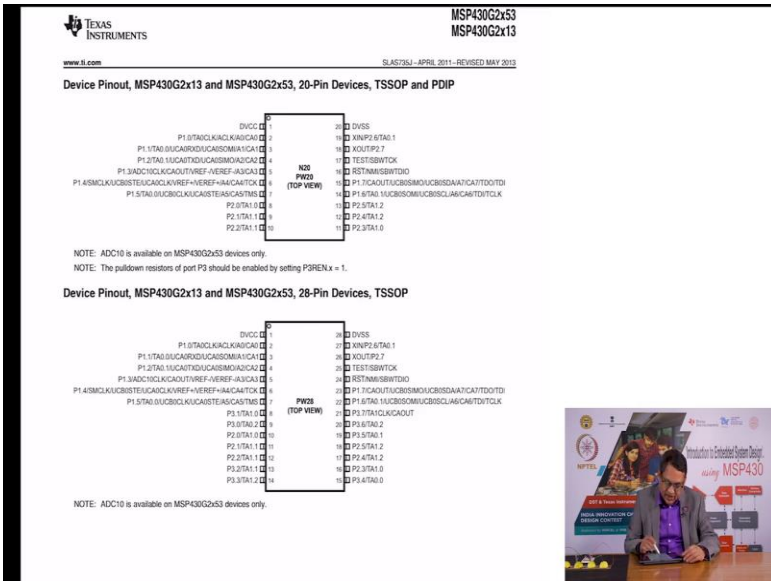

MSP430G2x53
MSP430G2x13

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Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP

DVCC 1
P1.0/TA0CLK/ACLK/A0/CA0 2
P1.1/TA0.0/UCA0RXD/UCA0SOMI/A1/CA1 3
P1.2/TA0.1/UCA0TXD/UCA0SIMO/A2/CA2 4
P1.3/ADC10CLK/CAOUT/VREF-/VEREF-/A3/CA3 5
P1.4/SMCLK/UCB0STE/UCA0CLK/VREF+/VEREF+/A4/CA4/TCK 6
P1.5/TA0.0/UCB0CLK/UCA0STE/A5/CA5/TMS 7
P2.0/TA1.0 8
P2.1/TA1.1 9
P2.2/TA1.1 10
N20
PW20
(TOP VIEW)
20 DVSS
19 XIN/P2.6/TA0.1
18 XOUT/P2.7
17 TEST/SBWTCK
16 RST/NMI/SBWTDIO
15 P1.7/CAOUT/UCB0SIMO/UCB0SDA/A7/CA7/TDO/TDI
14 P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6/CA6/TDI/TCLK
13 P2.5/TA1.2
12 P2.4/TA1.2
11 P2.3/TA1.0

NOTE: ADC10 is available on MSP430G2x53 devices only.

NOTE: The pulldown resistors of port P3 should be enabled by setting P3REN.x = 1.

Device Pinout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP

DVCC 1
P1.0/TA0CLK/ACLK/A0/CA0 2
P1.1/TA0.0/UCA0RXD/UCA0SOMI/A1/CA1 3
P1.2/TA0.1/UCA0TXD/UCA0SIMO/A2/CA2 4
P1.3/ADC10CLK/CAOUT/VREF-/VEREF-/A3/CA3 5
P1.4/SMCLK/UCB0STE/UCA0CLK/VREF+/VEREF+/A4/CA4/TCK 6
P1.5/TA0.0/UCB0CLK/UCA0STE/A5/CA5/TMS 7
P3.1/TA1.0 8
P3.0/TA0.2 9
P2.0/TA1.0 10
P2.1/TA1.1 11
P2.2/TA1.1 12
P3.2/TA1.1 13
P3.3/TA1.2 14
PW28
(TOP VIEW)
28 DVSS
27 XIN/P2.6/TA0.1
26 XOUT/P2.7
25 TEST/SBWTCK
24 RST/NMI/SBWTDIO
23 P1.7/CAOUT/UCB0SIMO/UCB0SDA/A7/CA7/TDO/TDI
22 P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6/CA6/TDI/TCLK
21 P3.7/TA1CLK/CAOUT
20 P3.6/TA0.2
19 P3.5/TA0.1
18 P2.5/TA1.2
17 P2.4/TA1.2
16 P2.3/TA1.0
15 P3.4/TA0.0
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NOTE: ADC10 is available on MSP430G2x53 devices only.

Then if this micro if this data sheet reference to a certain family, it will talk about the pin outs that are available. In this case, it says that it is available in TSSOP as well as PDIP on this page

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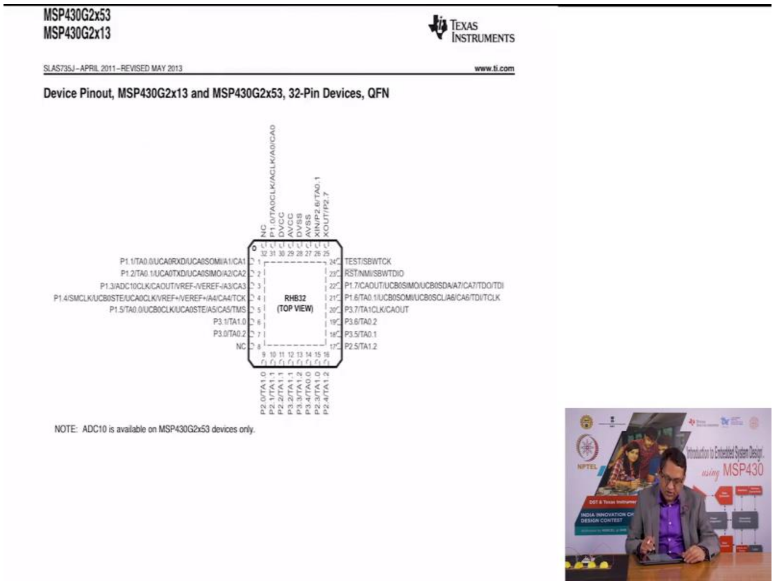

MSP430G2x53
MSP430G2x13

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Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN

NC
P1.0/TA0CLK/ACLK/A0/CA0
DVCC
AVCC
DVSS
AVSS
XIN/P2.6/TA0.1
XOUT/P2.7
32 31 30 29 28 27 26 25
P1.1/TA0.0/UCA0RXD/UCA0SOMI/A1/CA1 1
P1.2/TA0.1/UCA0TXD/UCA0SIMO/A2/CA2 2
P1.3/ADC10CLK/CAOUT/VREF-/VEREF-/A3/CA3 3
P1.4/SMCLK/UCB0STE/UCA0CLK/VREF+/VEREF+/A4/CA4/TCK 4
P1.5/TA0.0/UCB0CLK/UCA0STE/A5/CA5/TMS 5
P3.1/TA1.0 6
P3.0/TA0.2 7
NC 8
RHB32
(TOP VIEW)
24 TEST/SBWTCK
23 RST/NMI/SBWTDIO
22 P1.7/CAOUT/UCB0SIMO/UCB0SDA/A7/CA7/TDO/TDI
21 P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6/CA6/TDI/TCLK
20 P3.7/TA1CLK/CAOUT
19 P3.6/TA0.2
18 P3.5/TA0.1
17 P2.5/TA1.2
9 10 11 12 13 14 15 16
P2.0/TA1.0
P2.1/TA1.1
P2.2/TA1.1
P3.2/TA1.1
P3.3/TA1.2
P3.4/TA0.0
P2.3/TA1.0
P2.4/TA1.2
NPTEL
Introduction to Embedded System Design using MSP430

NOTE: ADC10 is available on MSP430G2x53 devices only.

And the next page shows QFN which is quad package, which has pins on all sides the same pins distributed on for all sides.

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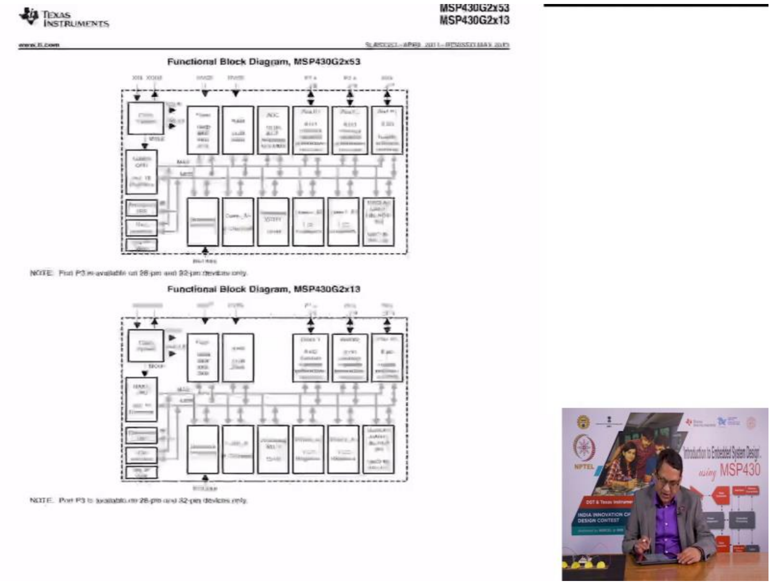

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Functional Block Diagram, MSP430G2x53

NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Functional Block Diagram, MSP430G2x13

NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Here is the functional block diagram the one we just discussed few moments ago.

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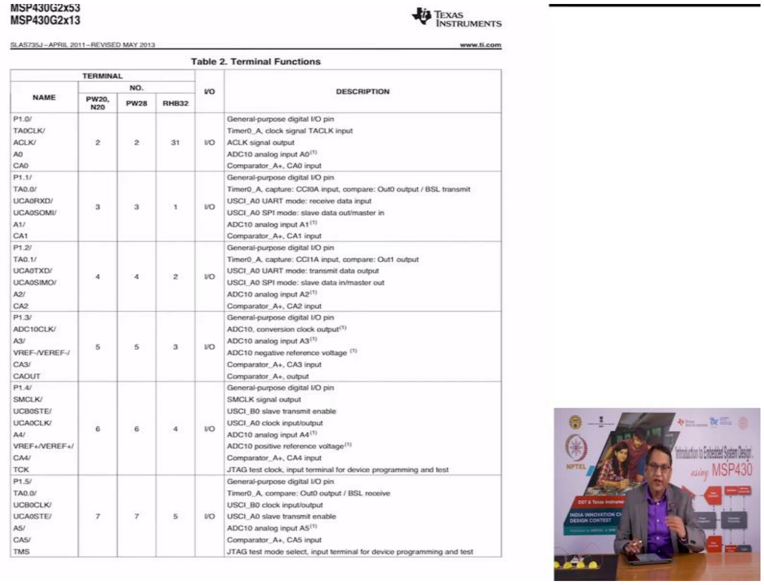

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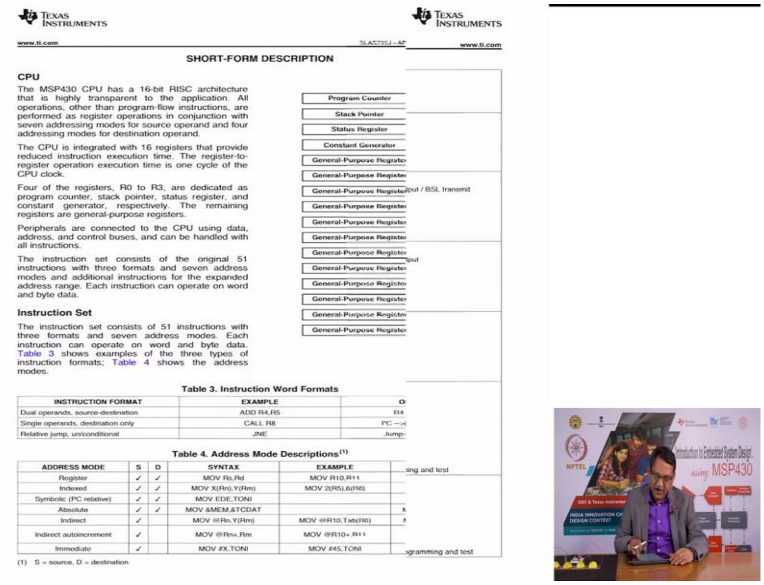
Table 2. Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.0/ TA0CLK/ ACLK/ A0 CA0	2	2	31	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal output ADC10 analog input A0[1] Comparator_A+, CA0 input
P1.1/ TA0.0/ UCA0RXD/ UCA0SOMI/ A1/ CA1	3	3	1	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output / BSL transmit USCI_A0 UART mode: receive data input USCI_A0 SPI mode: slave data out/master in ADC10 analog input A1[1] Comparator_A+, CA1 input
P1.2/ TA0.1/ UCA0TXD/ UCA0SIMO/ A2/ CA2	4	4	2	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output USCI_A0 UART mode: transmit data output USCI_A0 SPI mode: slave data in/master out ADC10 analog input A2[1] Comparator_A+, CA2 input
P1.3/ ADC10CLK/ A3/ VREF-/VEREF-/ CA3/ CAOUT	5	5	3	I/O	General-purpose digital I/O pin ADC10, conversion clock output[1] ADC10 analog input A3[1] ADC10 negative reference voltage [1] Comparator_A+, CA3 input Comparator_A+, output
P1.4/ SMCLK/ UCB0STE/ UCA0CLK/ A4/ VREF+/VEREF+/ CA4/ TCK	6	6	4	I/O	General-purpose digital I/O pin SMCLK signal output USCI_B0 slave transmit enable USCI_A0 clock input/output ADC10 analog input A4[1] ADC10 positive reference voltage[1] Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ UCB0CLK/ UCA0STE/ A5/ CA5/ TMS	7	7	5	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output / BSL receive USCI_B0 clock input/output USCI_A0 slave transmit enable ADC10 analog input A5[1] Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test

It has what are the various terminals the pins of the microcontroller. What are the functions of each of these pins? What alternate functions those pins serve, this is a list table of that.

(Refer Slide Time: 16:10)



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SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Program Counter
Stack Pointer
Status Register
Constant Generator
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register
General-Purpose Register

put / BSL transmit

put

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	O
Dual operands, source-destination	ADD R4,R5	R4
Single operands, destination only	CALL R8	PC -->
Relative jump, un/conditional	JNE	Jump-

Table 4. Address Mode Descriptions[1]

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		
Absolute	✓	✓	MOV &MEM,&TCDAT		M
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	
Immediate	✓		MOV #X,TONI	MOV #45,TONI	

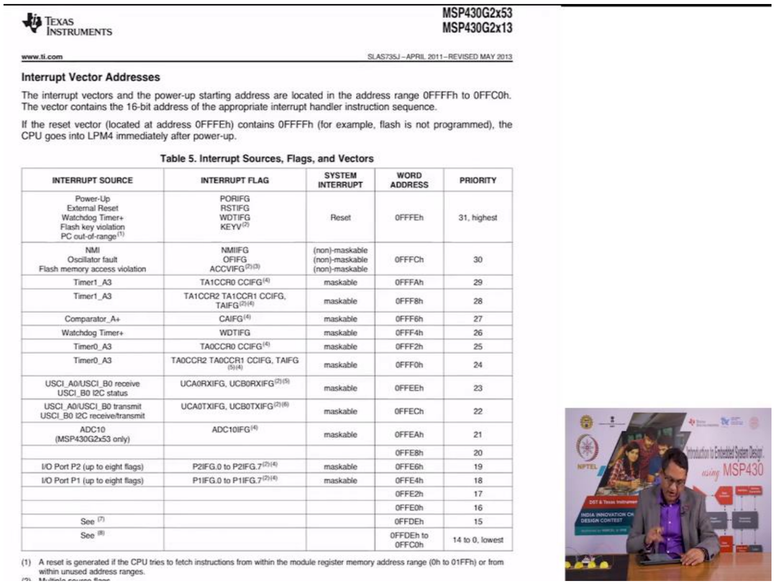
ing and test

gramming and test

[1] S = source, D = destination

Continued with that, here is a short form description of the CPU the various general purpose register we are going to come to that shortly.

(Refer Slide Time: 16:21)



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Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

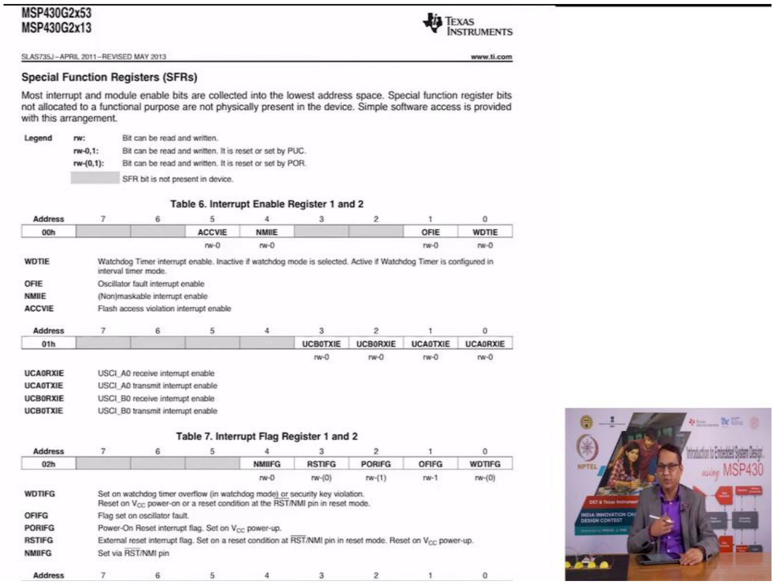
Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range[1]	PORIFG RSTIFG WDTIFG KEYV[2]	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG[2][3]	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG[4]	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG[2][4]	maskable	0FFF8h	28
Comparator_A+	CAIFG[4]	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG[4]	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG[5][4]	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG[2][5]	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG[2][6]	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG[4]	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7[2][4]	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7[2][4]	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See [7]			0FFDEh	15
See [8]			0FFDEh to 0FFC0h	14 to 0, lowest

[1] A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
[2] Multiple source flags

The instruction set and eventually it is going to talk about for example here are the interrupt vector addresses these locations will be used to put pointers to the interrupt subroutines if you want to use those interrupts in your in your system.

(Refer Slide Time: 16:35)



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Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	▨	SFR bit is not present in device.

Table 6. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h	▨	▨	ACCVIE	NMIIE	▨	▨	OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE Oscillator fault interrupt enable
NMIIE (Non)maskable interrupt enable
ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	▨	▨	▨	▨	UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive interrupt enable
UCA0TXIE USCI_A0 transmit interrupt enable
UCB0RXIE USCI_B0 receive interrupt enable
UCB0TXIE USCI_B0 transmit interrupt enable

Table 7. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	▨	▨	▨	NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.
OFIFG Flag set on oscillator fault.
PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0

This is a description of all the special function registers. And so on.

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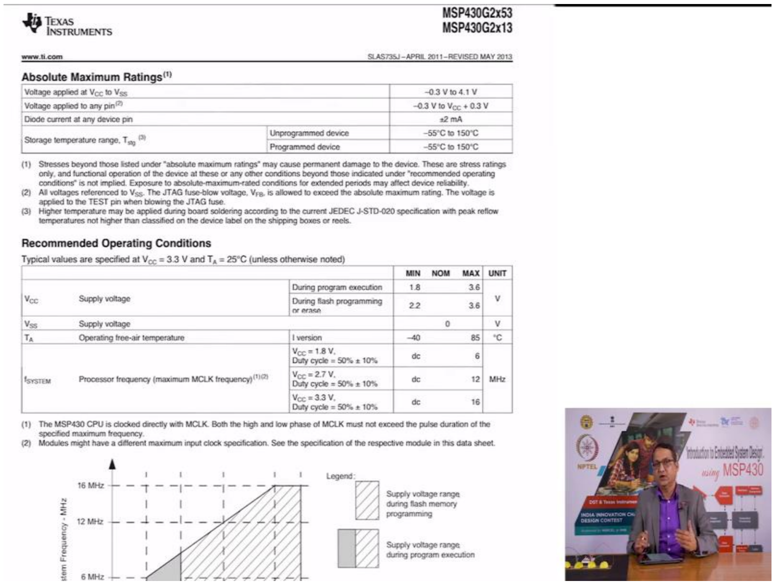

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Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg} (3)	Unprogrammed device	–55°C to 150°C
	Programmed device	–55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash programming or erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} = 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.

(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.

16 MHz
12 MHz
6 MHz
stem Frequency - MHz
Legend:
Supply voltage range during flash memory programming
Supply voltage range during program execution

And here are the electrical characteristics you would find these electrical characteristics in almost every data sheet, whether it is for a microcontroller, whether it is for a logic IC, whether it is for a for a semiconductor device any semiconductor device and it talks out absolute maximum ratings, which means what are the maximum voltage you can apply to this IC in this case without destroying it. It talks of maximum voltage it talks of maximum temperature that it can survive.

Then there are recommended operating condition meaning maximum ratings you are not going to normally encounter in commonly, but recommended operating conditions are what you must adhere to. So, it talks of the supply voltage the operating temperature and the frequency of operation in this case of this microcontroller

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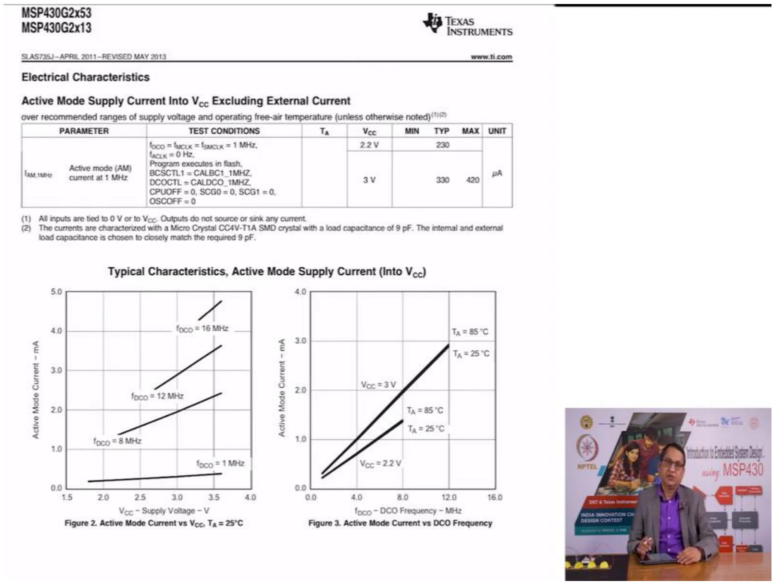

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Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current at 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 0 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		230		μA
				3 V		330	420	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics, Active Mode Supply Current (Into V_{CC})

Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

Figure 3. Active Mode Current vs DCO Frequency

Then it talks of the various current consumptions, the various in active mode and low power modes, you can get you can use the information in this data sheet to verify when you are designing a system and you find that it is not working the way you would expect. This is the place to refer to to find out how much current should it consume versus how much current it is actually consuming.

So, I recommend very strongly that you practice reading a data sheet and to (())(18:18) the information given in this data sheet at the very fag end you will find this IC or the series of IC’s in what bulk packaging form there available as I mentioned in the last lecture whether they are available in a tube form or whether they are packaged in a role of which can be used in production all that information is available in this data sheet.

Let us get back to our discussion on the features of this MSP430 G-series of microcontrollers. So, the architecture of MSP430 CPU, is that as I mentioned it is a Risc architecture. You see here. It is a RISC architecture and one of the silent features of RISC architecture as a name suggest reduced instruction set computer is that compared to a corresponding CISC architecture the number of instructions would be limited. And in this case, there are only 27 basic type of instructions.

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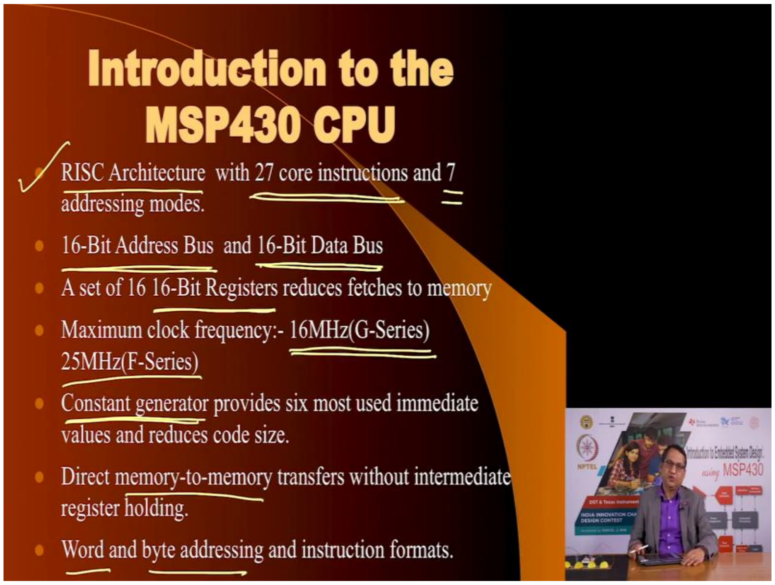

Introduction to the MSP430 CPU

- RISC Architecture with 27 core instructions and 7 addressing modes.
- 16-Bit Address Bus and 16-Bit Data Bus
- A set of 16 16-Bit Registers reduces fetches to memory
- Maximum clock frequency:- 16MHz(G-Series) 25MHz(F-Series)
- Constant generator provides six most used immediate values and reduces code size.
- Direct memory-to-memory transfers without intermediate register holding.
- Word and byte addressing and instruction formats.

It has 7 addressing which means each or many of these instructions would have variations how it is going to fetch the operant. And for that it uses 7 addressing modes. The address bit usually 16-bits for G-series certainly it is 16-bits, but for other variants, it could be 20 bits. The data bus is 16-bits because it is a 16-bit microcontroller.

Apart from the architecture and the bus interface unit, it has 16 16-bit registers. There are 16 registers each of the registers can hold a 16-bit value and we will see what all these registers perform. The maximum clock frequency for a G-series is 16 megahertz and for the F-series it is 25 megahertz. The registers have a interesting feature that they can be used to get constant values. And so there is a constant generator. I am going to come back to the constant generator shortly.

It has direct memory to memory transfer. So, you want to move a chunk of memory or you want to copy some part of memory into another section of the memory, you can do that without bringing a register in the picture and the instructions have word and byte addressing which means there are instructions which can fetch a word which means two bytes and there are instructions which can fetch or deal with a single byte of instruction.

The memory architecture is Von-Neumann here, which means there is a unified memory map. And in the same memory map you would have program memory you would have data memory.

And in this case it also has access to the special function registers. These registers control the input output peripherals of MSP430 microcontroller.

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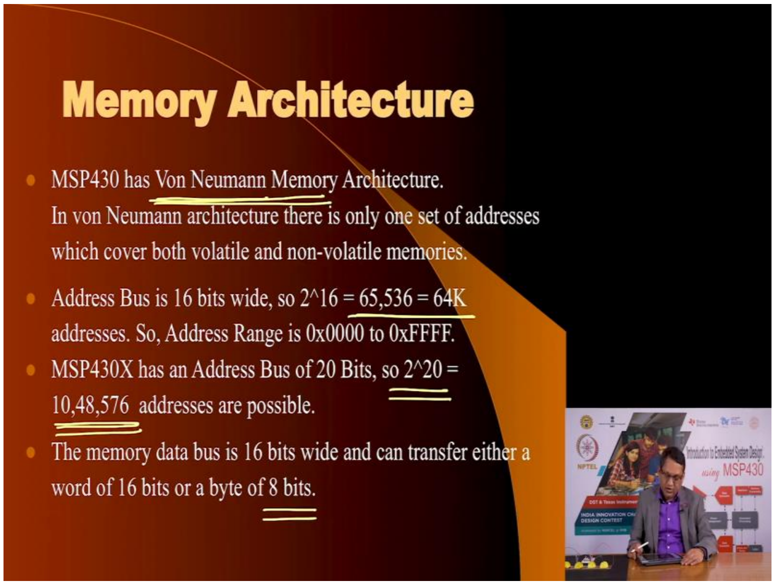

Memory Architecture

- MSP430 has Von Neumann Memory Architecture.
  In von Neumann architecture there is only one set of addresses which cover both volatile and non-volatile memories.
- Address Bus is 16 bits wide, so 2^16 = 65,536 = 64K addresses. So, Address Range is 0x0000 to 0xFFFF.
- MSP430X has an Address Bus of 20 Bits, so 2^20 = 10,48,576 addresses are possible.
- The memory data bus is 16 bits wide and can transfer either a word of 16 bits or a byte of 8 bits.

The address bus allows you up to 64K memory locations as we seen. But in some cases it also has 20 address lines and you can have 1048 1 million memory locations like this. The data bus is 16 bits wide so you can transfer either 16 bits in a in a single cycle, but you can choose to have only a byte of data transfer as well. The way the words are stored, a word here means one word is equal to 2 bytes, which is equal to 16 bits. So, inherently the microcontroller can store 16 bits, but there is a restriction as to which memory addresses can it store these words.

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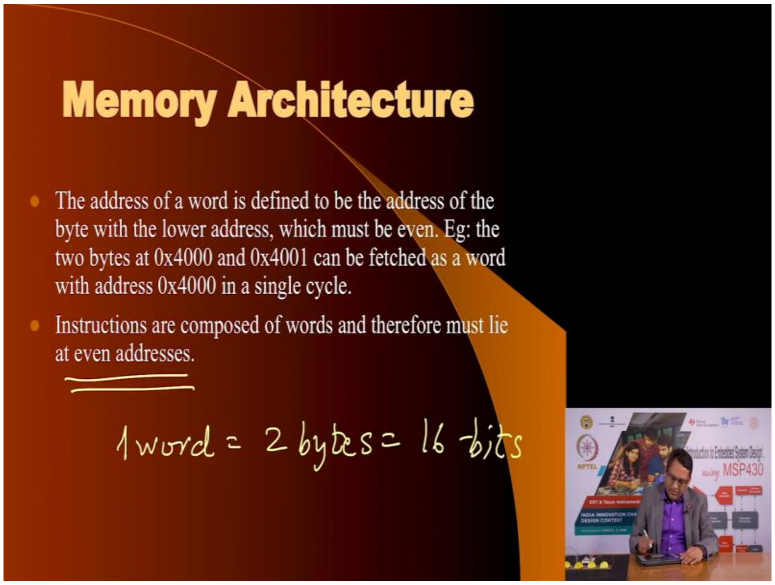

Memory Architecture

- The address of a word is defined to be the address of the byte with the lower address, which must be even. Eg: the two bytes at 0x4000 and 0x4001 can be fetched as a word with address 0x4000 in a single cycle.
- Instructions are composed of words and therefore must lie at even addresses.

1 word = 2 bytes = 16 bits

It turns out that you can only store words starting from even memory locations. The memory is addressed in byte addresses. And so you can only store words which start at a even byte address. And since the instructions are all 16 bits, that means all the instructions are located at even byte addresses. That is the meaning even addresses.

So, your first instruction will be at address 0 and so on and so forth. Now when I have 2 bytes to store and my memory is arranged in byte form. The question is, in what sequence should I store the 2 bytes? So, let me say the 2 bytes are, so this is my LSB lower significant byte and my MSB.

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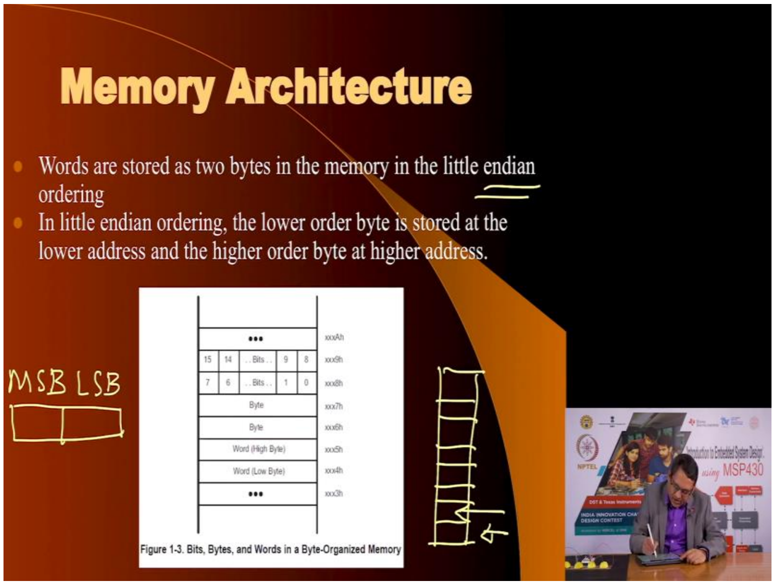

Memory Architecture

- Words are stored as two bytes in the memory in the little endian ordering
- In little endian ordering, the lower order byte is stored at the lower address and the higher order byte at higher address.

Figure 1-3. Bits, Bytes, and Words in a Byte-Organized Memory

And my address is are each address can hold a byte of memory. I have two options. I can store LSB here and I can store MSB here in this location into sequential memory locations, or I could reverse I could store MSB first and I can store LSB later and the way memory words are stored is referred to as endianness of storage. Let me explain this.

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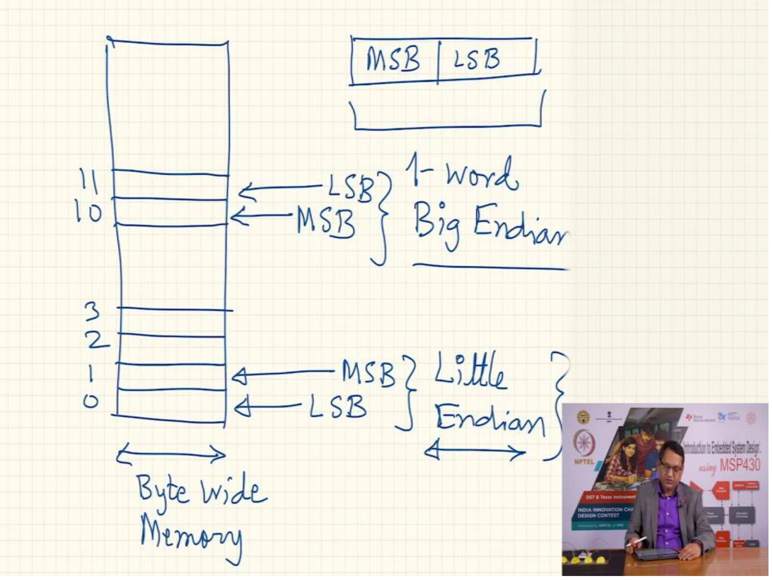


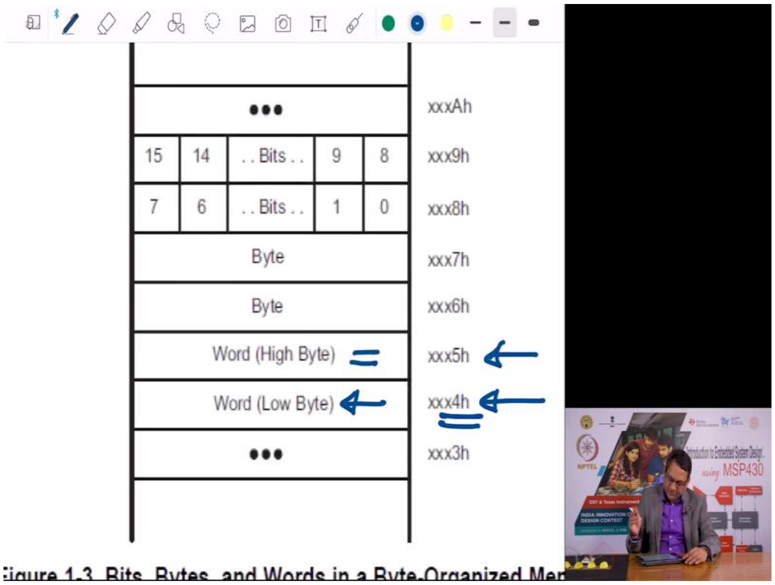
So, let us say my memory has addresses which is starting from say address 0 then 1, then 2 and so on and 3. And let us say I have a word which means I have 2 bytes. The right most is always referred to as LSB and I have MSB. There are two options to store these two bytes in a byte wide this memory is byte wide. This is very important to mention here byte wide memory. That is each location can store one byte byte wide memory.

Given that each locations can store only 1 byte and I have to store 2 byte bites because this is 1 word I have as you can see I have two options. I can store LSB at some address and next address I can store MSB. When I do the following that at a lower address I store the LSB and at the next address which is a higher address I store MSB, this is called little endian.

On the other hand, if let us say at a subsequent address, maybe 10 and next address is 11. If I store MSB first and then I store at the next address the LSB value of the word. This is called Big-Endian. So, as a computer engineer as a electronics engineer who is into embedded system design. It is very important to know the architecture that you are using. What kind of endianness this is the term, I would call endianness is not Endian.

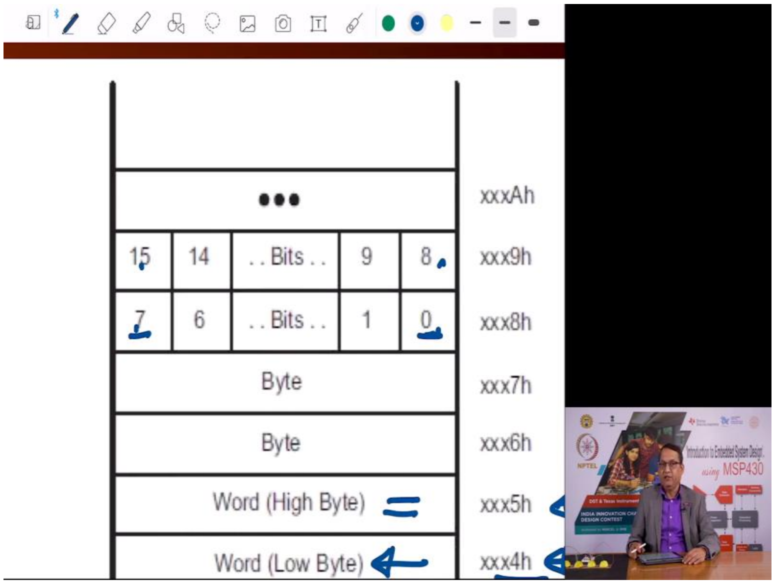
We are Indians but we are talking of endianness how all the endings of the bytes being stored. This is referred to as endianness. So, there are two methods one is the little endian the other is the big endian. For MSP430 they have the designers have chosen to use little endian format of data storage. Let us go back.

(Refer Slide Time: 26:24)



•••					xxxAh
15	14	. . Bits . .	9	8	xxx9h
7	6	. . Bits . .	1	0	xxx8h
Byte					xxx7h
Byte					xxx6h
Word (High Byte)					xxx5h
Word (Low Byte)					xxx4h
•••					xxx3h

igure 1-3. Bits, Bytes, and Words in a Byte-Organized Mem



•••					xxxAh
15	14	. . Bits . .	9	8	xxx9h
7	6	. . Bits . .	1	0	xxx8h
Byte					xxx7h
Byte					xxx6h
Word (High Byte)					xxx5h
Word (Low Byte)					xxx4h

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Now, If you see here, let me zoom this up for you. You see the low byte is stored at a lower address. So, the way to remember is little endian means low byte, low address. High bite high address. This is the safest way to remember, what is the meaning of low-endian and anything else is the opposite of this is high endian. So in low address, this is the lower address. I am storing the low byte and at the higher address I am storing the high byte and this refers to the little endian format.

Within the within each location I can store 8 bits as you see here from 0 to 7. And since I have, if I am storing words, the number of bits will be 16. So, it will go from 0 to 7 and then from 8 to 15 in the higher memory locations because of the little endian format that MSP430 microcontroller follows.

This is the MSP430 G-series memory map, meaning the entire 64 kilobyte memory space. How is it occupied? It is very important to know that and although there are 1 to 5 columns, which means it is referring to 5 different microcontrollers. I am going to concentrate on this column here, which is MSP430G2553 because that is the microcontroller that we are using in our course here. Now, you see the address goes from 0 here if you can see this address.

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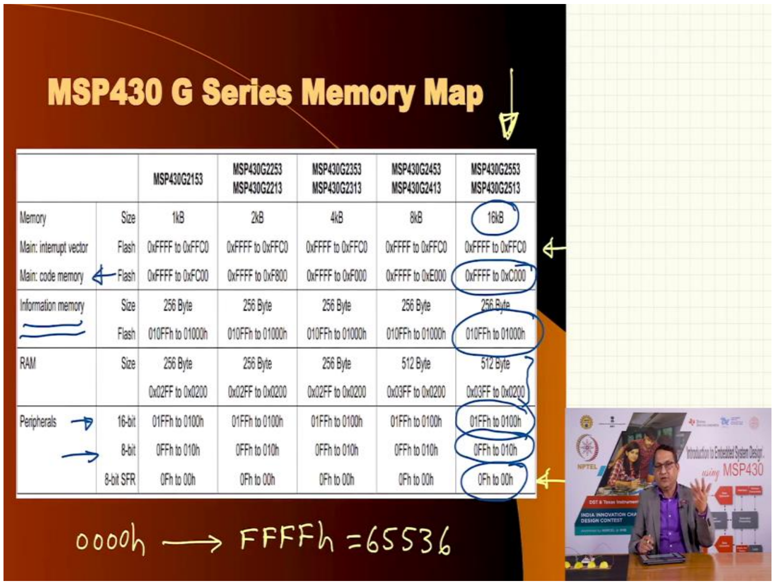

MSP430 G Series Memory Map

		MSP430G2153	MSP430G2253 MSP430G2213	MSP430G2353 MSP430G2313	MSP430G2453 MSP430G2413	MSP430G2553 MSP430G2513
Memory	Size	1kB	2kB	4kB	8kB	16kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xFC00	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000	0xFFFF to 0xC000
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
RAM	Size	256 Byte	256 Byte	256 Byte	512 Byte	512 Byte
		0x02FF to 0x0200	0x02FF to 0x0200	0x02FF to 0x0200	0x03FF to 0x0200	0x03FF to 0x0200
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

0000h → FFFFh = 65536

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This is address 0 and at the top it goes to FFFF in a 16-bit address range. This is the numbers you are going to have. You are going to go from 0000 x to the maximum value is FFFF x and this is equal to 65536 memory locations. So, the way these locations these addresses are utilized is that the lower 16 locations. If you see here lower 16 locations are used to store 8-bit special function registers. These special function registers deal with the input output ports.

The next again, next lot more locations from 10 x that is 16 to FF that is 256. They are reserved for storing 8-bit peripherals and thereafter from 100x to 1 FF. Let us see how the how much that is this is further 256 locations are used to store 16-bit information about 16-bit peripherals. That is such peripherals which require 16 bit of data. They are access in this range. The next memory addresses are used to store the RAM which is the data memory. In this case the address starts from 0200 to 03FF and this let me explain.

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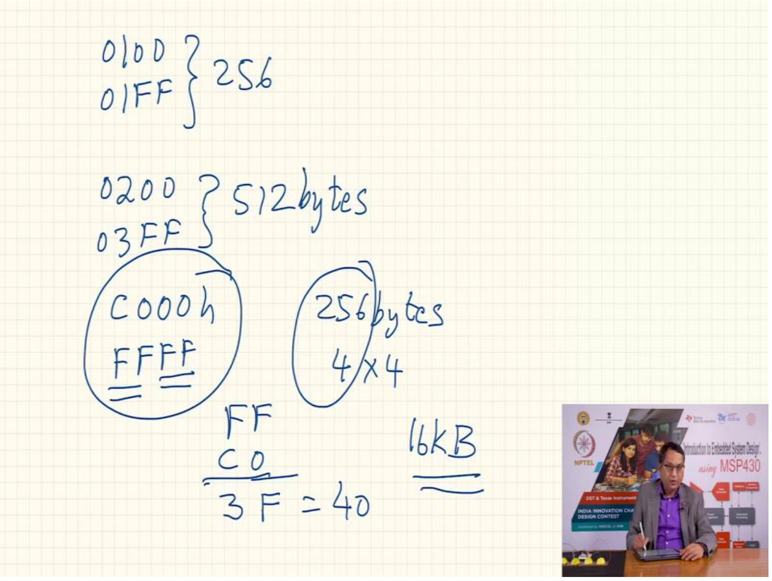

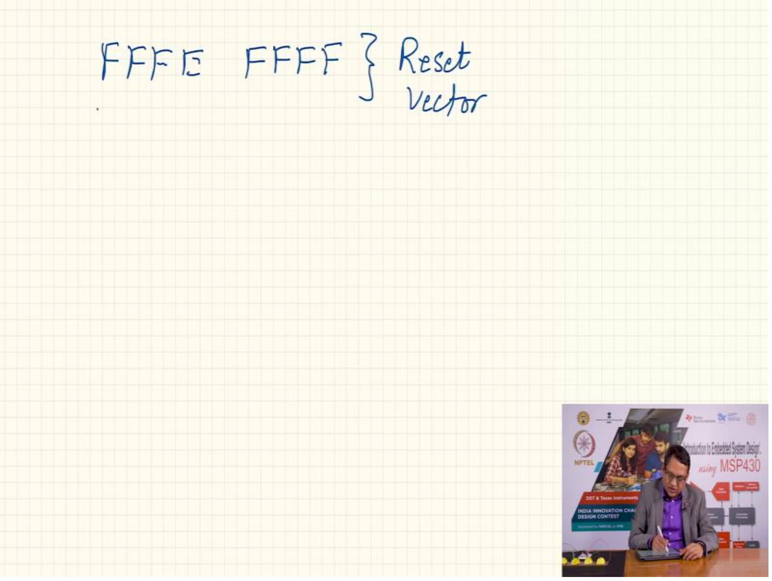

This is if I go from 0100 to 01FF these are 256 memory locations. In our case, we are going from 0200 to 03FF and these are 512 bytes of 512 locations. That means in this range. We are we have mapped the MSP430 microcontroller mapped RAM in this memory location. And so this is what we have.

Thereafter there is some gap and you come at here, which is 01000 that is 1000 to 10FF and this is called as information memory. Now information memory is also flash memory except this information memory is used to store user data that you would not want to be lost if the power is switched off.

So, this is basically a flash memory and in the G 2553 microcontroller you have 256 bytes of flash memory defined as information memory and at the top we have the main program memory. In this case, we have 16 kilobytes and this is the address range actually of which there are the 16 kilobytes are utilized in two way. So, the starting address is C2 C3000 to four FFFF's. Let me mention what it is. So, our address are C000h to FFFF we have already seen that the lower two digits refer to 256 bytes of memory.

And here we have FF minus C0, so it will go from C0 to CF, then D0 to DF, then E0 to EF and F0 to FF and each of these pages is to like 16 locations. So, we have total of 256 bytes into C0 to CF is 4 segments and like that we have total of into 4. So, this into this is 1 kilobyte and so this is a total of from 00 to 40 and 40 here means 64 pages.

So, 64 into 256 bytes will give you 16 kilobytes of memory. So, the difference between these two numbers is 16 kilobytes of memory and these 16 kilobytes of memory is what is available on 2553 microcontroller of this the top locations FFC0 to FFFF are stored to store vector locations and these are 32 locations each having the storage of 2 bytes. That means a total of 64 locations and I am able to store 32 interrupt vectors and the top of the address that is that is FFFE and FFFF these are two memory locations. This is the Reset vector.

So, what happens when you reset this microcontroller or this microcontroller is reset in any which way whether it is the user reset or whether it is a brownout reset or watchdog reset. It goes to this memory location. At this memory location it reads the value and it jumps to that memory location, which has to be in the in this code memory region and from there, it will fetch the first instruction interpreted executed increment the program counter and get go to the next location and so on and so forth.

So, this is the way the entire memory map of G2553 microcontroller 16 64 kilobyte memory map is utilized for storing the peripherals the RAM the information memory and the main code memory as well as storing the interrupt vectors. So, we stop our lecture here, and we will resume in the next session and will continue this discussion about MSP430. Thank you.