High Power Multilevel Converters – Analysis, Design and Operational Issues

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Lecture – 39
Gate Driver Circuits – Turn - on and Turn- off Process

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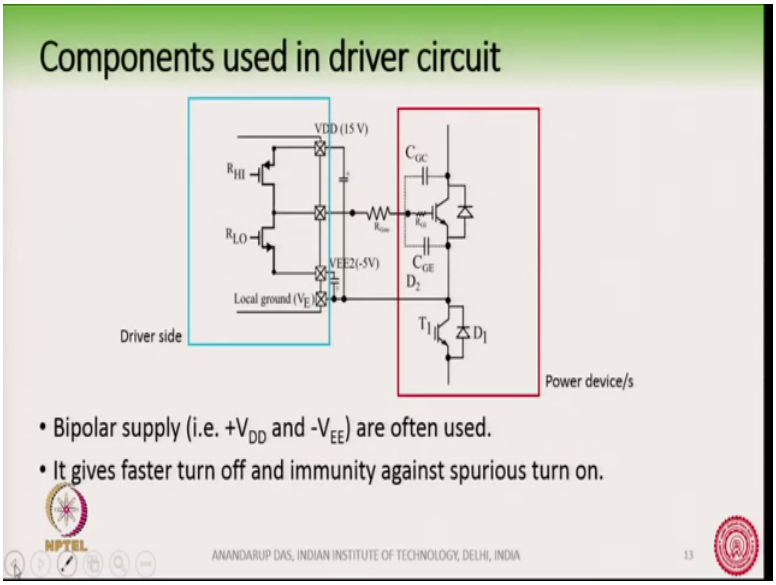

An additional point to keep in mind is that you may choose V DD to be 15 volt and instead of a minus 5 volt you may choose to have a 0 volt. So, therefore, this there will be a local ground; here, you will connect it to instead of minus 5 you will connect it to a 0 volt, this is also possible and is used. However, the minus 5 volt gives you certain advantages. In particular, nowadays when the MOSFET's are getting a lot of development. I would means we would say that a minus 5 volt will give you advantages faster turnoff and immunity

against spurious turn on, these advantages will be particularly helpful for silicon carbide based MOSFET's.

So, the application notes from the manufacturers recommend many of them, most of them it will say that recommend a bipolar supply that is plus V DD and minus V E for such high frequency MOSFET's.

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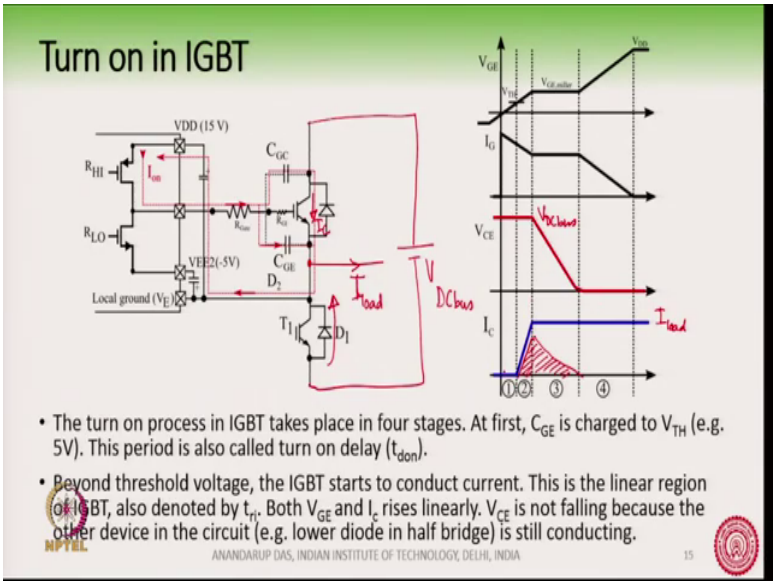

Next is the turn on process in the IGBT. So, now, we will study the switching characteristics. So, we will focus now on the, what happens during turn on. Now in order to understand this turn on process, we will see this circuit a little bit in details. So, you can see here there are two IGBT's connected, following the course structure with which was heavily based on half bridge structure I have tried to use such a circuit.

But it is also the analysis is also valid for other types of circuits. Now the DC link for example, is present here ok, the DC link is for example, present here and you will also have the load current flowing out here ok. Now so, this is the half bridge structure here and this is the driver of the upper side IGBT and we have this as the gate resistance, this is the internal gate resistance of the device and these are the two capacitances which we want to charge up during the turn on process. And these are two additional capacitors which are usually connected externally to provide the gate charge which is needed by the power device.

Now, the turn on process in the IGBT usually takes place in four stages at the first stage C GE, this capacitor here this capacitor charges up to the V threshold voltage and this period is called the turn on delay. So, threshold voltage is the voltage after which the device starts to conduct and again we this C G. So, you can see here that the V G E voltage initially was minus V EE or about minus 5 volt and it has started to build towards V DD that is the 15 volt. So, this value here V DD is plus 15 and this value is here minus 5 volt and we have just discussed that minus 5 volt has certain advantages.

So, that is why before the start of the turning on this V GE voltage was minus 5 volt. Let us assume that and now we are trying to charge up to the V DD voltage and of course, how is the circuit? So, if you follow this red lines you can see that this it. So, during the turn on process this MOSFET is on ok. So, the current is flowing from here going like this, going like this and then going like this and coming back like this.

So, this is the circuit here. This point here is the, we say it is a local ground this is basically connected to the midpoint or to the emitter of this IGBT. So, this is a local ground it has nothing, it is completely isolated from the controller ground ok. We assume that this points potential is 0 ok.

So, you can see here that this, this one is going like this. So, this is the current flow here when the capacitor C GE is charging up of course, it will charge up in and R C time constant, but this R C is. So, large that we can assume that it is linearly charging up, now beyond this threshold voltage what happens the IGBT, starts to conduct current and this region is called

the linear region of the IGBT why it is called linear region because both V G E as well as I C will rise linearly during stage 2 ok, this is the stage 2.

So, I C is rising linearly here and V G E is also rising linearly, actually it is an R C, V GE is rising in a R C time constant, but this time duration is very small.

So, when the IGBT has started to conduct then the current is like this here, both this current is flowing ok. Now one thing to observe here is that V CE during this time, during this stage 2 V CE is not falling away, of not falling why V CE is not falling.

Because the total current, the current which is flowing through the IGBT this is the I C current here, this is the I C current here not this one. So, this is the current I C here, this current is not equal to the load current. So, this is the load current here ok, this is the load current.

So, I C has not taken up the whole load current ok, if you think that the load current is a big current source then the if I C, I mean the IGBT has not taken up the full load current then the rest of the current must be flowing through this diode ok, because the load current is a current source and the total current should be constant.

So, therefore, this diode was is still conducting and since this diode is conducting therefore, this points potential if you neglect the diode drop this points potential is same as this points potential and hence the voltage across the IGBT is still equal to the DC bus ok. So, this is the DC bus voltage. So, if this is the V DC bus. So, this voltage will be V DC bus here. So, the IGBT the voltage across it is equal to the DC bus whereas, the current is rising up here, this is a stage where there is a loss in the IGBT why because the loss across the IGBT is V CE times V CE times I C ok. So, there is a V CE voltage here, there was very little loss because I C was 0 there was a V CE.

But now here there is a V CE equal to V DC bus and then there is a current rising here if you plot the V CE the loss here you will see that there is a loss happening here in this region stage 2 because there is a I C current and there is a V DC voltage and the loss is linearly rising here.

So, the loss is something like linearly rising here and again as you can understand in stage 3, there will be a loss which will be like this V CE times IC. So, there will be a loss in stage 2 and 3, anyway we will come to the stage 3, but in stage 2 you can see there is a loss happening fine.

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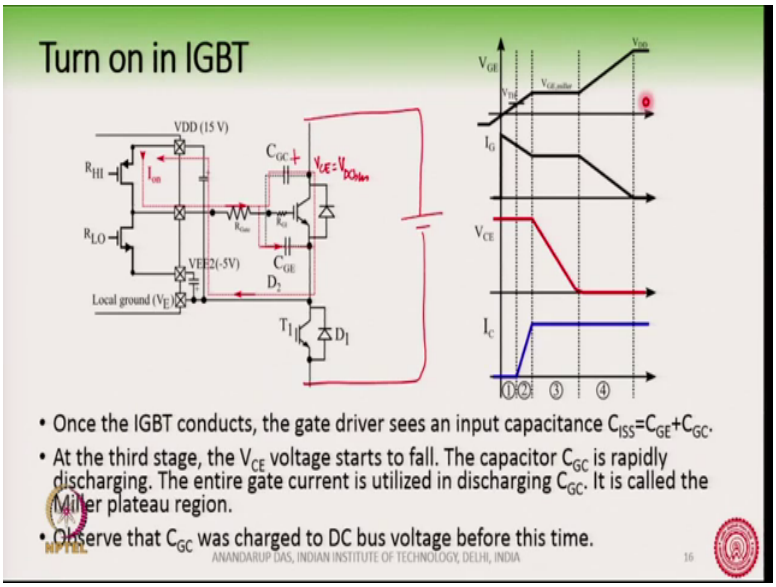

Now, what happens in stage the once the IGBT has started to conduct the gate driver, this gate driver is seeing a input capacitance which is the parallel combination of two of these

capacitors you see this switch has started to conduct. So, this path will have two parallel capacitors here. So, these two capacitors are in parallel.

So, this is seeing an input capacitance which is the parallel combination of two capacitors. Now comes a very important stage and this is the stage that called the third stage which is the stage at which V CE voltage will start to fall. Now the current has reached this limit and the V CE voltage has started to fall.

Now, at this condition you see that this capacitor is basically discharging during this now how or why this capacitor is discharging? You can see that, before this stage what was happening is this capacitor here is charged to V CE which is equal to V DC bus, if this is the DC bus voltage.

So, this points potential was equal to the DC bus voltage whereas, this points potential was somewhere here ok, which is maybe around 8, 9, 10 volts something like that. Whereas, this voltage if the DC bus is say 600 volts then this points potential is 600 volts right. So, you can see understand that this capacitor C GC has a huge voltage applied across it.

And so, it is having a lot of charge inside it, unless we take away that charge we cannot fully so, because we, we would like to take away that charge in order to turn the transistor fully on. So, at this point so, in this stage 3, this capacitor has to be fully discharged and the total charge and so, this region you can see here this region is called the miller plateau region ok. In this region this capacitor is completely discharging tremendously. It is discharging and a huge amount of charge from the gate driver circuit, from the gate driver, from this point a huge amount of charge is needed to discharge this capacitor here in the miller plateau region ok.

In this condition this voltage will more or less remain constant here ok, slightly it will increase, but it is more or less we can say the voltage here will remain constant because this capacitor is discharging through this. So, this is the third region again in the third region there is a power loss.

So, the power loss is happening in stage 2 and stage 3 or region 2 and region 3.

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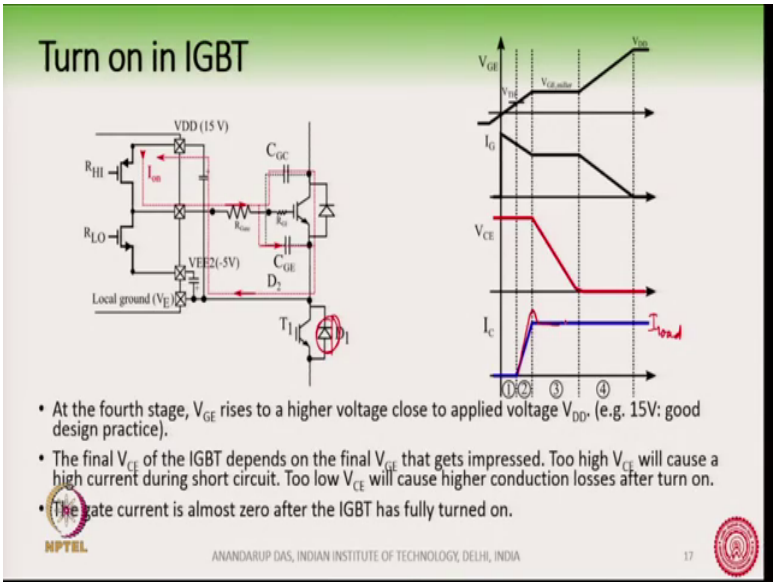

Once this capacitor has been fully discharge then the voltage, the gate emitter voltage here will rise towards V DD because this is what it was supposed to rise as per this R C diagram, this voltage or this V G E voltage should rise up to the V DD voltage 15 volt.

Again as I told you from the static characteristics the magnitude of V DD can be 10 volt, can be 12 volt, 15 volt, 18 volt you can choose this value. So, if you use too high means very high value of V CE then it can cause a high current during short circuit whereas, if you use a very low value of V CE it will cause higher conduction losses after the device has been turned on ok.

Now the gate current is almost 0, after the IGBT has fully turned on. So, you can see here the gate current has almost come down to 0, there is a slight modification, but I would like to make this I C current is not exactly like this, but there may be a slight like this I C current there may be a slight peak here and this peak happens because of the reverse recovery of this diode here ok.

When there is a reverse recovery of this diode then this collector current may not kind of like fully become equal to load current, but there may be a slight overshoot here. So, that is sometimes observed.

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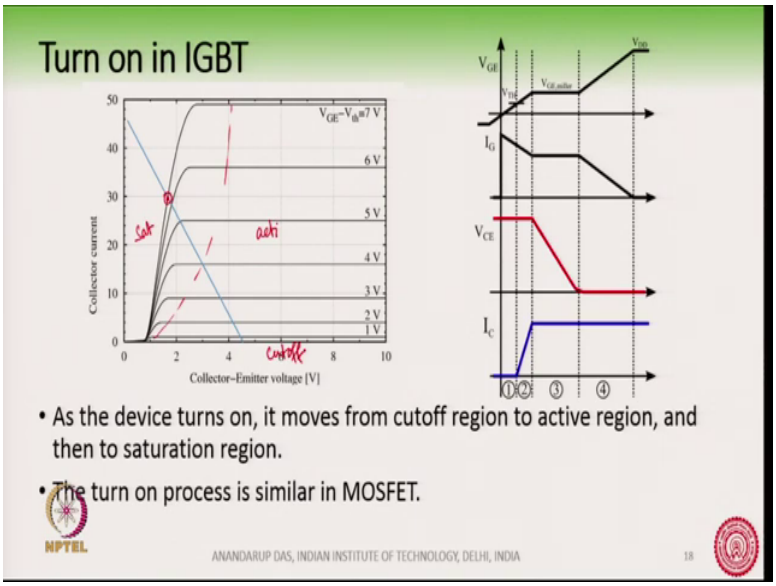

So, we can say that, if we see this I C versus V CE characteristics of the device then I can see that it has now moved from the cutoff region through the active region and have settled at the saturation region.

So, this is the saturation region here it will settle. So, so it is like something like this this is the, this left hand side is saturation region, this is the active region and this is the cutoff region of the device the IGBT, the turn on process whatever I have discussed is very similar also in a MOSFET, the MOSFET and IGBT the gate side of it is very similar in structure.

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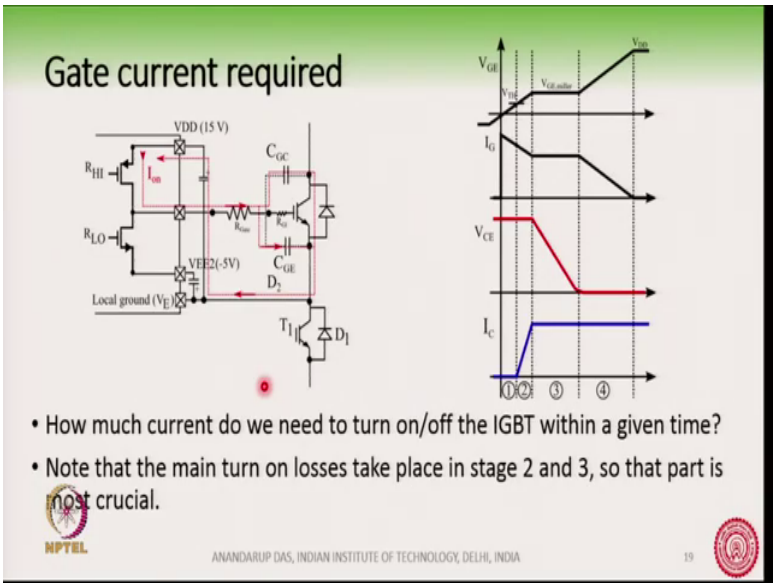

Now, once we have understood the process then the question comes how much current do we need from the gate driver. So, this is our gate driver here how much current will I need from the gate driver within a given time.

Now, in order to understand this we should also make a note that the main turn on losses of this device is taking place in stage 2 and 3 ok, this is these are the 2 stages in which the losses are taking place.

So, if we can reduce this time then it is beneficial or it is advantageous in reducing the turn on losses. So, these 2 times, if we can reduce it then we will reduce our turn on switching loss or turn on loss this time unfortunately this stage 2 and 3 cannot be reduced too much, because it will have other consequences. So, we will always have a design compromise. So, what are the other consequences we will talk about it ok?

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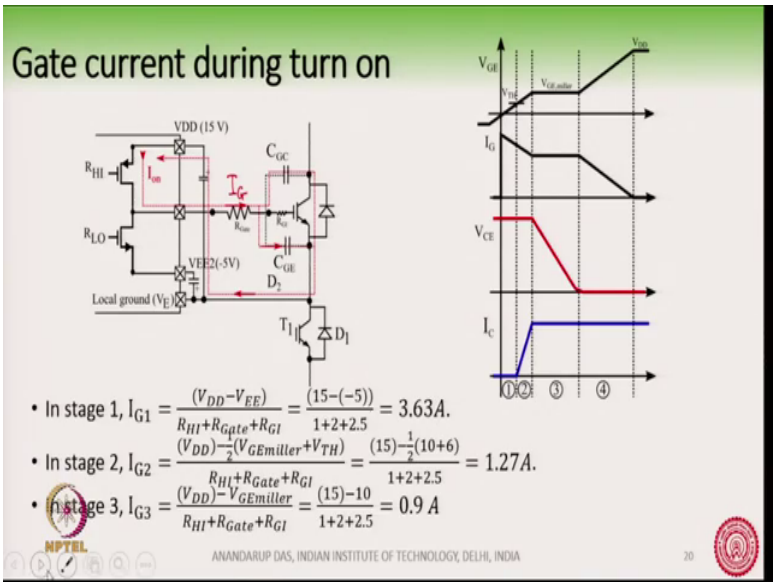

Now, we can roughly get some values based on the, whatever discussed about how much are the currents that may flow. So, you can see that how much are the gate currents which are flowing at different stages.

So, let us take stage 1 first. So, in stage 1 if you apply the KVL, then this is the gate current, here this is the current which we are talking about I G this is the current here. So, this current if you see here the circuit this is V DD the, when this MOSFET is turned on, we can assume that there is a on state resistance R high, R high as the on state resistance when this MOSFET turns on then this is R low resistance.

So, you see here this is the 15 volt V DD and then there is a R high and then there is a R gate, this is a resistance which we will externally connect because we would like to control the gate current ok, because we would like to control how much is the turn on interval? How much is the time for which stage 2 and 3 has to be applied?

So, that we can control the switching losses of the power device, so, this is this gate resistance R gate is a element which has a profound effect in controlling the losses. Of course, then we have this C GE and C GC and then the circuit is getting completed here fine. So, then we can find out what is the approximately, what is the gate current I G 1 at the stage 1 at stage 1, you have V DD voltage and then you have here this voltage here is minus 5 volt ok.

We have already said that when we turn off we turn off. So, that the V G E voltage is minus 5 volt. So, therefore, V DD minus VGE, so, this current is this voltage minus this voltage divided, sorry the total voltage in this loop divided by the total resistance in the loop. So, the total voltage is this much and the total resistance is this much R high plus R gate plus R gate internal.

So, these 3 we have added. So, we have taken some values which also we have obtained from the datasheet of this SKM 300 GB 12 V 4 that particular IGBT. So, we took some values from there. So, V DD is 15 V EE is minus 5 volt ok.

Now, here minus 5 volt sometimes people do not use minus 5 sometimes they use minus 8 also, its a designer choice ok. So, 15 minus 5 and then R high we have taken one ohm R gate 2 and then R GI 2.5 and we get this amount of current this is the peak current I G one here roughly this is the peak current here.

In a similar way I G 2 that is the average current I mean here the current roughly, here the current what is the current here then you see here the V G E voltage V G E again we will apply the KVL the V G E voltage we can assume like midway between V threshold and V G E miller.

So, we have taken half of V G E miller and V threshold and V DD is the applied voltage. So, this is the net voltage in the loop and this is the net resistance in the loop and this value is 1.27, these values V G E miller and V threshold I have taken from the datasheet in stage 3 the V G E voltage is equal to V G E miller. So, therefore, I G 3 is 15 minus 10 divided by this and 0.9 ampere ok.

So, we can get a rough approximation of the magnitudes of current which is obtainable and so, with magnitude of current which is required and so, the gate driver circuit should be able to supply this magnitude of current.

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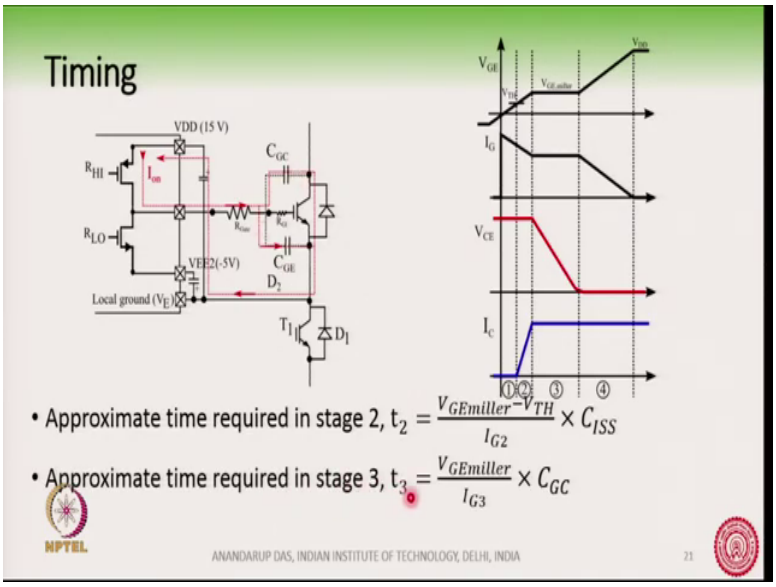

Again, approximate time how much is required in stage 2, again these are very crude approximations as I told you these values of capacitance and all they are varying with voltage. So, a very rough approximation is saying like the time required in stage 2 is how much the total charge. So, I G 2 into t 2 is the total charge and this total charge is equal to C times V so, V G E miller minus V threshold into C ISS.

So, this is the equivalent capacitance here and approximate time required in stage 3 is the V G E miller is the voltage and because in stage 3 as I told you the entire charge is used in discharging this capacitor C GC, the entire effort is utilized in order to discharge the C GC. So, therefore, this time I t 3 into I G 3 is the total charge which will be equal to V G E miller into CGC.

So, that much of charge will be required from the gate driver mode. So, these are the, from this we will approximately get these values again a very crude approximation.

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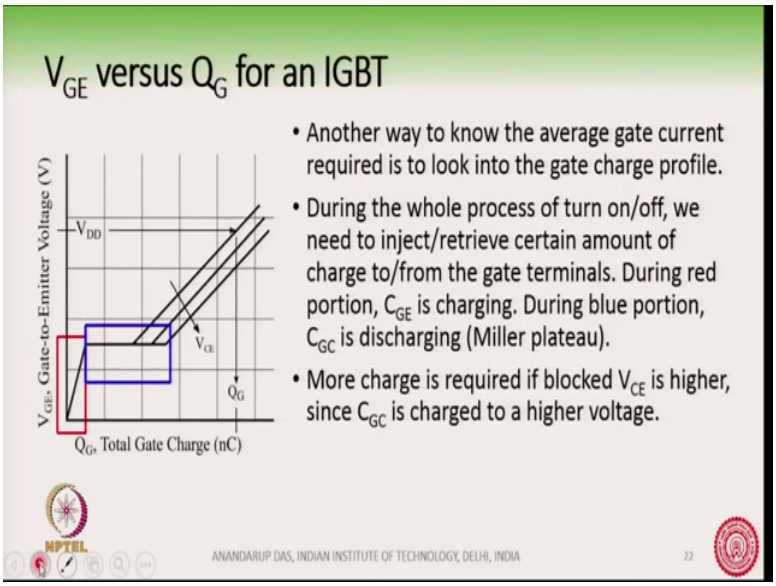

Now, often people do not go in that fashion often people design it in a slightly different way instead of exactly finding out what is the current required and what is the time required the other way to know is to look into the gate charge profile of the device. So, another way to know the average gate current or. So, there are to look into the gate charge profile ok.

So, often people design the gate driver is based on the gate charge profile. Now what is the gate charge profile basically, gate charge profile tells you how much is the gate total gate charge required by the device in order to turn on or turn off ok. So, instead of looking into

individual stages of turning on, they look it at a cumulative way that in order to turn this device on I require so much of gate charge.

Now, how fast you will deliver this charge if you do it very fast you will be turning the device faster if you do it slow you will turn the device on slowly. So, this gate charge how much gate charge is needed is often available in the datasheet.

So, here you can see I have taken from this is a genetic data sheets I. So, this is the total gate charge on the x axis and this is the V G E voltage ok. So, you can see here that as V G E voltage increases ok, as the V G E voltage is increasing the total gate charge is increasing and this is the miller plateau region where you can see that the V G E voltage is almost flat.

But there is a lot of charge required to discharge the gate collector capacitance and this is the initial t 1 stage. Now when the, you can see here that there are 3 curves shown and these 3 curves are for different values of V CE that is the different values of the DC bus voltage ok.

So, of course, we can understand that gate collector capacitance, if the DC bus is more than the gate collector capacitance is also charged more and hence we will need more charge to kind of like discharge this capacitor. So, therefore, as V CE or the as the DC bus voltage increases, we will require more amount of charge in order to fully turn on the device fine.

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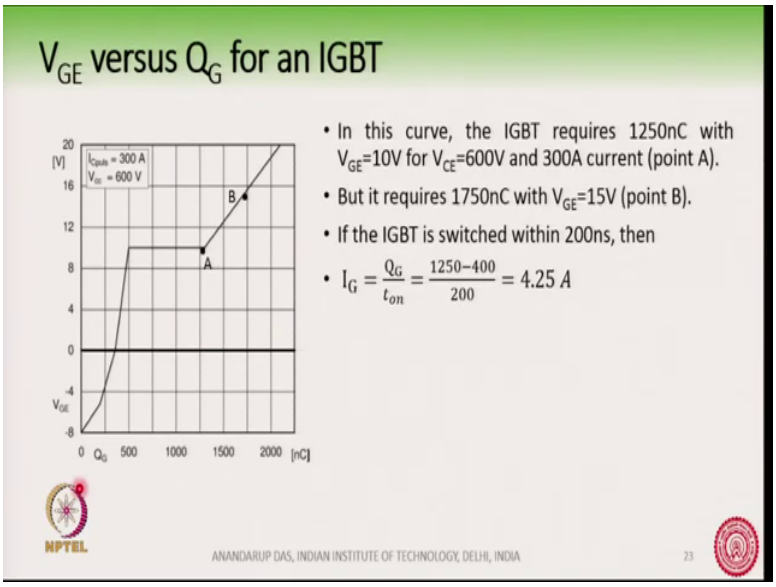

So, here this is a more specific example, which is again taken from the same datasheet of the device which we talked earlier and here you can see the values given right. So, this is the whole turn on process, you will see this turn on process starting from so, in this case the device was started from minus 8 volt.

So, it that minus V EE that was minus 8 volt, in our case we have taken it minus 5 volt anyway that the concept is same. And this device will go the this data is shown for 300 ampere and with V CC of 600 volt; so, the V G E which was used for this. So, if you, if you if you observe this curve here you can settle at point A or you can settle at point B ok.

So, if the V G E voltage is 10 volt, then you will come and settle at point A and then you will require a less amount of charge maybe around 1250 nano coulomb. Here you will come here 1250 nano coulomb, but if you increase the V G E took the point B ok, this is about 15 volts

here then you will need about roughly 1750 nano coulomb of charge starting from the complete off stage 2 a complete on stage of the device ok.

So, the device has basically traveled from this to the point B and then in this whole process this area here under this curve this area this is about 1750 nano coulomb. So, this much of charge will be required to turn the device from fully off stage off state to fully on stage. Now if you say that I want to switch this device within 200 nanoseconds then roughly or an in an average sense I can say that the gate current required will be the total charge divided by ok.

Now, here the as I told you the main charge, the main switching transition is from in starting from stage 2 to stage 3. Now in this one in these characteristics where is stage 2 starting ok. So, this is of course, the stage 3 and going up here last stage. So, stage 2 starts somewhere around here ok.

So, therefore, we can say that the total charge which is needed because this is where the switching loss is happening and that region is about 200 nanosecond, we would like to keep it at 200 nanosecond so, therefore, the charge required is 1250 minus this point here and in this point there is a 400 nano coulomb already taken away.

So, 1250 minus 400 it is 200 4.25 ampere, this will be the current average current required from the gate driver circuit ok. So, this you can this many people use to calculate how much will be the driving capability of the gate driver circuit.

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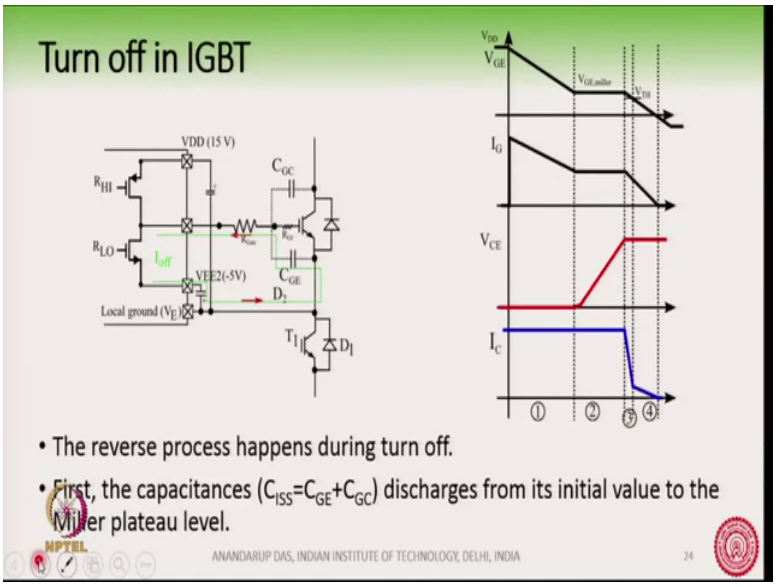

Now, the turn off process, that is the other process of course, the turn of process is an exact replica, but in a reverse fashion this just reverse thing is happening. So, at first the capacitances these two capacitances are discharging from their initial value. So, how is that? How is the circuit behaving? So, you can see here that this capacitance is going to be so, going to be discharge through this MOSFET during turn off, we will turn on this MOSFET and turn off this MOSFET.

So, it will go through like this go through like this and will complete the path like this here and of course, you can see here that this is charged to minus 5 volt in this example. So, it is like this here. So, the gate emitter voltage at the end of turn off will come to minus 5 volt because this is plus terminal. So, this will come here and so this point and so, it this capacitor

will be charged to minus 5 volt at the end of the turn off the whole process of turn off, again there are 4 stages during turn off ok.

So, the capacitance initially this C ISS both of them are discharging from its initial value to the miller plateau level.

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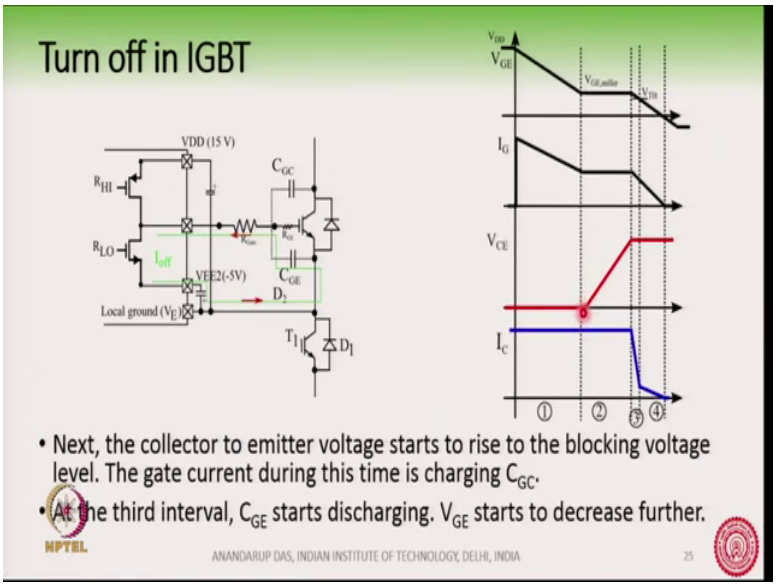

And then like the previous phase second stage V CE voltage is rising whereas, the current is still maintained and at the third interval the C GE starts decreasing that is this C GE capacitor is starting to decrease.

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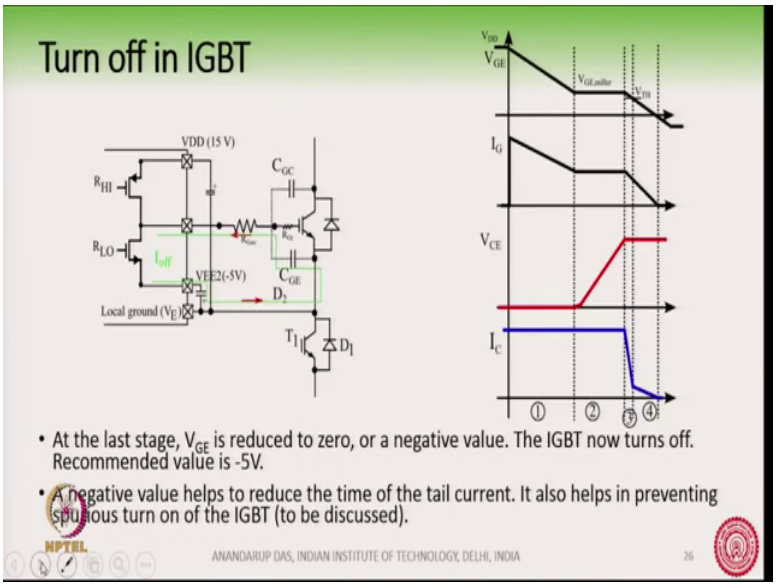

And then the ultimately at the fourth stage this voltage V G E goes to minus 5 volt and the IGBT will turn off fully ok. Another particular exam help why V G E is negative is that in case of IGBT there is a long tail current because there are excess minority carriers which needs to be recombined and so, in order to reduce or in order to, in order to quickly take away these minority carriers.

Otherwise there will be a long tail current we also keep a minus V G E.

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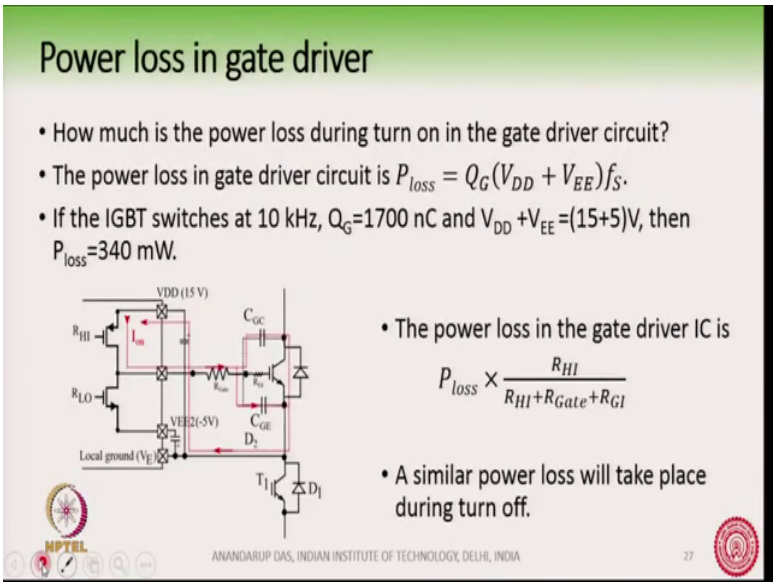

Now, what is the power loss in the gate driver as well as in the gate resistance? How much is the power loss? So, the because why this is important because not only we have to when we are taking a gate driver I C, we have to see how much current it can deliver and how much is the power loss that it can sustain to drive this IGBT ok.

So, so, we need to know how much is going to be the power loss. Now how much is the power loss for example, during turn on the total loss will be Q G times this voltage through which it is transitioning it is transitioning from V DD to , during turn on the total voltage getting applied is this much and this is the total charge which we have taken and the switching frequency.

So, this will give you the total power loss. So, suppose if you take an example if this IGBT is switching at 10 kilo Hertz and QG is 17 nano 1700 nano coulomb and this total voltage is 20

volt, then the loss total happening is 340 mainly what this is the total loss happening of course, this loss will spread over this resistance, this resistance and this resistance here ok. So, the power loss in the gate driver I C is proportional to the resistance here. So, this is the total loss happening inside the driver IC and another fraction will be happening in this R gate here ok.

So, then you can choose what type of a resistance you will use external gate resistance so, that it can deliver the peak current as well as can sustain this loss ok. So, this was the expression of loss when it is turning on and then similar power loss expression or value will happen when the device is also turning off, another thing that is to be kept in mind if you see the datasheet of these power devices you will see that the turn on and turn off times are usually quite different and so, they will require separate consideration ok.

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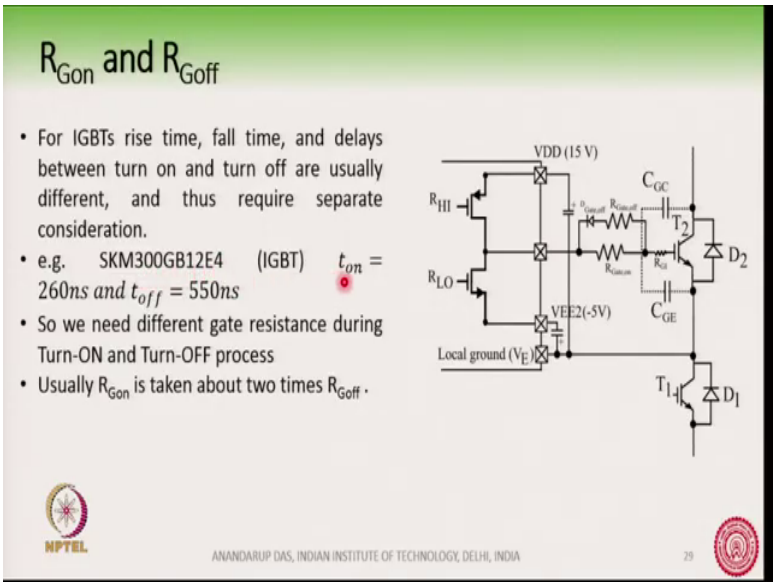

For example for this IGBT t on is 260 nanosecond and t off is 550 nanoseconds something like that ok.

So, this means that we need different gate resistances during turn on and turn off process ok. So, here you can see one circuit which has two different resistances during turn on this R gate on; this resistance is comes into picture this is how the circuit is flowing this R gate on because this diode here is reverse biased whereas, during turn off a parallel combination of these two resistances come into picture ok.

So, it has been generally found out that R G on is taken about 2 times RG off again it its again a designers choice how fast you want to turn on and how fast you want to turn off RG off and RG on has other implications also.

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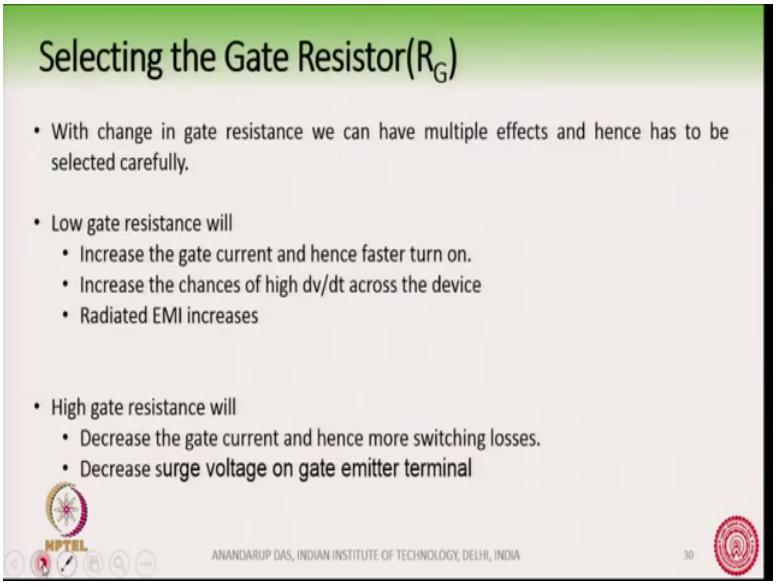

So, we see that the gate resister RG has, have multiple effects and it has to be selected very carefully. So, far we have only seen that suppose if you have a low gate resistance then, we can increase the gate current of course, if the resistance is low we can allow more current to flow and we can have a faster turn.

On the other hand, if you use a high gate resistance then you will decrease the gate current your requirement from the driver I C will be less, but you will have more switching loss because the R C time constant will increase and it will take more time for the switching process to take place for the transition to take place and so, the losses will be more ok. But there are other issues like if you have a low gate resistance, then it increases the chances of high dv dt across the device.

We will come to these issues. It is also reported that with a low gate resistance the radiated EMI increases from the device, on the other hand if you use a high gate resistance then it decreases the surge voltage on the gate emitter terminal ok. We will see these some of these parasitic effects as we go on. But this is kind of like a overview that what the gate resistance can control in the device.

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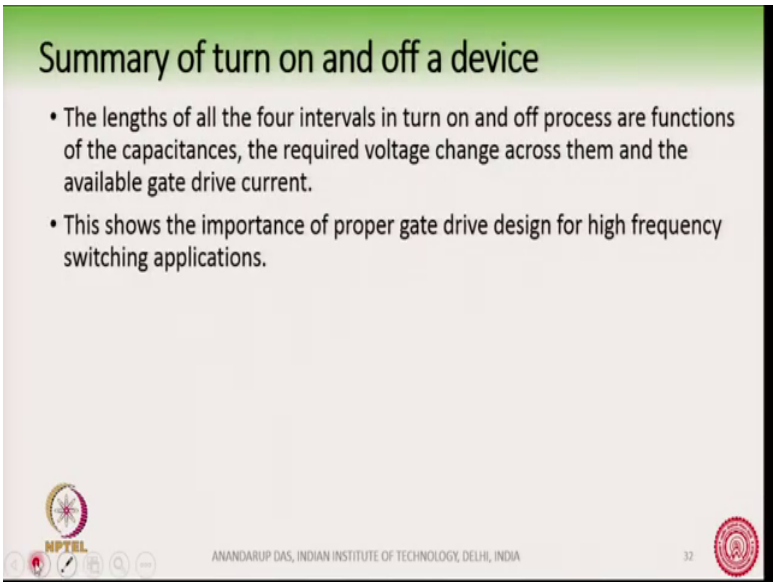

So, this is what I wanted to summarize that this length of all these four intervals in turn on and turn off process are function of the capacitors, the required voltage change across them and the available gate drive current ok. So, a gate drive design for high switching frequency application. So, it is important to properly choose these components.

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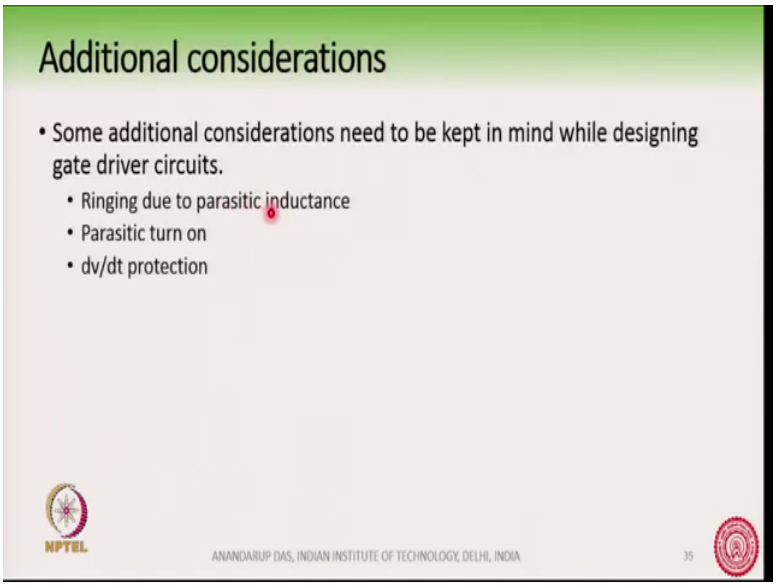

Now, let us see some additional things that we should keep in mind, what are these additional things? Number 1 is the ringing due to parasitic inductance, then we have also parasitic turn on and then we have a dv dt protection. So, let us see what are these things.

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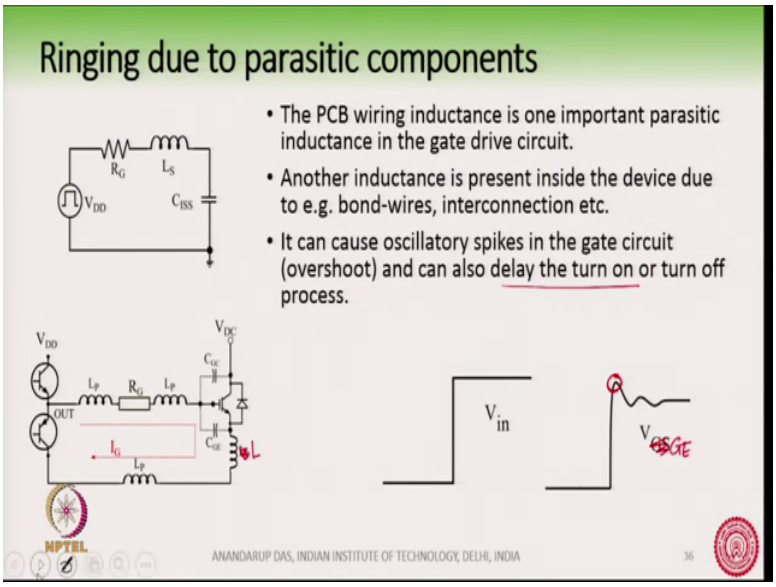

Now, what is the ringing due to parasitic components?

Now, the, although so, far we have not talked about any inductance in the circuit, but actually all these circuits have inductances where are the inductances? Number 1, there is a PCB wiring inductance because the gate driver circuit is on a PCB whereas, the power device is away from the gate driver circuit.

So, there is a PCB which will connect the gate driver I C to the power device and this PCB has a routing of wires which has an inductance and this plays a major role in particular for high switching frequency application. So, we would definitely want to make this distance.

So, this so, here it is shown this circuit this L P, these are part of the PCB wiring inductances ok. So, these should be minimized as much as possible ok. Now another inductance which is

present inside the device is this one here this one although I have there is a mistake here it should not be L P we should give it some other name say yeah some other L ok. So, this inductance is actually a part of the device because inside the device there is a bond wire and there are interconnections and so, there will be an inductance inside also and this will also play a role and will contribute to the total inductance in the circuit.

So, if we see this circuit carefully, we will see that this circuit is not exactly an R C circuit; rather it is an RLC circuit with these inductances in picture. So, this will is a this will follow a second order system response. And so, what will happen is that, if this is an under damped system then the this voltage gate emitter voltage will not be we would ideally want to have a gate emitter voltage like this, but because of the RLC circuit the gate emitter voltage will be oscillating like this here ok. So, this one should be V G E ok. So, this voltage here will be oscillating in nature ok, this is something which has must be.

So, this is because of the parasitic inductances in the circuit, but it must be kept in mind ok. So, what is the effect of this not only with this? So, not only will there be a peak ok, but this can also delay the turn on process of the device ok. So, these are the important effects of this inductance.

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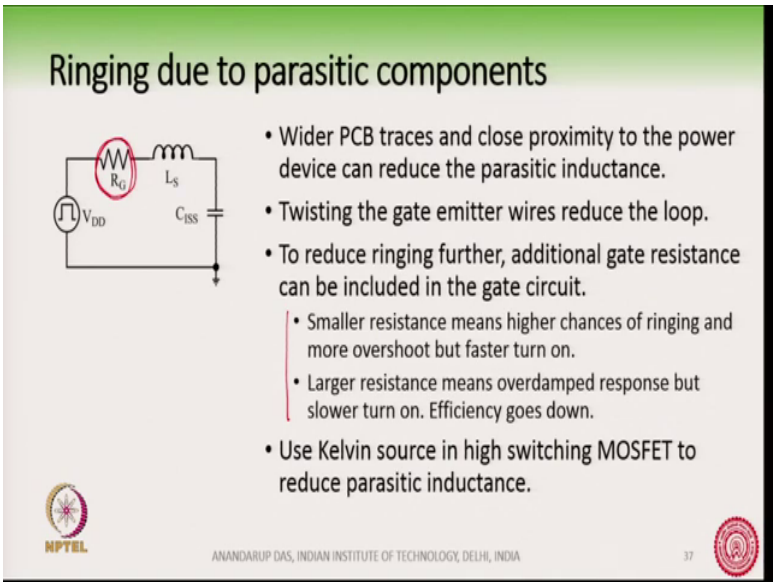

So, how can you mitigate it? Of course, if you use a wider PCB trace and close proximity to the power device you can reduce, you can reduce the parasitic inductance people sometime use twisted gate emitter wires rounding the loop. Now another way because since this is an under damped system another way to mitigate this effect is to put additional gate resistance ok.

So, basically if you increase this value here, you can do that by increasing the gate resistance. So, if you increase this value it the system will go from an under damped to a critically or over damped system. And so, smaller resistance means that higher chances of ringing and more overshoot, but smaller resistance means faster turn on, smaller gate resistance means faster turn on. Whereas, larger gate resistance means over damped response, but slower turn on and more losses.

So, you see often that this parasitic inductance is not known beforehand. So, you cannot so, you have to first put a value of gate resistance and see the performance. If the performance is satisfactory then you go ahead otherwise you have to modify the gate resistance a little bit so, that you can make a design compromise between these two factors here ok. So, this has to be kept in mind.

Another one in particular for MOSFET's, when you go for a very high switching frequency MOSFET, say several hundreds of kilo Hertz then one way to reduce the parasitic inductance is to use a Kelvin source.

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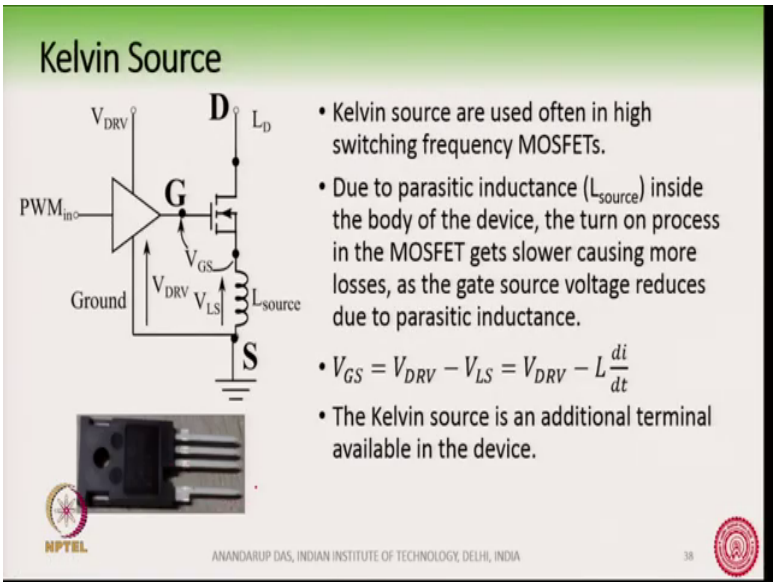

So, Kelvin source I think we have shown you sometime back in one of the classes a Kelvin source MOSFET has 4 terminals ok. So, it is an additional terminal available in the device. So, what happens there, now as I told you the MOSFET has some additional inductance

inside the power device probably this is coming from the bond wires and from the interconnections like this. So, inside the body of the device and so, what will happen is that the turn on process in the MOSFET will get slower ok.

Why? Because if you see this VGS voltage, now this VGS voltage will be V drive minus. So, I assume there is no loss in this totem pole here. So, VGS my equal to V drive minus VLS minus this voltage VLS here.

So, this is equal to VDR minus L di dt and so, when the current is rising through this MOSFET this value will cause VGS to fall when the current is rising that is what is happening during turn on. So, this VGS actual voltage which is available across the gate source terminal of the MOSFET is low than the V DRV or 15 volt ok. So, therefore, people what they have done is in order to reduce the effect of this inductance they have taken out a terminal from here and is has made it available to the user as the fourth terminal ok.

So, this is the Kelvin source, it is an additional terminal which tries to mitigate the effect of this L source. Now, another thing that I would like to comment on here is that remember this RLC circuit here is this RLC circuit here also has another component which is not shown and that is this source, this source here ok. This source also is not an ideal source ok, we have taken here as an ideal source it also has its own capacitance and that capacitance is part of the circuit ok.

So, that capacitance of this source also has an effect, next another phenomena again this is another parasitic phenomena that can happen. And so, let us understand this parasitic phenomena again it has effect on how we design the gate driver resistance?

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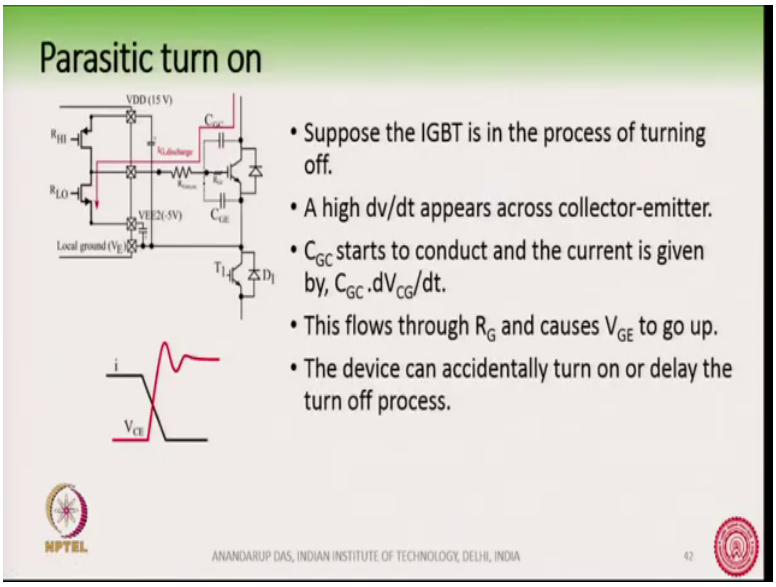

So, suppose these IGBT here is in the process of turning off, let us assume like that, it is in the process of turning off then what is happening because this is in the process of turning off. So, this voltage the, this voltage here is going to the blocking voltage it is rising up to the blocking voltage and hence a high dv dt will, will appear across the collector emitter. And so, this high dv dt and there is a capacitance here and this high dv dt on this terminal along with this capacitor it will cause a current to flow ok.

So, if and what is the current flowing CGC times d V CG d t, this is the current which will flow through this here. Now, this current will flow through the R gate off or it is a parallel combination of R gate on and R gate off, RG on and RG off it will flow through this together if it flows through that resistance then this points potential, the gate potential will increase and therefore, V G E voltage will go up because this is flowing through this RG here.

So, this points potential will increase. So, when the device is in the process of turning off, where we are reducing the value of V G E, now we are getting a situation where because of this parasitic the gate emitter voltage is actually rising up.

So, it can have two impacts it can delay the turn off process or it can even accidentally turn on a device which has been almost on the verge of turning off. So, this is something which is also a very important effect and has to be taken care of.

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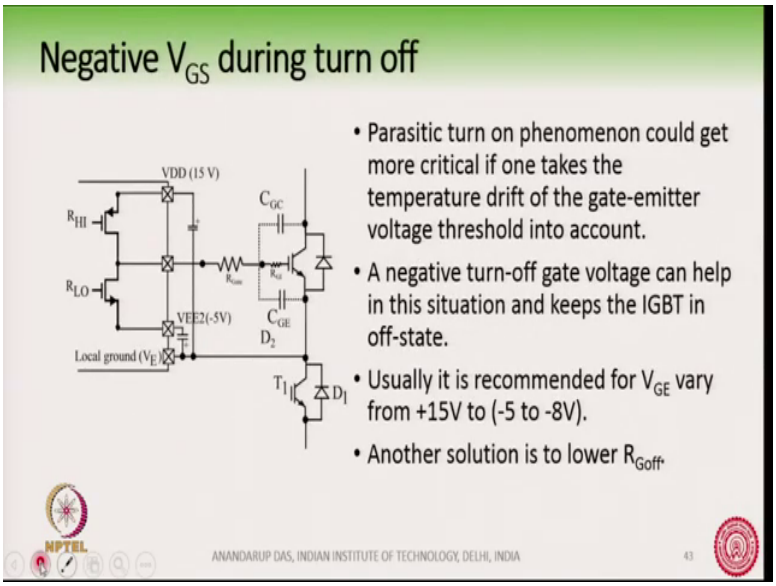

Now, how will you take care of this one?

Of course, you can take care of by decreasing the value of R gate here ok, if you reduce the value of this RG during this. So, if you reduce the value of RG, then this effect can be reduced again you see that it is a compromise if you reduce the value of RG; then you will

have somewhere else a problem coming up as we had earlier discussed. So, the gate driver selection is always a tradeoff between different aspects.