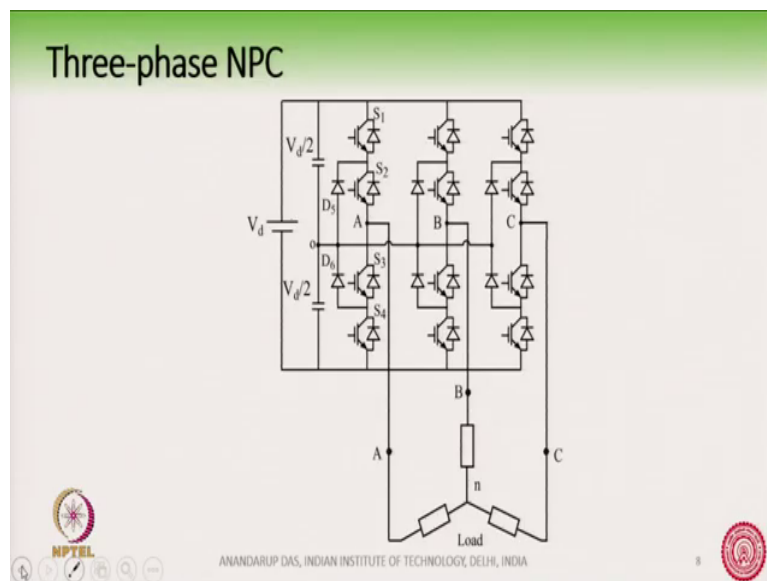


High Power Multilevel Converters – Analysis, Design and Operational Issues
Dr. Anandarup Das
Department of Electrical Engineering
Indian Institute of Technology, Delhi

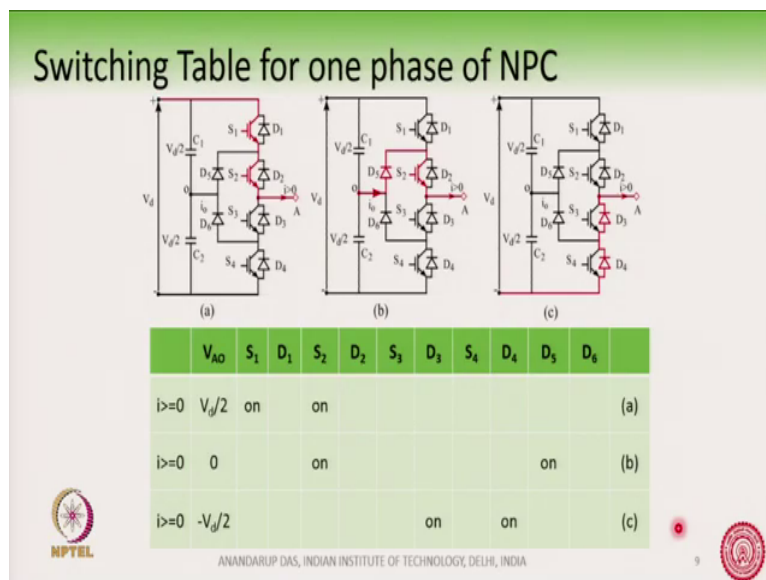
Lecture - 27
Neutral Point Clamped Converter- Circuit Topology (Part II)

(Refer Slide Time: 00:17)



So, this is the three phase NPC circuit and let us now understand the operation of this circuit in details. In order to understand the operation of the circuit in details, we take only one phase of the converter and analyze it in details. So that, we can also understand the other phases, other phases are identical in operation.

(Refer Slide Time: 00:35)



So, we have taken here one phase. So, first of all let me clarify this is a DC bus voltage which actually is split into two parts using this capacitor ok. So, the midpoint of this two capacitor is what is being accessed by the converter. So, there are no two separate DC sources, but the dc source is split into two parts using two capacitors and the midpoint.

Now how does this converter operate? So, let us first take the case when the current i is going out through the terminal A, let us take this case first. When the current is going outside out of this converter and we would like to get a voltage V_d by 2 the voltage V_{AO} , the voltage the pole voltage V_{AO} . So, everything is now accessed with respect to the point O which is assumed to be at 0 potential.

So, V_{AO} , the voltage is equal to V_d by 2 and the two transistors S_1 and S_2 are conducting. And then, we get V_d by 2 voltage at point O with respect to point O point A with respect to

point O as you can see here V_A is equal to $V_d/2$, the S 1 and S 2 are on ok. And, these are the two devices conducting for the current going out of the terminal A ok.

Now when we want to get a 0 voltage, what happens? When we want to get the 0 voltage, we turn off the pulse to S 1 ok. While keeping the both the pulses for S 2 and S 3 on so, let me clarify it that if I want to get the 0 voltage and the current is also going outside, what can be the possible path of the current? The possible path of the current can be like this, D 5 and S 2 and going out like this. So, this is the possible path of the current, if the current assumes this direction and assuming that if there is no drop on D 5 and S 2, that is; these two devices are identical, this means; point A here will be shorted to point O and so, we will get a 0 voltage ok.

So, therefore, in order to get 0 voltage what we can do for a positive direction of current as shown, what we can do is the switch S 1 has turned off and S 2 can be kept on. When the transition is happening from this to this S 2 can be kept on and then the current will flow like this here and we will get a 0 voltage ok. If we want to get the negative voltage, then what we will do? Suppose, the current direction is positive and going out here. We will give pulses to S 3 and S 4 together ok and withdrawing pulses from S 1 and S 2 ok.

If we give pulses to S 3 and S 4 then the two diodes, D 3 and D 4 will start to conduct here because, the current direction is as shown. The current is controlling the direction of the current is actually controlling which devices are turning on at a particular instant. So, in spite of giving the gate pulses to S 3 and S 4 the diodes D 3 and D 4 will conduct. And, the pole voltage a with respect point O will be minus $V_d/2$ because the diodes are ideal.

So, this will be minus $V_d/2$ and so, this is that third row in the table. Minus $V_d/2$ diodes, D 3 and D 4 will turn on in spite of the fact that S 3 and S 4 are given pulses ok. Let us see, what happens when I is less than 0? This is shown in this figure.

(Refer Slide Time: 06:16)

Switching Table for one phase of NPC

	V_{AO}	S_1	D_1	S_2	D_2	S_3	D_3	S_4	D_4	D_5	D_6	
$i < 0$	$V_d/2$		on		on							(d)
$i < 0$	0					on					on	(e)
$i < 0$	$-V_d/2$					on		on				(f)

ANANDARUP DAS, INDIAN INSTITUTE OF TECHNOLOGY, DELHI, INDIA

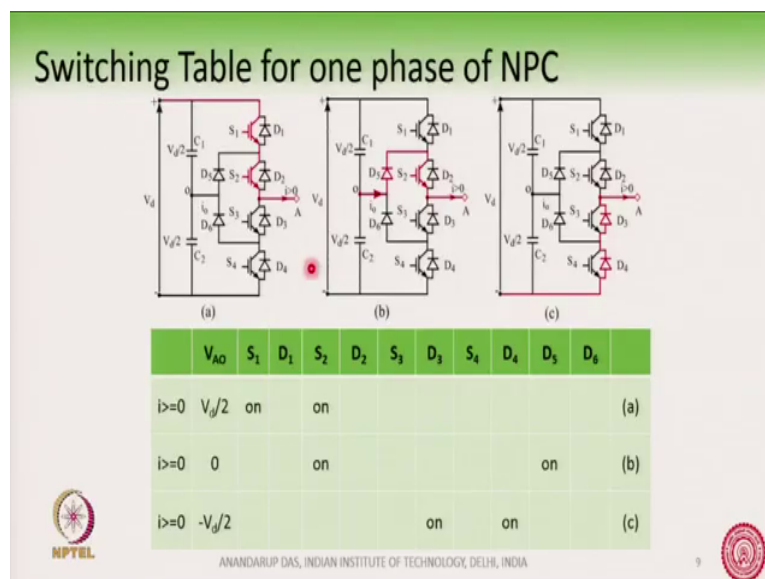
Now, when I is flowing into the converter like we have shown. Suppose, we want to get $V_d/2$ voltage. So, we would like to have so, what is our aim here? We would like to have $V_d/2$ and $-V_d/2$ these three levels of voltages between point A and O. This is what we design and the current through point O should be bidirectional in nature. It is an AC current ok. It can be going out to the a terminal or it can flow inside the a terminal.

So, suppose, the current is now flowing inside to the converter and during that time if I want to have the plus voltage on point A, plus $V_d/2$ on A with respect to point O then what I will do? I will give pulses to S_1 and S_2 . But since the current is going inside what will happen is the diodes, D_1 and D_2 will start to conduct ok. And therefore, I will get since the diodes are ideal I will get V_{AO} voltage to be plus $V_d/2$ it is shown on this row here.

Now, comes the condition this is tricky, now comes the condition 0 voltage. Suppose, the current is going in and I want to get 0 voltage V_{AO} , what will I do? What is actually the path of the current? The path of the current is so, I will turn on S_3 and the path of the current will be something like this. Here, it will come in like this go through this transistor and go through the diode and come to the point O ok. So, during this point of time I will get 0 voltage V_{AO} with the switches S_3 and D_6 conducting. So, that is what it is shown here S_3 and D_6 are on in this table.

Again, if I want to get the negative voltage then, I will turn on S_3 and S_4 , I will give pulses to it and then the current will flow like this. The current is inside and it will flow through the two transistors S_3 and S_4 as shown in the table. So, summarizing what we can say? We can say that, if I want to get the voltage V_{AO} to be V_d by 2 ok.

(Refer Slide Time: 09:47)



Give pulses to S 1 and S 2 ok, means; comparing this figure with along with this figure, I can say that if I want to get V_{AO} voltage to be equal to V_d by 2 then give positive gate pulses to S 1 and S 2 ok. Do not give pulses to other switches. If the current direction is positive, then S 1 and S 2 will flow will conduct where as if current direction is negative then D 1 and D 2 will conduct.

So, the current will decide which devices will conduct. So, we will just give the pulses to S 1 and S 2 ok. Now next case when we want to get the 0 voltage, V_{AO} is 0, what will we do? What shall we do? We will give pulses to S 2 and S 3. We will give pulses to S 2 and S 3. You can compare this figure with also with this figure ok. I will give pulses to S 2 and S 3 withdrawing the pulses to other switches.

Now, if the current direction is positive, then it will automatically make sure that D 5 and S 2 are conducting ok. D 5 and S 2 are conducting. Whereas, if the current direction is negative, it will automatically be ensured that S 3 and D 6 are conducting ok, S 3 and D 6 are conducting. Because so, when we want to access the 0 voltage, we just give the pulses to S 2 and S 3 simultaneously together. Depending on the direction of the current, either S 2 will conduct or S 3 conduct and along with either D 5 or D 6, the clamping diodes.

So, one of them will be conducting depending on the direction of the current. In both these cases we will get 0 voltage. And similarly, if I want to have V_{AO} as minus V_d by 2, what we will do? We will turn on S 3 and S 4 or we will give pulses to S 3 and S 4 ok. And so, if the direction of current is negative then these two devices or the two transistor will be conducting. Whereas, if the current is in the positive direction, then the two diodes will be conducting ok.

So, the, we understand that in this converter all these four IGBT s or transistors or MOSFETs if you use MOSFETs, all these will be useful all these four transistors as well as the four diodes are useful and together with D 5 and D 6. So, under different conditions of operation some switches one or more switches will be conducting and you should be able to fully understand under what condition, which device will turn on ok.

So, another thing that I forgot to mention previously is like where do we use neutral point clamp converters because as I was discussing the IGBTs uh. So, it came up in the mind that neutral point clamp converters again it is a multilevel converters typically used in their kilo volt range and mega watt hundreds of kilowatts to mega watt power range.

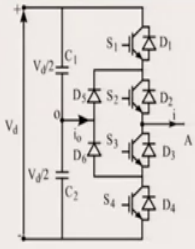
So, 11 kilo volt they can be used something like that, but not probably not at the high voltage DC transmission at hundreds of kilo volts, this is not the most recommended converter. So, neutral point clamp converters are highly used in grid connected applications as well as motor drive applications ok. It is probably, it is the most popular multilevel converter topology ok. But, usually it is all limited to three level we see that there are 3 levels of 3 levels are possible from NPC although people have proposed 5 levels 7 levels like that, but it is not so popular.

We will see that why it is not so popular. So, this is what the converter operation is and this is shown for A phase and we can also do the same thing with the B phase and the C phase ok. So, this is a straight forward. So, this is what we are summarizing here. And we see that based on the table which we have shown we can see that in this converter S 1 is S 3 compliment and S 2 is S 4 compliment. So, these two switches S 1 and S 3 are given complimentary switching or complimentary pulses. Whereas, S 2 and S 4 are given complimentary pulses ok. You can also understand in a slightly different fashion like if you give see you need S 1 and S 2 to be turned on.

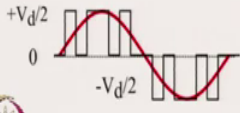
So, as to get the $V_d/2$ voltage. So, S 1 and S 2 cannot be made complimentary. So, they are the same means in order to access the V_{AO} equal to $V_d/2$. I need S 1 and S 2 to be turned on. I cannot make S 1, S 2, S 3, S 4, all four of them turned on at the same time right, then it will short the whole DC bus. I cannot also make S 1, S 2, S 3 to be turned on the same time ok. If I turn on S 1, S 2, S 3 at the same time then what will happen is this way the DC bus will be shorted in this path here ok.

(Refer Slide Time: 17:03)

Switching Table for one phase of NPC



- $S_1 = \overline{S_3}$ and $S_2 = \overline{S_4}$
- $V_d/2$: pulses to S_1 & S_2
0: pulses to S_2 & S_3
- $-V_d/2$: pulses to S_3 & S_4
- During 0 voltage, pulses are given to both S_2 & S_3 but as per direction of current one switch between these two will conduct.
- It is possible to go from $+V_d/2$ to $-V_d/2$ directly but this increases the instantaneous error so this is forbidden.



ANANDARUP DAS, INDIAN INSTITUTE OF TECHNOLOGY, DELHI, INDIA

So, in order to prevent that I must turn off S 3 when I am turning on S 1 ok. This can be obtained from the table given in the previous slides, but you can also see that how can we obtain these like, if you see observe this converter S 1, S 2, S 3, S 4, you cannot turn on all of them simultaneously ok. So, then you will short this DC bus. Now if I want to get the positive voltage; I of course, will turn on S 1 and S 2 simultaneously ok. So, S 1 and S 2 cannot be made complimentary. On the other hand, if you see that if I turn on S 1 S 2 S 3 at the same time ok, then what will happen is I will have a path like this; S 1, S 2, S 3 like this here.

So I will short this DC bus. So, I cannot turn on S 1, S 2, S 3 at the same time right. So, therefore, I have to turn off S 3 when I am turning on S 1 and that is how S 1 and S 3 becomes complimentary and on a similar logic we can also find out that S 2 and S 4 are complimentary ok. So, these two switches are always given complimentary gate pulses. So, if I give a turn on signal for this one, I must give a turn off signal for S 3. And S 2 and S 4 are

again given complimentary signals ok. So, this is what is also kind of like a summary. So, if I want to get $V_d/2$ voltage give pulses to S 1 and S 2, give turn on pulses or high pulses to S 1 and S 2 ok.

Again, depending on the direction of the current, either S 1, S 2 will conduct or D 1, D 2 will conduct ok. If I want to get 0 voltage between V AO give high pulses to S 2 and S 3 ok. And then if the current direction is positive D 5 and S 2 will conduct if the current direction is negative S 3 and D 6 will conduct like this. If I want to get minus $V_d/2$ voltage give a high pulse to S 3 and S 4 ok. And then i is positive means; D 3 and D 4 will conduct, i is negative means; this way it will conduct ok.

And under all operating conditions we maintain that S 1 is complimentary to S 3, S 2 is complimentary to S 4. Now it is also possible in this converter to go from plus $V_d/2$ to minus $V_d/2$ ok. If you see here the V AO voltage, we have switched between 0 and $V_d/2$ here and then again 0 and minus $V_d/2$ here. But it is actually you can also go from plus $V_d/2$ to minus $V_d/2$ directly, like from here to this state here ok.

So, you are turning on S 1 and S 2 and immediately, you flip it to S 3 and S 4. However, this operation is not done ok. It is primarily, this operation is avoided. We always go from plus $V_d/2$ to minus $V_d/2$ through a 0 level ok. Why? Because the main reason is the dv/dt is very high in this plus $V_d/2$ to minus $V_d/2$ case. So, no this is not fully correct so, I will write it in not like this. It increases the dv/dt because, when the voltage goes from plus $V_d/2$ to minus $V_d/2$ directly then the whole DC bus, the total DC bus is the dv is the total DC bus.

And so, the dv/dt can be enormously high and that is detrimental to the operation of the converter or the operation of the suppose the motor drive which is connected. So, we in case of a neutral point clamp converter, we always go from plus V_d to minus V_d through 0. So, when we switch it, we go from plus $V_d/2$ to 0 and to minus $V_d/2$ usually. Always it is like this or when it is going from minus $V_d/2$ to plus $V_d/2$, it goes through a 0 state otherwise the dv/dt can be very high.

Remember, this is a multilevel converter and so, the voltage can be the DC bus voltage can be quite high. And so, the dv/dt can also be quite high for such a converter.