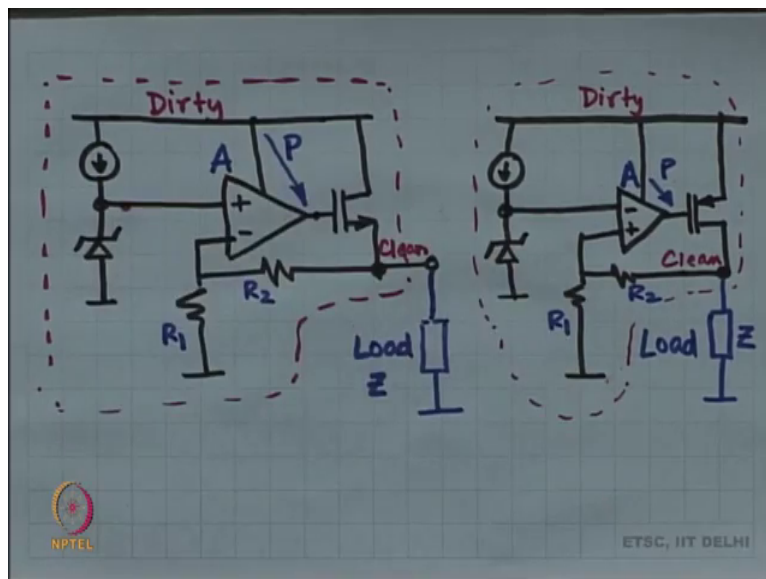


Analog Electronic Circuits
Prof. Shouribrata Chatterjee
Department of Electrical Engineering
Indian Institute of Technology, Delhi

Lecture 40
Voltage regulators - line, load; conclusion regulation

Welcome back to Analog Electronics and today is lecture 40. This is pretty much going to be the last lecture of the course. Today we are going to discuss Voltage regulators. We were discussing voltage regulators in the last class as well and we saw two separate topologies of voltage regulators. Today we are going to further that discussion. We are going to discuss line and load regulation specifically and then, finally we are going to conclude the course.

(Refer Slide Time: 00:59)



So, in the last class we saw two separate topologies; one is I have a voltage reference and then, so this was topology number 1. This load is outside the circuit, this is the dirty supply and this is the clean supply. This was one topology that we saw and then we saw a second topology which is very similar, but uses a common source amplifier at the output as opposed to common drain, right and once again this is dirty, this is clean.

So, the first one is the classical voltage regulator and the second one is called a low dropout voltage regulator or in short an LDO. So, the first one is not an LDO. It is the voltage regulator, the classic one. Second is an LDO. These were the two topologies we

saw yesterday and we were discussing drawbacks of each as oppose to the other and what I want to do is first, I want to investigate a numerical verification of what is line and load regulation of each of these, alright. So, this is my plan number 1.

So, let us decide on a few things. Let us say this is R_2 R_1 . Let us say this is Z , ok. R_2 R_1 Z and then, we will use the standard parameters of this MOSFET in both cases, right. The standard parameters would be G_{MRDS} or G_{DS} whatever you want, right. I am not going to worry, bother about body effect, right now, let us keep that aside.

Then, we have a 3rd set for the op-amp. Let us assume that the op-amp has a gain of A ok, gain of A and let us assume that op-amp has a PSR. That is a second gain from the dirty power supply to the output small signal gain, from the dirty power supply to this point, right.

What do you want to call this? Let us call it P , capital P . So, P is the small signal gain between the dirty power supply and the output of the op-amp, alright and it is P , no matter which orientation you connect the op-amp because it is not connected to any of the plus and minus terminal. So, it does not matter which terminal whether the op-amp is this way or the other way, it is P in both cases. So, this is what I have.

Now, what we are going to do is we are going do we are going to try and find out two different things. One is I am going to apply a small signal at the power supply, ok. I am going to apply a small signal at the power supply and see how much of that signal comes out at the clean end. Small signal will be applied at the dirty end and we will see how much dirt comes out on the clean side, ok, for both of these.

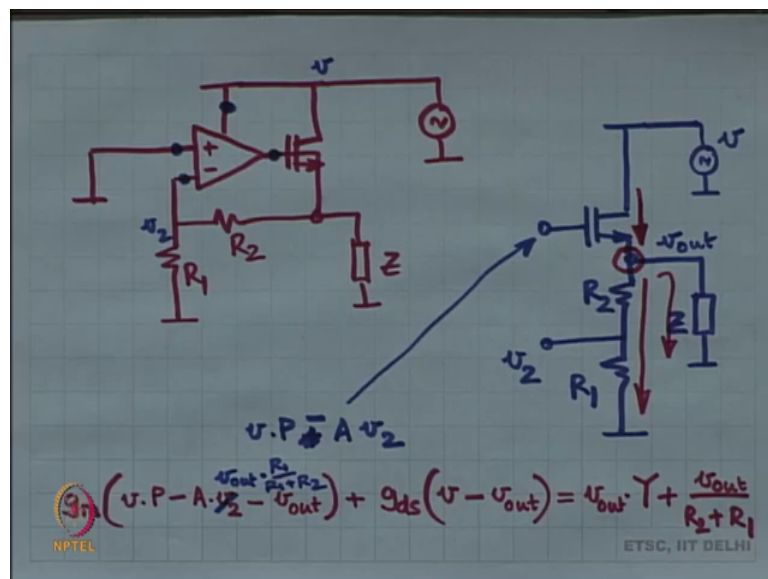
This is experiment number 1 and experiment number 2 is we are going to change the value of Z , alright. We are going to change the value of Z and measure how much clean power supply is varying, ok. Of course, to do this it is very easy. It is not very hard at all. All we have to figure out is what is the Thevenin equivalent of the entire block.

So, in other words for the second experiment, for the second experiment, we are going to work out the Thevenin equivalent of this entire block, that is Thevenin equivalent will have open circuit voltage and output impedance. We will work out the open circuit voltage output impedance of the entire block and see how much you know if I make a change in Z , how much does the voltage change. So, once you have the Thevenin

equivalent impedance, everything is Thevenin equivalent, everything is ready in front of you. So, we will do it for both of these, ok.

So, 2 and 2, 4 things we have to do. So, let us start from the beginning. Let us first apply a small signal at the dirty supply and see how much comes out at the clean end of the classical voltage regulator. So, this is going to be our first job. So, by the way when I apply a small signal at the dirty supply, what is going to be the change over here at this node? Nothing, no change, why because this is a current source, ok. So, it does not matter what is the small signal impedance of the Zener diode, all of that does not matter. This is a nice clean current source. Of course, you have to make an, it is your job to make a nice clean current source. Once you have made a nice clean current source, this voltage is fixed, ok. No, it is not changing at all. So, this is constant, right. Now, let us draw our small signal diagram.

(Refer Slide Time: 08:38)



Our small signal diagram looks like this. I have applied signal instead of the power supply and this voltage reference input has been grounded because that voltage is not changing. So, in the incremental picture that is fixed, in the small signal picture that is 0, fine. You understand that this op-amp is now going to be represented as two different things. The output voltage of the op-amp is now the sum of A times the difference between plus and minus plus P times the difference between power supply and ground of the op-amp, ok. So, let us look at it this way. Let us simplify. So, this is what I have and

let us say this gate voltage is equal to v times P plus A times minus v_2 , ok. This is V , this one is V_2 . So, the voltage over here is A times, A is the gain of the op-amp A times minus V_2 plus P times the small signal on the power supply V , alright. This is the setup and I am interested into interested in finding out this v out. Of course, V_2 has to be eliminated from the setup, ok. We do not want to keep V_2 in the equation anymore, alright. How will you do it? You will just solve, ok.

So, let us just solve one easy that is that seems like it is the easiest way to look at things, right. We can do one quick KCL at this node, ok. So, a KCL at this node what should be going to give? It is going to give, so you have a current because of g_m times the difference voltage plus a current because of r_{ds} , this is the difference voltage g_m times the difference voltage plus g_{ds} time v minus v out, ok. That is your value of v out, that is that is this current I am sorry fine and then, what is this current and what is this current? This current is nothing but v out divided by R_2 plus R_1 plus v out divided by Z , ok. Any questions? So far everything is fine.

And what is V_2 ? V_2 is just a potential divided version of v out, ok. v out V_2 is R_1 by R_1 plus R_2 times v out and then, the standard way of doing things is to put all the v outs on one side, all the V 's on the other side and then, we find out what is the relationship between v out and V , ok. That is what we are going to do. We are going to put all the v outs on one side.

(Refer Slide Time: 14:54)

$$v_{out} \cdot \left[Y + \frac{1}{R_2 + R_1} + g_{ds} + g_m + g_m \cdot A \cdot \frac{R_1}{R_1 + R_2} \right] = v (g_{ds} + g_m \cdot P)$$

$$\frac{v_{out}}{v} = \frac{g_{ds} + g_m \cdot P}{Y + \frac{1}{R_2 + R_1} + g_{ds} + g_m (1 + A\beta)} \approx \frac{P}{1 + A\beta}$$

$$= \frac{g_{ds}/g_m + P}{Y/g_m + \frac{1}{g_m(R_2 + R_1)} + g_{ds}/g_m + (1 + A\beta)}$$

NPTEL ETSC, IIT DELHI

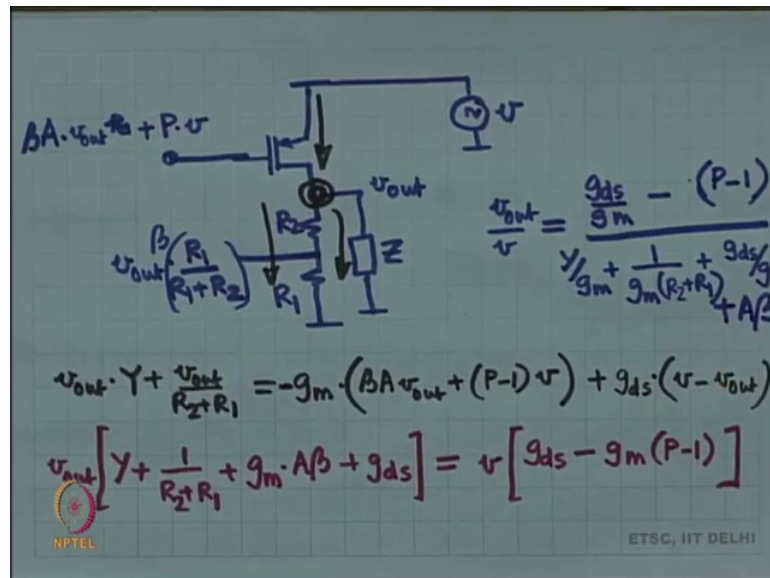
So, v_{out} times Y plus 1 by R_2 plus R_1 plus g_{ds} plus g_m plus g_m into A into R_1 by R_1 plus R_2 . By the way what is this factor R_1 by R_1 plus R_2 ? This is the feedback factor. Remember? This is the feedback factor. This is β . So, this whole thing happens to be equal to β .

So, this is all the v_{out} terms on one side and then, I am going to put, keep all the V 's on the other side. So, v_{out} times g_{ds} plus g_m times P . So, we have put all the v_{out} terms on one side, all the v_{out} terms on the other side and therefore, v_{out} by v_{out} is nothing but g_{ds} plus g_m times P divided by Y plus 1 by R_2 plus R_1 plus g_{ds} plus g_m times 1 plus $A\beta$, alright and the good news is that g_m is hopefully a large quantity number 1. Number 2, A is hopefully a very large quantity. So, g_m times 1 plus $A\beta$ is hopefully to dominate the denominator. In the numerator g_m times P is hopefully going to be the biggest thing, ok. I mean I mean the hope is that g_{ds} is not that significant. If g_{ds} is significant, very good. I mean the P effect is not there, right. It is even better.

If g_{ds} is not significant, if there is effect of P for example, then g_m times P is dominant and then, what is going to happen is that these denominator terms can be thrown out, alright and hopefully these are the only two terms that are significant which means that the rejection, the PSR the power supply rejection of the op-amp P has been attenuated by 1 plus $A\beta$, $A\beta$ being the loop gain, ok; A times β is the loop gain, β is the feedback factor, A is the forward gain, right. 1 plus $A\beta$ is 1 plus the loop gain, alright. This is what we have. So, one possibility is that you approximate this as P by 1 plus $A\beta$, alright. Even if you cannot see that straight away, you can maybe rewrite it as g_{ds} by g_m plus P divided by Y by g_m plus 1 by g_m times R_2 plus R_1 plus g_{ds} by g_m plus 1 plus $A\beta$ and g_{ds} by g_m is hopefully a small number.

So, even if P is substantial, if P is not substantial, you are good, ok. Even if P is substantial, right suppose P is 5, ok. Even if P is 5, that is going to be attenuated, g_{ds} by g_m is of the order of you know one-tenth, one-twentieth, one-fortieth of that order, right. If the device is any good device, then it is going to be something of that order of magnitude. Again g_{ds} by g_m and if Y is large, you win in this case, right. The larger the Y , the better right the denominator becomes bigger, alright. So, this is our classical voltage reference circuit. We are going to do exactly the same thing for the LDO and what is going to happen in the LDO? In case of the LDO, again this is small v , let us do it.

(Refer Slide Time: 20:43)



Now, in case of the LDO, this output voltage of the op-amp is minus A times the voltage over here. No, I am sorry A times the voltage over here plus P times the dirty voltage, A times the feedback voltage plus P times the dirty voltage. So, this is beta. So, it is A beta times v out plus P times small v, ok. This is Z and then, we do the same thing. We are going to do KCL over here. So, v out by v out into Y plus v out by R2 plus R1, that is these two currents, right. The sum of these two currents is equal to this current, and what is that current? That current is g m times v g s gate is over here. Source is at v plus g d s times difference of these two, ok. The g m current always points the other way, right. It always goes from drain to source. We want the current from source to drain. So, there is a implicit minus sign, alright.

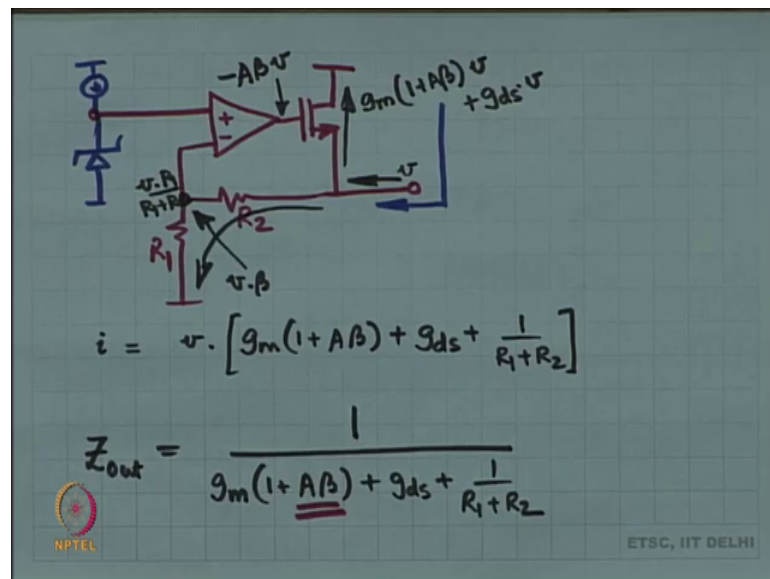
Once again you put all the v outs together, all the v's together. So, I put all the v outs together. Is that ok? It looks reasonable and therefore, I will just do it on the top. I have divided by g m like last time, alright. This is what we have and once again you look at the situation, where P is reasonably large, ok. If P is substantial, then g d s by g m can be thrown out, right you do not worry about g d s by g m. You do not worry about Y by g m all of these terms because A beta is going to be large.

So, your net answer is going to be minus P minus 1 by A beta. In the earlier case, it was P divided by 1 plus A beta. In this case, it is P minus 1 divided by A beta with a negative sign, ok. Now, in the large scheme of things the negative time does not matter, ok.

Whether it is P minus 1 by $A\beta$ or whether it is P by 1 plus $A\beta$, it is all very similar, alright, hopefully in fact, this is smaller, ok. This power supply rejection is hopefully in fact a little better than the earlier one, alright. So, this is as far as the power supply rejection of the circuit is concerned.

Next we are going to do the; so this is the line regulation, alright. How much does it regulate the small signal at the line, the line voltage is the power supply voltage, how much does it regulate at the output. The next is going to be the load regulation and for the load regulation, we are not going to do anything much. We are only going to work out what is the output impedance and if required what is the Thevenin equivalent voltage. Thevenin equivalent voltage does not really matter. It is going to be some value, ok. So, let us think about it a little bit. You have got your reference voltage.

(Refer Slide Time: 27:43)



Reference voltage is being applied and all I am saying is let us find the Thevenin equivalent of this block, ok. You wanted the Zener diode, fine. All that does not matter right, all of these do not come into the picture at all.

So, we are going to find out number 1 is output impedance, number 2 just think about first, the Thevenin equivalent voltage. Suppose, I find out the Thevenin equivalent voltage, it is going to be some value, right. Now, if I twig the load depending on the output volt output impedance, you are going to get a percentage change in that value, right and that is your load regulation. That percentage change is the load regulation. It is

not going to really depend on whether this output voltage is 1 volt, 2 volt, what it is, right. All that you are really worried about is the output impedance. So, let us just find the output impedance.

How do we find the output impedance? You apply a test voltage and see how much current is going in. So, we apply a test voltage v and we are going to measure the current going in. You could also push a current in and measure the voltage. Let us just do it this way. Let us apply a voltage and measure the current. So, if I apply a voltage v over here, then what is going to be a small signal? This is a small signal voltage. If I apply a small signal incremental voltage v over here, what is going to be the incremental voltage here? It is just a potential divider. So, it is going to be v times R_1 by R_1 plus R_2 or in other words, v times beta, beta is the feedback factor, ok. This voltage is steady. The voltage here is v times beta. That means, it is going to get amplified and you are going to get minus A times v times beta, fine.

Now, what is v_{gs} ? v_{gs} is minus A beta times v minus v , alright. So, that means you are going to have a current going upwards. So, first of all there has been current already in this direction, right. There is going to be current going upwards which is of value g_m times 1 plus A beta times v and this is because of the g_m . There is also going to be a portion because of g_{ds} and that is just going to be g_{ds} times v , ok. So, if I apply a voltage v , then I get a current going inside and the value of that current going inside is the sum of these 3 components. One is because of g_m , the other is because of g_{ds} and the third is because of R_1 plus R_2 and therefore, the net output impedance is 1 by this factor. Is it large or small? Small, ok, so, the output impedance of this circuit is very small. Output impedance of just the buffer is approximately 1 by g_m , whereas, the output impedance of this is 1 plus A beta smaller than 1 by g_m , ok

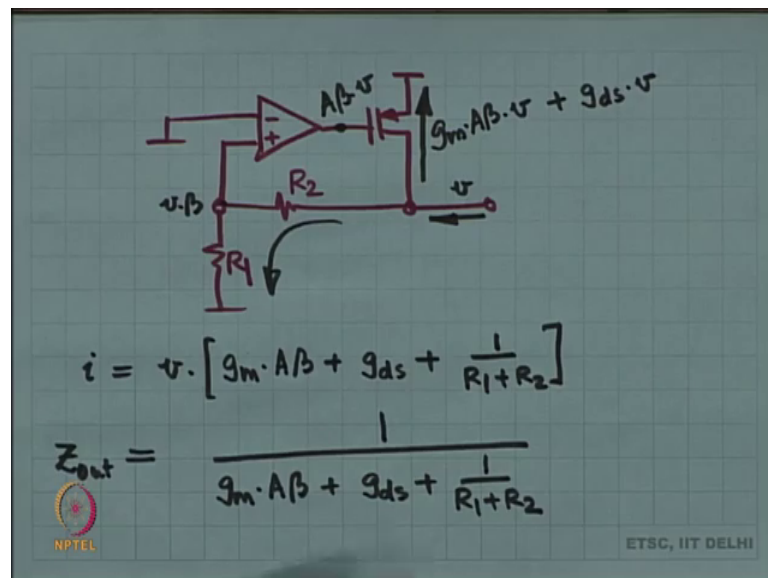
So, you see what the feedback has done. You had a negative feedback circuit. The negative feedback circuit has improved the output impedance of the circuit. It knew that you wanted to make a voltage source, ok. It is almost as if you knew it knew the circuit the feedback circuit knew that you wanted to make a voltage source over here and it made your job better, right. The negative feedback improved the quality of your voltage source by decreasing the output impedance. So, this is what always happens. So, we did not study negative feedback specifically, but whenever you apply negative feedback, you are going to be applying negative feedback to do either make a current source or to make

a voltage source, ok. If you are not really trying to make either of these, then you are you probably do not know what you are doing. So, be careful.

So, you should either attempt making a current source controlled voltage, controlled current source, current controlled current source, some sort of current source or you should attempt making a voltage source. If you attempt making a voltage source, then you will find that the output impedance of your circuit is going to decrease by a factor 1 plus A beta approximately. If you are trying to make a current source, then magically negative feedback will increase the output impedance by a factor of 1 plus A beta, ok. Everywhere this 1 plus A beta factor comes out because it is 1 plus the loop gain. A beta is the loop gain, ok.

So, we have not really invested much time in studying negative feedback, but this is generally the action of negative feedback, ok. So, this is what happens in the classical voltage reference circuit and then, quickly let us workout what happens in the LDO. In the LDO, the circuit is similar.

(Refer Slide Time: 34:57)



So, this is all that we are looking at and once again let us apply a voltage v and measure the current going inside. First of all you are going to have current in this path v by R_2 plus R_1 . That is going to create a voltage over here which is v times βR_1 by R_1 plus R_2 . That is going to create A times v times β at the output of the op-amp and now, your gate to source voltage is $A \beta$ times v minus 0, which means that you are going to

get a current over here a value $g_m \times A \beta \times v$ plus this some more because of g_{ds} , $g_{ds} \times V$.

So, the net current is the sum of these 3 components and the output impedance is 1 by of that, alright. So, what do you see? What is the difference between the earlier one and this one? The output impedance is also pretty much the same, right. The expressions look very similar. They are just about the same. So, if I use the same values of A and the same MOSFET, then you get pretty much the same performance whether you are trying to make an LDO or whether you are trying to make a classical voltage regulator, the performance is going to be similar.

So, what is the hiccup then? The hiccup is that now you are making a three stage amplifier. So, you have to start breaking your head with how to stabilize the system because it in feedback. So, there going to be 3 poles and a lot of people stop the exercise right there and say that let us make a one stage op-amp that is let us decrease the value of A , right. Let us settle for less of performance in terms of A , right. Look, it is a tradeoff. You want better efficiency; you have to do something, ok.

You have to decrease performance. So, you decrease performance in terms of the value of A , right because you can afford only one stage inside this and then, either you compensate like this across the PMOS or you can do dominant pole compensation and put a gigantic capacitor on the load. So, actually both are invoke, right. Putting a large dominant pole capacitor is actually the most common practice because typical loads have large capacitors along with them. So, this is what is normally done in terms of the LDO.

Now, we are going to stop our discussions over here and then, I would like to conclude the course, but before I conclude the course, I would like to emphasize that in no way in this course to be considered as a complete course, ok. Given the amount of time, we can only cover so much, ok. There is a lot more to learn, right, analog circuits has a lot more to offer.

So, what are the different things that we could not teach or could not learn in this course? Number 1: In terms of voltage regulators because let us you know do voltage regulator is the most recent in memory. So, in terms of voltage regulators modern practice or normal practice is instead of having a voltage regulator regulate and supply voltages in different

domains on a chip, normally what you are going to do is you are going to have a big DC converter, ok.

So, this is you think it is power electronics. It is not necessarily power electronics; it is also analogue circuits. So, you are going to use something called DC to DC converter which is the switching switched converter ok. Switching mode, switched mode, buck converter, boost converter, all of these are analog circuits. So, you are going to make a buck converter and convert 3.3 volts to 1.8 volts, then you are going to use a voltage regulator between 1.8 volts and 1.5 volts and you are going to deliver 1.5 volts to the chip, right. This is what is normally done. You are not going to use 3.3 volts and have a voltage regulator to generate 1.5 volts. Distribute 1.5 volts on the chip. Why? Because this is a large head room. So, the efficiency is going to be very poor.

DC to DC converters use inductors and capacitors; inductors are lossless, capacitors are lossless and they use switches. Switches are also we saw in power amplifiers. Switches are lossless, right and therefore, theoretically at least DC DC converters have an efficiency of 100 percent theoretically, right. In practice you are not going to get 100 percent. You are going to get 90 percent, but you see the point. The point is that only if the theoretical efficiency is high, will the practical efficiency be high. So, this is what is normally done. We could not cover DC DC converters in this course, right.

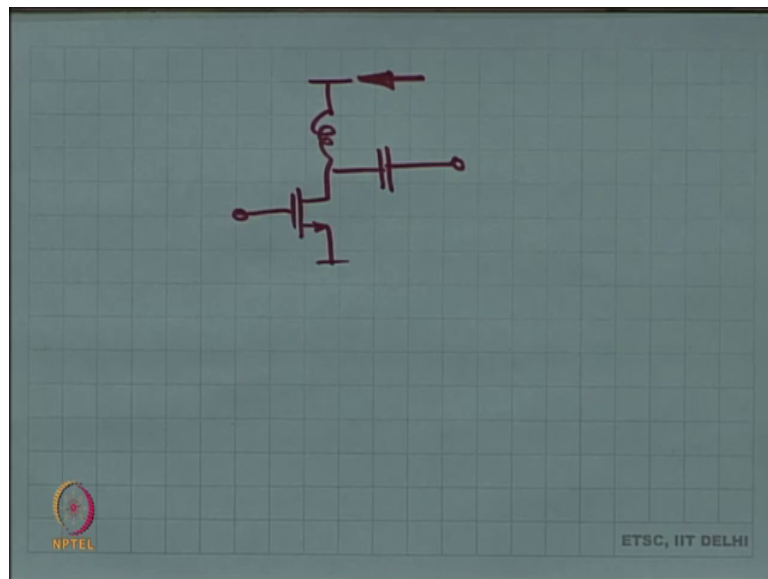
Then there are before these voltage regulators, what did we study? We studied power amplifiers, right. We took an, we did an overview of the power amplifiers class A, class B, right class C, linear and switching power amplifiers. We did not really get into the depth, we did not really look at what happens how you actually go ahead and design a power amplifier. So, whatever we did in the 3 lectures or 4 lectures on power amplifiers was more of an overview of power amplifiers, a lot of modern research, right.

The last 5 years, I would not say 5 years. Let us say 7 years of work in analogue circuits has completely changed the landscape of power amplifiers. Today or rather in this course, we saw power amplifiers is the one transistor device, the one transistor circuit with some you know passives, right. Modern power amplifiers do not look like that at all, right. A modern power amplifier, if you buy a modern power amplifier IC, it is going to have more than 1 million transistors which include a computer and a DSP. What are

they going to do, what is all this for? They are going to change the value of the power supply itself, right.

Suppose you want to work at class A always, ok. You are very worried about distortion linearity. So, you want to work in class A mode, right. What a modern power amplifier is going to do is it is going to change the value of the power supply voltage; it is going to track the envelope of the signal such that you get maximum efficiency. Your efficiency is going to be much more than 50 percent and you know class B, class C, correspondingly. Class B is actually very popular right but what you are going to do is, you are going to track the power supply voltage, itself. How will you make this power supply voltage? Using DC converter, ok a lossless switching DC DC converter is going to be used to generate the power supply voltage of the power amplifier, ok. So, we are talking about this, right.

(Refer Slide Time: 43:54)



This was our power amplifier circuit class A, class B, whatever class you want. Now, what they are going to do is a modern power amplifier is going to do is it is going to change the value of the power supply itself, such that you get maximum efficiency. They are not this voltage is no longer going to be a static one, ok. In fact, this inductor is going to be replaced with a current source or another MOSFET basically, alright and then, how will you generate that power supply voltage? Using a DC DC converter. How will you

clock the DC DC converter? Using pulse width modulation. How will you generate those pulses? Using digital signal processing, using a huge DSP, right.

So, analog circuits today have become extremely complex, alright and all these innovations, these innovations are all from the last 10 years. So, these are called Envelope Tracking Power Amplifiers. Then, there are polar power amplifiers which actually just set the right value, right. Suppose, you want to send a magnitude in a phase, then imagine setting the magnitude with the power supply and with the phase from class D amplifier, this is working in class D mode. The phase is through a clock over here, right. The magnitude is coming from the power supply, ok. So, whatever vector you want to send which has a magnitude in a phase can be set like this, right. Lot of innovation has happened in the power amplifier front.

Then, before that we studied op-amps. Our discussion on op-amps was also somewhat incomplete. We did not really discuss for example compensation of a fully differential op-amp. We did not discuss fully differential op-amps completely in fact. So, when you have a fully differential op-amp, you need certain structures like common mode feedback to stabilize the value of the common mode voltage. We did not discuss these things. So, I am just pointing out where all are the holes, right in our lectures, where are the holes. So, these holes please try to fill by yourself, right. I would encourage you to fill these holes up by yourself because these are all very interesting areas, right and a lot of work has happened in all of these.

When we were talking about voltage regulators, one more thing that we did not cover was that Zener diode, right. In modern circuits you do not use a Zener diode. You are actually going to make a voltage reference, a reference voltage that is stable with temperature. We have not managed to discuss that at all. We have not managed to discuss feedback in detail, right. Feedback we have done it you know over here. We have seen illustrations of feedback which we have solved by hand. We have not really used the shortcuts of you know the intuition, that feedback offers a lot of times.

So, we have not discussed feedback, we have not discussed voltage regulators, power amplifiers, we did not discuss in great detail, DC DC converters we did not discuss, lot of these things, lot of lacuna are there in the course, but we still managed to cover a lot of

fronts. We managed to cover op-amps substantially, right single ended op-amps using MOSFETS, we managed to cover it substantially.

We worked on current sources, current mirrors, biasing. I think we did quite a lot of work with biasing, cascode current mirrors, ordinary current mirrors all of this we have studied. We have studied op-amps in great detail all the way till compensation, fully completely justifying why we are doing each and every step, dominant pole compensation as well as miller compensation, right, compensation for the cascode op-amp, compensation for two-stage op-amps, right. We have studied all of them all of those in quite a good detail and the remaining parts I encourage whatever is the lacuna in the course, I strongly encourage that you read these up. These are these can benefit you in many ways, alright.

Thank you. Thanks for attending the course.