Analog Electronics
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Lecture – 33
Op-amp design with compensation

Welcome to Analog Electronics. Today is the 33rd lecture, and we are going to talk about Op-Amp design along with compensation. So, this is going to be a kind of an example of a summarisation of all the stuff that we have learnt so far. So, pretty much the culmination of all of the things that we have learnt, right we started with the objective of being able to design an Op-Amp. And today we are going to give a demonstration of that, ok. So, first if you are planning to make an Op-Amp, then you need DC gain, right your objectives are DC gain.

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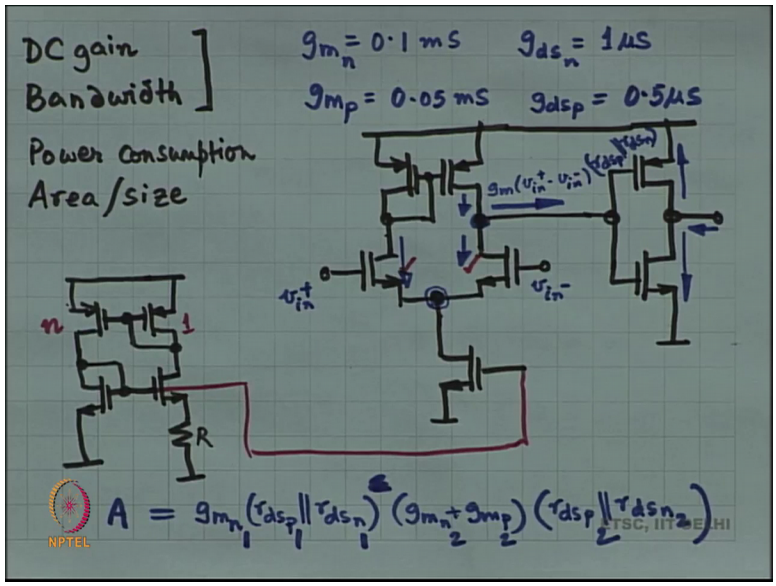

You have a second objective and that is bandwidth, ok. These are your primary objectives. Your constraints are of course, power consumption, right this is one of the important constraints.

The other there is one more important constraint which you have not seen so far, and that is area or size, ok. Especially when we are talking about electronic circuits, that will go and an integrated circuit, the size of the device it matters, because size is directly proportional to how expensive the circuit is going to be. So, you want to make things

cheap, one of the goals of engineering is to make your electronics cheaper right. So, in that sense, you need to be able to conserve on the size, size directly relates to the size of the capacitor, capacitor is a epsilon by d right. So, size of the capacitor, sizes of the individual devices. So, all of these finally relate to size.

We are not really going to focus that much on area and size right now, but this is usually one of the constraints if you are employed in the industry, then you will find that area is something that people are worried about all the time, fine. So, we are planning to make our Op-Amp, and there are 2 constraints important objectives one is DC gain the other is bandwidth, and we have a constraint on power consumption, all right. What is going to be the structure of our Op-Amp? You probably will have let us take one of the simplest cases. It is let us start with a differential pair, this is the input structure a differential pair. And usually when you have a differential pair you are you will have to have a tail current source ok.

The differential pair will have to drive a load as well. And this load is typically going to be made up of p mosses, not resistors, all right. And supposing you are thinking of a single output, differential input single ended output Op-Amp, then this load could also be in the most simple case in one of the simpler cases, it could be an active current mirror, right. Self-biased active load amplifier, differential amplifier ok.

We could have something like this in one of the simpler situations. In this case, the output of this amplifier comes out of this particular load. And typically you are not going to get enough gain. Suppose your gain requirement is 1000 all right. You are not going to get enough gain; you are not going to get 1000 DC gain from the first stage itself. The first stage will probably give you a differential gain of 40 ok in which case you need yet another stage of amplification.

Now the second stage of amplification if the first stage is giving your single ended output, right the second stage of amplification does not have to be differential anymore, all right. So, in such a scenario you could have either just one common source amplifier or you could even have a common source amplifier with a common source amplifier as a load.

So, one popular structure is something like this, ok. The n mos common source amplifier has a load which is a p mos common source amplifier, right. The p mos common source

amplifier has a load which is an n mos common source amplifier. All right this actually works quite well this is called the C mos inverter, this is this actually a very popular digital circuit the C mos inverter not gate ok. The not gate also happens to be a common source amplifier right. P mos common source amplifier n mos also is a common source amplifier ok. So, this is the structure, we have one loose end over here, this particular node is not really biased, right. This needs to be biased out of some constant g m biasing circuit ok.

Typically, that is how it is going to be done; you are going to make a constant g m biasing circuit. What is that look like? Something like this ok. There are there are more sophisticated constant g m biasing circuits as well, right. You could even have cascade current mirrors; all kinds of sophistications could be brought into this constant g m biasing circuit depending on how constant you need the g m to be, all right. Something like this, right you will have some ratios of this w by ls ok. Remember to check this circuit once more for your own benefit right. This is actually a very useful, small little circuit. And the result is going to be the result of this is going to be that the g m of these 2 devices is going to be related proportional to 1 by R, ok.

It is going to be related to R and the value n ok 1 by R and something to do with n ok. I think square root of 1 by n minus 1 or something I forgotten what it is, or 1 minus 1 by n something like that. It does not matter, it is a constant number right; which is related to n and R 1 by R. So, the g m of the input differential pair is suddenly proportional to 1 by R. So, that is the magic of this all right. This is now my overall structure ok now supposing let us throwing some numbers over here. So, let us say g m of all the n mos devices after doing this constant g m biasing circuit. Let us say g m of all the n mos devices is 0.1 millisiemens all right. And R o of all the n mos devices suppose it is or rather g o g ds.

Suppose that is equal to 1 microsiemens fine. And at the same time for the same size of the mosfet, suppose the p mos will have a g m, and correspondingly g ds is 0.5 microsiemens ok. For the same size of the n mos. Typically what is going to happen is, that you want to keep these 2 of similar order of magnitude, not really necessary, but you can do that, ok. For example, over here it is not really required whereas, over here it is going to be required ok. Because this is a C mos inverter, you want the g ms to be equal

the g d ss to be equal, all right. Otherwise, it is going to be suboptimal. The behaviour of this second circuit is not going to be optimal, all right.

So, this is kind of the structure. I am just trying to motivate an example Op-Amp over here. This might not be the Op-Amp that you finally, end up with, but this is just trying to motivate an example Op-Amp ok. Now how are we going to proceed? What is where is bandwidth coming in number one. So, what about DC gain, as far as the differential mode is concerned, right from what you I hope you remember; is that this first stage, in this first stage this node will somehow act like a virtual ground.

Not really virtual ground, but somehow it so happens that this acts like a virtual ground and double the current comes out over here ok. The way it works is that, this node does not move right, if this is v in minus, this is v in plus; the middle node does not move at all ok. G m times v in plus current comes this way, all right. This current is reflected over here by the current mirror.

So, the top p mos is actually pushing a current g m times v in plus, fine? On the other hand, this n mos is pulling a current g m times v in minus; which means that the current that is pushed out is g m times v in plus minus v in minus. But a current cannot go into a gate ok, you are pushing out the current, it is trying to go into 2 gates, this just does not happen, right. The gates do not draw any current. So, it is going to respond by increasing the voltage over there, right. How is the current going to get converted into voltage? It is going to get converted into voltage with the help of the output impedance at that particular node. So, at that particular node at this node, the output impedance is the impedance of the p mos in shunt with the impedance of the n mos.

So, effectively the voltage over here is going to be g m times v in plus minus v in minus times R o of the r ds of the p mos in parallel with r ds of the n mos. I am assuming once again that this node is not really moving this is like a ground. So, this is this is how you analyse this circuit very fast. So, instead of a current being pushed out, now the voltage over here rises by a value g m times v in plus minus v in minus times the current, which is r ds p in shunt with r ds n all right. And then what happens in the next stage? This is the first stage, first stage is done. In the second stage, I have a voltage which has gone up right, the n mos responds by drawing a current ok.

How much current is it going to draw? It is going to draw g m of n mos times the voltage that has gone up. The p mos also responds by drawing a current, g m of p mos times the voltage that has gone up small signal incremental voltage that has gone up. Net you have a current coming in from outside; which is g m of n mos plus g m of p mos times the amount of voltage that has gone up all right. Now again this is an empty node, current cannot really be drawn. So, therefore, this is going to be multiplied by the output impedance of the circuit, which happens to be r ds of p mos in parallel with r ds of n mos. Net result is going to be this; that my DC gain is going to be g m of n mos times the r ds p parallel r ds n.

This is in the first stage, and in the second stage I have g m of n mos plus g m of p mos times r ds of p in parallel with r ds of m ok. 1 and 2 relate to first stage and second stage ok. Now if these are all equal then you can combine them, if they are not equal then you calculate and figure it out accordingly ok. It is unlikely that they will be equal, g m of the second stage is uncontrolled in this particular circuit, it has nothing to do with the biased current, for example.

So, you cannot really combine the 2, but anyway this is how you figure out the overall gain, ok. Suppose g m is equal for everything, then I have got 0.1 over here, 0.1 plus another 0.1. So, 0.1 times 0.2, right and r ds p in parallel with r ds n is you know r ds n is one mega ohm.

So, r ds p is also going to be one mega ohm. So, this is 500 kilo ohms, this is also 500 kilo ohms right. So, I have got 0.1 millisiemens times 500 kilo ohm will give me a gain of 50, and then I have got 0.2 and 500 kilo ohms that will give me a gain of 100. So, 50 times 100 something like 5000 is what you have computed over here ok. With these numbers with the numbers that I have given you assuming they are all equal. Now let us say you have got this gain of 5000. Then you say that, all right now I need to make sure that my phase margin is 60 degrees.

How are you going to do that? So, what is, how will you work out the phase margin? So, let us simplify the circuit and draw redraw, this circuit this differential circuit with first stage second stage let simplify it and redraw. So, after simplifying and redrawing, basically what am I going to do? I am going to assume that this node is at some ground right I am going to throw in all of this.

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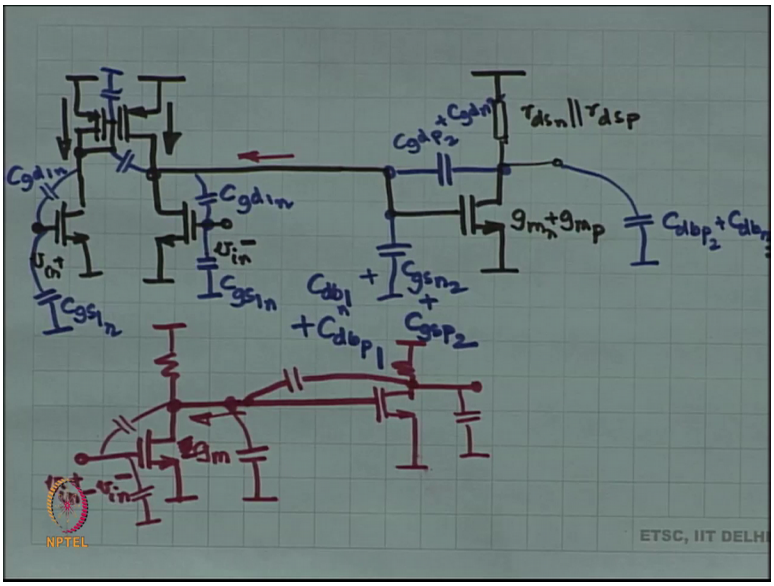

And let us just draw half of it, ok. Something like this, this is the current mirror v in plus is being mirrored, sorry, this g m times v in plus current is going to be mirrored otherwise I just keep everything. And then I have replaced the p mos r ds p and r ds n I have replaced with this rectangle. And I have combined g m n and g m p inside this ok.

And we have to work out the individual capacitances. So, for example, this particular mosfet has both the p mos as well as the n mos inside it, all right. So, when we talk about this capacitance, this should be the sum of C gate to drain of the p mos and C gate to drain of the n mos, ok. Then there is going to be some capacitance over here that is going to be C drain to body of p mos plus C drain to body of n mos, right. Then source to gate to source capacitances will come over here, right this is the second stage is done. Now the first stage, I have drained to body capacitance of the p mos as well as of the n mos, right.

Those capacitances come onto this node, fine. Then what else do I have? I have drained to body of the p mos. I have drained to gate of the p mos as well ok. I have drained to gate, I have source to body which is irrelevant and I have gate to source. Something like this ok, then for the n mos we have gate to source, we have gate to drain, we have source to body which is irrelevant.

Assuming this is at ground already and drain to body we have already accounted for. Similarly, we have capacitance for the other n mos. And for the top corner p mos we

have capacitances gate to source which adds on to this. We have a gate to drain which is shorted out. We have drain to body which gets added on to this right, and source to body which is shorted out. So, nothing extra ok, some things get added on to this particular node fine. So, this is how it is, this is the overall structure all right. Now one possibility is, that we just figure out we need to somehow simplify this, this whole thing right. It is possible to simplify it, all right.

If we can just do something like this, we can say that let us forget about this that entire structure, all that we are going to think of is 2 g m, I am sorry something that looks like this v in plus minus v in minus and g m times that current is posted ok. Remember this current was g m times v in plus minus v in minus ok. So, you can model this entire thing as just one device with a g m all right. And then you need some output impedance over there right the corresponding output impedance of that node, and the corresponding capacitance output capacitance of that node.

And you need some capacitance over here and some capacitance over here. These can be worked out ok. I am not planning to work those out right away, but can be worked out. So, you are going to model, this entire network, by the way all of this is nothing add DC, add small signal increment in the small signal incremental picture this is the ground. Because this does not change with signal, right none of the current voltage is here change with signal. So, therefore, this voltage is fixed with signal which means that this is ground in the small signal. If this is ground in the small signal, then this device behaves like a resistor in the small signal ok.

So, this entire thing is going to be modelled as this one device right. How can you do such a thing? By just estimating the output current, the output trans conductance, short circuit output trans conductance and by estimating the output impedance. So, this is like a gigantic Norton equivalent of the entire first stage ok. That is the plan. Now ones that is done, the second stage I have already modelled right.

This capacitance has to be combined with the other one. And now it looks like my 2 stage cascaded amplifier. And the 2 stage cascaded amplifier we have just learnt how to compensate how do we compensate the 2 stage cascaded amplifier by adding extra capacitance between these 2 nodes, right.

There already was some capacitance; we need to add on to it ok. How do we need to add how do we figure out? How to how much to add on? We can figure out by estimating the first pole with the miller amplified second capacitor. We can figure out the second pole by assuming that these capacitors are short circuits at the very high frequency that we are talking about ok. So, this looks like a diode connected transistor. So, we figure out the first pole and the second pole. The ratio of these 2 poles has to be as specified by the phase margin and the DC gain. So, DC gain and phase margin, we already know the ratio of these 2 poles right, and that will give us, how much this extra capacitance has to be fine.

Now this is the methodology, I am just trying to go through the entire methodology. After doing all this, you should be telling me that we made one mistake. What is the mistake? The mistake is that so far we have not talked about, we have we have seen that the output impedance has 2 poles, right. We have been talking only about those 2 poles. The short circuit trans conductance gave us a couple of right half plane 0's one of those 2 right half plane 0s is at a very large frequency, this input right half plane 0. Right, this is at a very large frequency because g m is going to be large and this overlap capacitance C g d is going to be small.

So, this particular one is not really of any concern; however, we have added on to this capacitor value, right. We have increased this capacitor value. It is no longer just a parasitic overlap capacitance. It is no longer gate to drain capacitance ok. We have added by doing the compensation exercise, we have added extra stuff over here right. And that is going to make this second right half plane 0, the location of the second right half plane 0 if you remember. If you do not remember we will work it out again, right. How to quickly estimate the right half plane 0, there is a nice shortcut method. But in any case if you remember it is g m of the second stage, divided by this capacitance all right.

Now this capacitance has become large and therefore, this particular frequency has become a reasonably small frequency. Small enough to start competing with the 2 poles might even come in between the 2 poles, and it is going to mess up your entire plot bode plot. Right, all the phase margin calculations, everything is going to go for a toss, because now there is a right half plane 0. Remember, we did the phase margin calculation assuming that the system has only 2 poles. We did not talk about any 0’s

right. And for that phase margin calculation we found that there it needs to be a certain ratio between the 2 poles.

Now, if you throw in a 0 the entire thing is out ok. So, we somehow I have to do something about this particular 0. So, let us do a quick thing.

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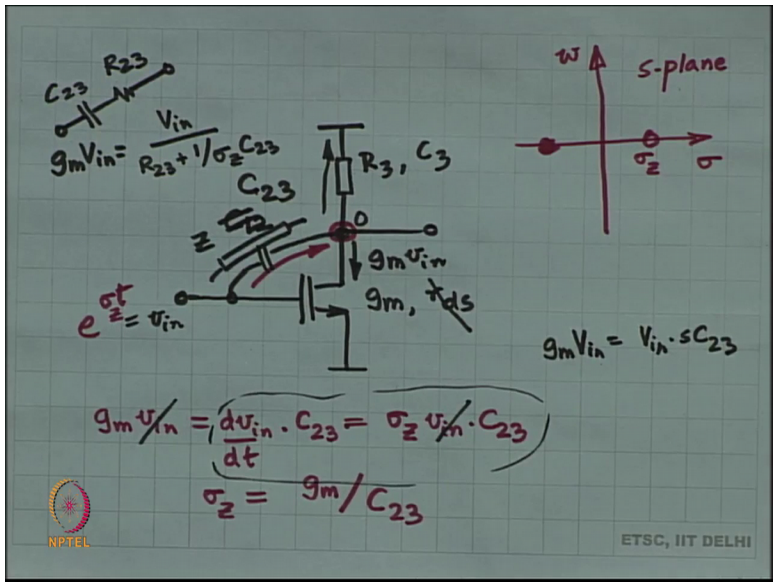

Let us see let us just to one analysis, oh, this was called C 2 3 ok. So, this is my second stage all right. And suppose I ask you to compute only the 0 suppose I asked you to compute only the 0. Is there any intuitive way to find out to calculate the 0 without going into complex calculations? And the answer is yes, there is, right. What do you have to first figure out realise is that a 0, the meaning of a 0 is that the response at that particular frequency is equal to 0, which means if I apply a voltage at the input then at that 0 frequency the output is going to be 0 ok.

This is the meaning of the word 0; however, you also have to understand that this frequency that we are talking about is not really any frequency ok. On the S plane, this frequency happens to be on the real axis, it is a right half plane 0. So, it is going to be over here ok. And this is not really a so called frequency right, it is some sigma. It is not omega right; which means that the kind of input you have to apply is not a sine wave right. You have to apply some kind of e power sigma t right. So, if I apply a voltage over here looking like e power sigma t, then the response is going to be 0 ok.

This is the understanding fine, all right. Now let us just apply that input, whatever that input is let us apply that. It is probably e power sigma z times t let us apply that. Now after I have applied that, the voltage over here is 0; which means that the current through these R 3 C 3 all of that is equal to 0 ok. So, both sides of R 3 and C 3 the current is 0. The current through r ds, remember, inside the mosfet there is r ds to ground, the current through r ds is also 0, because both sides are at 0 volts. So, it does not matter. So, all that is there in the mosfet is g m times v in ok, and where is this current going to come from? All the other currents are 0 it has to come through the capacitor.

There is no other exit way for it all right. So, if you do a quick KCL, now you have got g m times v in is equal to v in times C 2 3 d v by dt. And that is going to be sigma z, v in d v in by dt is sigma z times v in right. Is this ok? And that means, you can now cancel v in from both sides, and suddenly sigma z is equal to g m by C 2 3, nothing else, it is not dependent on any other parameters, all that it depends on is g m and C 2 3, fine? Is this analysis? All right, now supposing this was not a pure capacitor, we could we could just a minute, we could also have instead of doing this time domain calculation.

We could also have written it as you know v in times S C 2 3; where S is implied to be equal to sigma z ok. So, instead of doing this time domain calculation, we could have done g m times v in is equal to right, this is the Laplace transform capital v in is equal to v in times S C 2 3 at S is equal to sigma z fine, we could have done that, all right. Now suppose this capacitor is not a capacitor, but an impedance z a complex impedance z, then what will you do? You are going to do g m times v in is equal to v in by z. At S is equal to S z, you have to work out what z is at S is equal to S z sigma z, ok. So, suppose this z is a capacitor in series with the resistor, C 2 3 in series with R 2 3, suppose.

Then what is go? What is what is going to happen? You are going to say g m v in is equal to v in times v in by g m v in is this current; is equal to v in by series combination of this R 2 3 plus 1 by sigma z C 2 3 is this ok? And in such a case, you can still cancel v in from both sides, and then you can simplify fine, ok. So, I have just simplified it, if and whenever you do such a thing, you have to do a sanity check if R 2 3 happens to be 0, the way I have written it you automatically see that the answer is the old answered g m by C 2 3,.

But this also gives you a new result; that if R 2 3 happens to be equal to 1 by g m. Then what happens? Sigma z is infinite right. So, sigma z the 0 frequency is thrown of all the way to infinity right. So, it is now a 0 at infinity which is as good as saying there is no 0 anymore right. There is no such 0 frequency anymore. So, all that you have to do now is have R 2 3 in series with C 2 3. So, therefore, the plan is that instead of compensating with just a capacitor C 2 3 between these 2 nodes, we are going to compensate with this structure ; where this resistance is 1 by the sum of these 2 g m's right.

And this compensation capacitor is whatever compensation capacitor we had calculated ok. So, this is you know how you compensate the overall circuit. Right this is kind of the final result of compensation fine. So, what all have we learnt? We figured out how to do a how to find out the 0 frequency in a short way right. What is the short technique? The short technique is to assume that at that 0 frequency the output voltage is equal to 0 by definition, ok. Then all of these extra things go away, all that remains is g m and whatever is happening in the cross path right, in from that you can work out the 0 frequency, fine?

This is one thing. We also figured out how our overall you know compensation technique is related to our Op-Amp design, right. We took an example of a complicate this is actually not a simple example. This self-biased active load Op-Amp, right def amp is actually one of the more complicated once. If you think of an ordinary differential amplifier which is completely symmetric then the result is even easier, because you just break it up into half circuits.

And in the half circuit you do the compensation right. You do the comp you draw your complete amplifier, break it up into half circuits, in the differential mode half circuit you apply your compensation technique; do the compensation in the differential mode half circuit. And then reverse come back to the full circuit right in the full circuit you will have 2 compensation capacitors across the 2 output stages right, in the 2 halves. So, that is you know the more general technique of doing this. So, all the things that we have studied, current mirrors right differential amplifiers constant g m biased circuits right.

And then all of these frequency response things, they all come together and finally, you make the Op-Amp. So, Op-Amp design is you know something that puts all of these techniques together, ok. So, invariably in exams of this particular course, you are going

to get an Op-Amp design right. Either you will be asked you will be given some I mean you know typical questions can be 2 into 2 different ways.

One way is that you are given the specs like DC gain oh we didn't talk about bandwidth ok. So, we have to talk about bandwidth. We are going to talk about bandwidth just now. So, you are going to be typically questions are going to be you are going to be given DC gain bandwidth power consumption, and then you will be asked to design the Op-Amp right.

One can walk through these steps. The other possibility would be to analyse, right you will be given the Op-Amp circuit, and you will be said told that tell me, what is the DC gain. Tell me how do I compensate this, what is that compensation capacitor right, and then what is the band width what is the power consumption. So, at the undergraduate level we normally avoid design type questions we ask analysis type questions; however, design type questions are more useful right that kind of an exercise gives you a direct insight into how the Op-Amp is going to be designed in the industry right. So, engineering a lot of engineering is preparing you for the industry, not preparing you for exams, right.

So, if you want exam preparation, then yes at the undergraduate level this is what we ask? We ask you to analyse not design, but in the industry you will be asked to design an Op-Amp, then what do you do? You say I did not study design I studied only analysis. No, you have 2 buckle up and you have to you know design to the specifications that have been given, ok. So, these are the 2 kinds of exercises that you normally get; design and analysis. All right, now quickly we are going to talk about bandwidth. Bandwidth is actually very straightforward.

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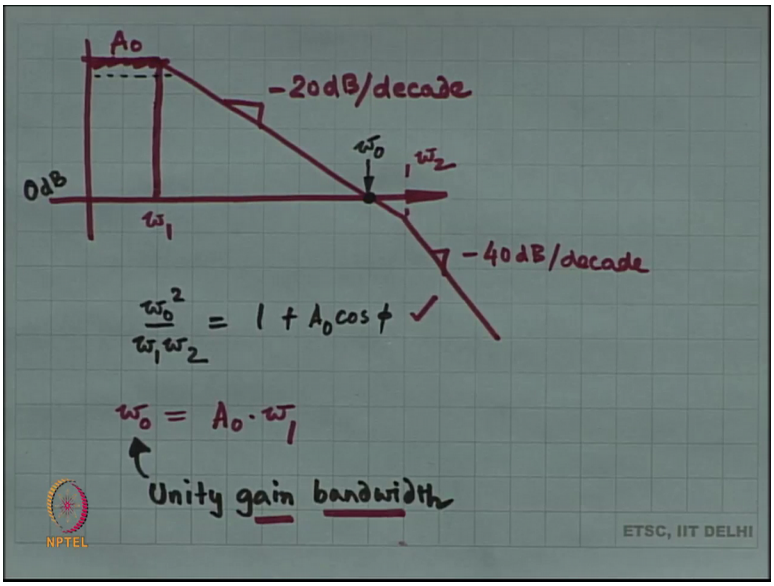

Remember, when we did the bode plot we had 2 poles, right. We had a DC gain and then we had 2 poles. And for a given phase margin, we also had a relationship between the 2 poles, right we had omega 2 by omega 1 equal to so much, right.

We also had a second relationship and a simpler one, between omega 2 omega 1 and omega naught ok. Omega naught is the gain crossover frequency. That is the frequency at which the gain is 0 dB or in other words 1, the gain is 1 at this particular frequency ok. So, we had a relationship between omega 2 omega 1 and omega naught. And that was typically something like omega naught squared, if you can check your notes 1 plus A naught cos phi, yeah, something like this ok.

So, if I know the value of omega 1 omega 2, then I know the value of omega naught. If I say just look at the bode plot, if you say that omega 2 is much higher, omega 2 is a large frequency, right. Do you see something happening between omega 1 and omega naught? Suppose this does not exists, ok. The relationship between omega 1 and omega naught is just this minus 20 dB per decade, what does minus 20 dB per decade mean?

It means that if I increase frequency some k times, then the gain is going to go down k times right. You can write this gain going down k times in terms of decibels, but actually what it means is, that if frequency goes up 10 times that is a decade then the gain drops 20 dB which is 10 times, right a frequency goes up 100 times, gain drops 100 times. If frequency goes up k times gain is going to go down k times. So, here I have gain coming

down gain decreasing by a factor A naught. It started with a gain of A naught ended up with a gain of 1. What is the ratio between omega naught and omega 1? It is therefore, going to be equal to A naught, because gain has dropped by a by A naught times, therefore, frequency must have increased A naught times.

So, this relationship is fine this is right, but it is also possible to say that omega 2 is a very high frequency, let us not bother about it at all. And omega naught is nothing but A naught times omega 1. It is possible to say such a thing. In which case the gain crossover frequency, the frequency at which the amplifier has a gain of 1 is nothing but A naught times omega. All right, now when you talk about bandwidth typically if you have done any communications or filters or anything they will say what is the 3 dB bandwidth; that is, what is the frequency at which gain has dropped 3 dB ok.

Unfortunately, in amplifier design we do not talk about that bandwidth at all. For us, the unity gain bandwidth is more important, the unity gain bandwidth is nothing but omega naught. And when you talk about bandwidth, you are just going to state the unity gain bandwidth omega naught. Unity means 1.

It also happens to be the product of A naught and omega 1. This value omega naught happens to be the multiplication of A naught times omega 1. So, if you say that the 3 dB bandwidth is omega 1 that is just bandwidth. And the gain is A naught, then the gain bandwidth product is omega naught, ok. So, another way of calling it saying the same thing right gain bandwidth gain times bandwidth is omega naught all right. So, there are many ways of calling this.

So, we typically as far as amplifier design is concerned, we typically specify the unity gain bandwidth the frequency at which the gain drops to one. And the reason why we do this is related to your Op-Amp circuit which is your favourite Op-Amp circuit, this one this is my favourite Op-Amp circuit ok.

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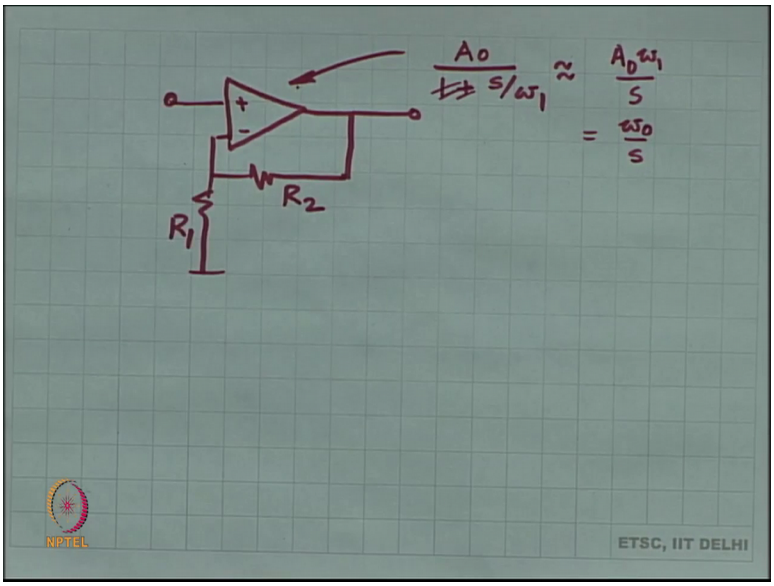

If I approximate this Op-Amp as something which has a response that looks like this, A naught divided by 1 plus S by omega 1. It is also possible to say that omega 1 is such a small frequency, that this 1 makes no difference.

This is this could also be approximated as A naught omega 1 by S; which means that this could be approximated as omega naught by S. So, the whole Op-Amp could be approximated as omega naught by S all right. So, anyway so, this is the reason why. You are going to find that if you have a block like this, omega naught by S, then the bandwidth is only related to omega naught.

In fact, the 3 dB bandwidth of this circuit is going to be related to just omega naught and the gain of this circuit. So, we will do this in the next class. So far this is where we stand that we have understood how all of our techniques related to relate to Op-Amp design ok.

Thank you.