Analog Electronic Circuits
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Lecture – 29
Cascade amplifier (with capacitance)

Welcome back to Analog Electronics Lectures. Today's lecture 29 and we are going to talk about the Cascade amplifier. Actually in the last class we had the intention of talking about both cascode and cascade, but clearly I was over ambitious right. We only managed to do the cascode, today we will talk about the cascaded amplifier with the effect of capacitances.

Now you would think that the cascaded amplifier is easy, it is not, ok. So, let us just draw one and the DC stuff is very easy. So, we will quickly do the DC stuff and then move on to the AC.

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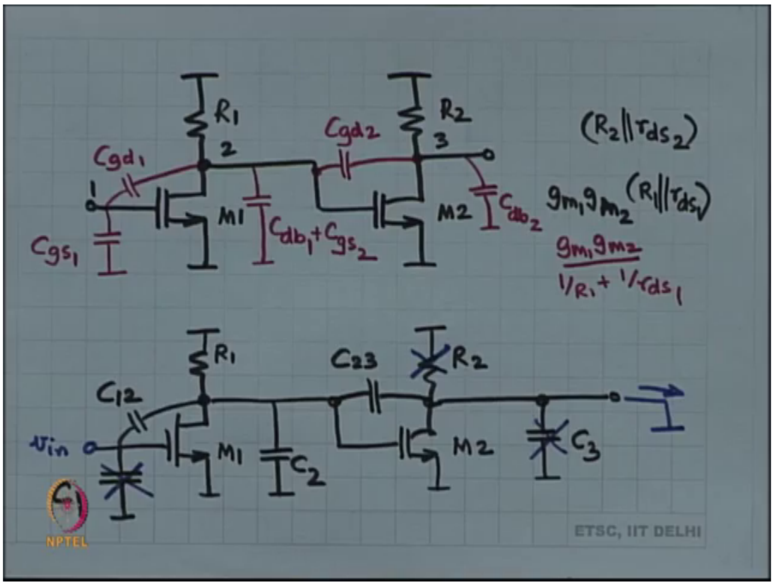

So, this is the cascade amplifier right two common source amplifiers one after the other and let us call them M 1, M 2, R 1, R 2 if you think of each separately then, this has an output impedance of r ds 1 in parallel with R 1. This has a transconductance of g m 1 ok. And therefore, the gain is g m 1 minus g m 1 times R 1 in parallel with r ds 1 and the same happens to the second one ok. So, it looks very straightforward the second one will I mean overall you will have a gain of g m 1 times g m 2 times R 1 in parallel with r ds 1 and R 2 in parallel with r ds 2. You could also do this a little differently, you could just find out the output impedance from the second stage. The output impedance from the second stage is R 2 in parallel with r ds 2.

This is the output impedance and the transconductance from just the second stage I will apply v in over here and measure the short circuit current at the output of the second stage right. If I apply v in over here that is going to create g m minus g m 1 times R 1 parallel r ds 1 over here and that will create g m 2 times that will be the short circuit current. So, the short circuit current is g m 1 g m 2 times R 1 in parallel with r ds 1 and that is it.

So, you have got the overall short circuit current, transconductance, this is the overall short circuit transconductance. This is the overall output impedance, the product of the two is the voltage gain, ok. So, it is same story. So, same story I did it in two different ways this is what happens at DC. So, it is very easy to work out at DC. However, our business is not at DC anymore right. DC was a long time back right, 20 lectures back we were thinking of DC now we have to plug in the capacitors and I have 4 capacitors for each device. So, let us do g m 1 first. I have got C gs 1 and I have got C gd 1 and once again you see C gd 1 is going to be very annoying, very annoying C gd 1. And, then I have got C drain to body of 1. I have got C source to body of 1, but that is that need not be drawn at all because source is at ground body is also at ground, ok.

So, you need not worry about source to body. Then device number 2, I have got C gs of 2. The C gs of 2 and C db of 1 are in shunt. Then I have got C gd of 2 which is even more annoying than C gd 1 think about C gd 1 was annoying C gd 2 who is even more annoying because, at least in C gd 1 you know sometimes this side is going to be grounded and so on, you have some respite here there is no respite. This is the most annoying one of the lot. And, then you have C drain to body of 2. And finally, you have C source to body of 2, but that is also irrelevant because both source and body are at ground ok.

Now, we need to be I do not want to keep drawing this again and again. So, I will label the nodes a little bit. So, I am going to call this node number 1 I think last time we did the input was called as node number 1. This I am going to call as node number 2 and this I am going to call as node number 3 and now I am going to redraw it. And you know what these capacitors are, just that I am going to call C gs 1 as C 1 and I am going to call C gd 1 as C 12. And, I am going to call this C db 1 plus C gs 2 as C 2 and then instead of C gd 2 I am going to call it C 23 and lastly I am going to have C 3 instead of C db 2, ok.

So, this is the circuit that I am going to analyze. And, you know what these C 1 C 12 what these are right. They are they correspond to these values ok. So, this is the notation we are going to use right now. What you want to do? Shall we do the short circuit transconductance first? Let us do that because I know in advance it happens to be easier ok. I know it is easier to work out the short circuit transconductance let us do that first.

So, when I do the short circuit transconductance over here the output is grounded ok. And we are going to measure the current through this output. So, when I ground this output there is no current through C 3, there is no current through R 2 ok. These are all irrelevant r ds 2 is gone inside this MOSFET there is only g m 2 ok. And that is it so far so good.

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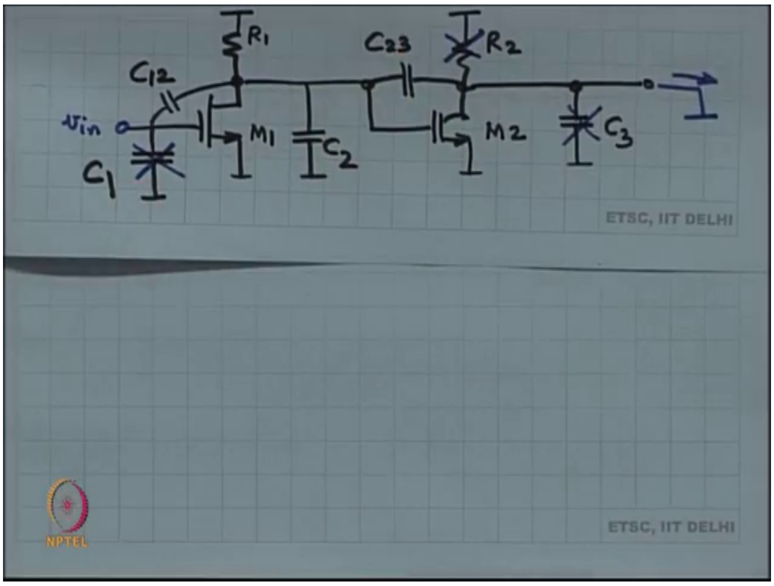

What about C 1? Do I have to worry about C 1? No, because it is forming a private loop with v 1 and this current is not going to go through the short circuit at all. So, do not worry about C 1. All I have is C 1 2, C 2 and C 2 3 ok.

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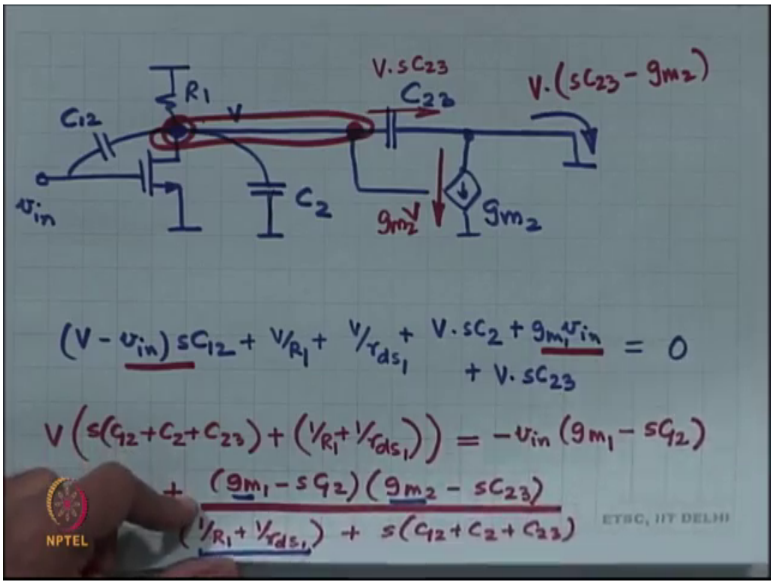

So, redraw that is all. Ok, I have broken up the transistor. I have broken up the m 2 to indicate that r ds 2 is gone ok, it is only g m 2 fine. What you will notice is that C 23 is not so irritating in this particular setup, alright. If I know the voltage over here then, the current through C 23 is easy to find. It is just s C 23 times the voltage over here. Now, what is going to be the voltage over here? I have got v in, let us do a KCL over there and figure out the voltage ok. So, let us call this voltage as V. V minus v in times sC 1 2 that is the current this way plus V by R 1, plus V by r ds 1 plus V times sC 2.

Student: G.

G m is a minus, no plus g m times v in ok, plus V times sC 23 this whole thing is equal to 0 ok. So, ordinarily I do not like writing these KCL equations, but in this case I have written it, please bear with me. Then, you put the v in’s on one side and the V's on the other side there are only two v in terms alright. And the others all form the denominator. This was g m 1 and therefore, I know what is V, V is v in times g m 1 minus sC 12 divided by this whole denominator alright. But that is no good. I need my answer, my answer what is my answer? If this is V, this current is V times sC 23. This current is g m 2 times V.

So, what is the short circuit current? The short circuit current is V times sC 23 minus g m 2 ok. So, knowing V is not enough I need to multiply it by that factor. That is the short circuit current. So, my short circuit current finally, is or rather let me write out the short circuit transconductance is what? So, this is the expression for the short circuit transconductance. What did I do? I did V by v in divided by V. I am sorry, I found out V in terms of v in. So, V by v in is g m 1 minus sC 12 divided by this, that was V by v in, but I wanted V times so much right. That was the current, current divided by v in is therefore, just V by v in times this extra factor ok.

So, this is my short circuit transconductance. And, unfortunately it is not complete right you have to put it in the form alright. And what is the form? The form is DC term times you know one plus the poles 1 minus the pole 1 minus the 0 or whatever product of 0's product of poles right. So, you have to take the dc term common outside and my dc term was quite straightforward it was just this g m 1 g m 2; g m 1 g m 2 divided by 1 by R 1 plus 1 by r ds 1. So, I am almost there in fact, g m 1 g m 2 ok. So, I have to take these things common outside forcefully even though things are not really common. So, my short circuit transconductance finally looks like this.

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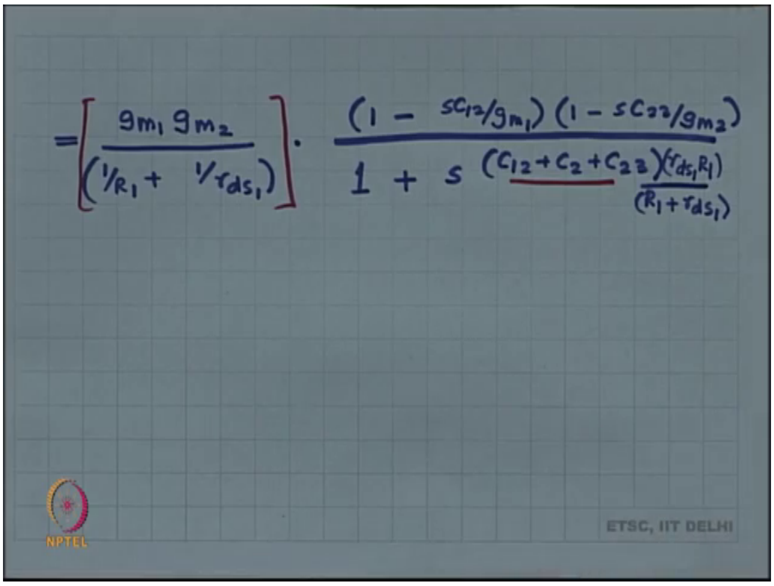

What has happened over here? In my short circuit current, I got two right half plane 0's one right half plane because of sC 12 and g m 1, let us look at the circuit sC 12 C 12 and g m 1 gave me one right half plane 0. So, try to try to see try to get a feel for what is going on if you see there is an m 1, there is a path through m 1 g m 1 and there is another path through s C 12 from v in to V ok. This is what is creating the right half plane zero.

Again, there is a path from V to the output through g m 2, there is a path from V to the output through C 23 that is what is creating the zero the right half plane zero.

So, you see there is a second term sC 23 by g m 2 ok. So, your right half plane zero is at the location g m 2 by sC 23 I am sorry C 23. So, if you say what is the value of the right half plane 0, it is at g m 2 divided by C 23 that is the frequency, g m 1 divided by C 12 that is the frequency ok. If you look back you open your common source amplifier you will see exactly the same thing, you open your expression for the cascode amplifier you see exactly the same thing, g m 1 divided by C 12 alright.

So, something very interesting is going on over here right, we seem to be lost in the maths, but we are not ok. We are trying to develop the intuition over here, that the right half plane zero that we are getting is related to this transconductance and C 12. And there are two such right half plane zeros over here because there were two paths, two times, once over here once more over here. Two right half plane zeros, one is g m 1 by C 12, the second is g m 2 by C 23 plus, right half plane 0 alright.

So, that is something that we saw. What else are we seeing? We are seeing that there is a pole. The pole is because of r ds 1 R 1, so some parallel parallel impedance, parallel resistance of r ds 1 and R 1 and a capacitance of C 12, C 2 and C 23. Let us look at the circuit. So, if you look at this particular node, there is only one node in this in this circuit only one unknown node is there. All other nodes are known, that is v in this node is 0 volts, there is only one node which is where the voltage is not known ok.

So, if you look at that particular node, then what is the impedance that you see? You see R 1 in parallel with r ds 1, R 1 in parallel with r ds 1, that is the resistance part of it. If you look at the capacitance part of it you have got C 2 to ground, C 23 to ground and you have got C 12 to v in and the zero part you have already taken care off right? So, you can think of this as a ground superposition, think superposition right? So, you have got C 2 to ground, C 23 to ground C 12 to ground. So, the effective capacitance is C 12 plus C 23 plus C 2 alright.

So, if you look at that one node where the voltage was not known, you inspect that one node where the voltage is not known, what is the effective resistance there? It is R 1 in parallel with r ds 1. There is no other resistance. What is the effective capacitance there? It is C 12 plus C 2 plus C 23, there is nothing else.

So, therefore, you can directly write this whole expression by inspection. This was the dc term which you knew beforehand and then the remaining part ok, one plus sC R is the pole, 1 plus s what is C? The C is the effective capacitance at that one unknown node. What is the R? R is the effective resistance at that one unknown node alright? And then, you are looking at the right half plane zeroes, and the right half plane zeros by now you probably are getting the hint, then it is g m 1 by s the by C 12 is 1, g m 2 by C 23 is the other. And that is it, and the entire expression can be written just by inspection ok.

So, the idea is to get to a level where you can start writing things by inspection. That is the agenda. Now, do not always try to write things by inspection sometimes you have to think as well ok. So, let us now go to the second half of the work. So, this is only half of the work right. The other half of the work is to find the output impedance. And my expected dc quantity is just this much, R 2 in parallel with r ds 2. I will have to look at the look in from the output null the input looking from the output and find the impedance.

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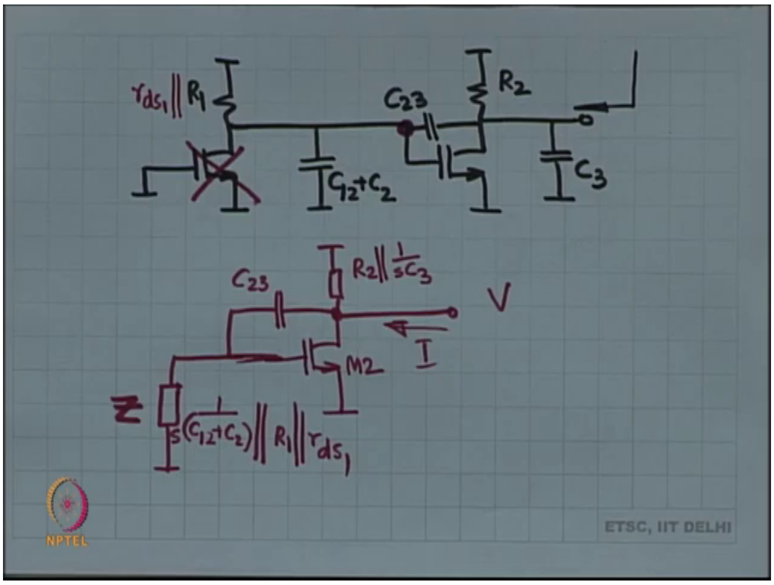

So, this is my circuit. I have already nulled the input I had some capacitors around. I had C 12 between node 1 and 2, but that C 12 is going to add to C 2. And then, I had C 3 between node 3 and ground and I had C 23 between node 2 and node 3. So, this was my circuit ok? So, the only important simplification is that C 12 is now sorted out alright.

So, we are going to now find the output impedance looking in from here. What is so hard about this? Is this hard? You look in from the output, you see R 2 and C 3 and maybe r ds 2 right. What about all of this stuff? Does it matter? What is the voltage here? So, ordinarily at dc that voltage used to be ground, because my input was a ground ok? So, this current g m was a was 0 volts, 0 amperes g m times the input right that was 0 amperes that was flowing through R 1 and r ds 1.

So, therefore, the voltage over here was equal to 0 volts? But now that is no longer true, this voltage is now related to the output through this capacitance C 23 it is, I am telling you the C 23 is going to cause havoc. If C 23 had not been there in this picture then this voltage would have been 0 volts ok. C 23 if this capacitance had not been in the picture all right, the voltage here would have been a clean 0 because the input is 0 that created g m 1 times zero, g m 1 times 0 is flowing through R 1, r ds 1 and C 12 plus C 2, and if a 0 is flowing through a RC combination then the result is a clean zero ok? So, there was nothing to be done, alright.

Now, what is happening is that I am applying a voltage from outside for the output impedance, what do you do? You apply a voltage from outside and see how much current is going inside. So, you have applied a voltage outside. Now when you apply a voltage outside C 23 couples that voltage to this node somehow. So, this node is no longer at zero ok, you have applied a voltage V over here all right, I agree that this current is zero, but that is not the end of the word ok. So, let us simplify the inside this MOSFET this current is 0. So, let us not draw this MOSFET at all and let us write this as ok? So, the MOSFET is gone ok, in fact, you could probably even draw it like this. Ok?.

So, you have got R 1 in parallel with r ds 1 over here, you have got C 12 and C 2. So, I have put all of that as one Z. I have drawn all of that as a combined Z ok, lumped everything together as one impedance Z from this node to ground. And then in between here and the output, you have got C 23 and then over here you are applying a voltage V and trying to measure what is the current I right. This is what you are doing.

Now, when you have applied voltage V, there is going to be voltage division between C 23 and this impedance Z and therefore, you will get some voltage at the gate it would not be zero anymore alright. So, this is the big deal over here, this is the problem. The problem is this C 23, the presence of the C 23 has coupled the voltage at the output back to the gate of the second MOSFET M 2 ok. And this is going to create current through M 2. So, now, g m 2 is going to come into life and start drawing current. Fine? You see the complication, the complication is as follows.

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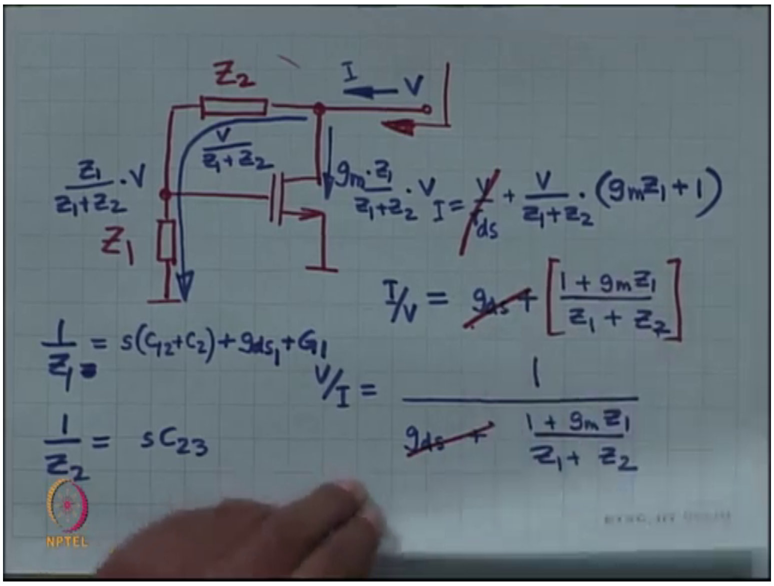

So, let us just do this. Let us just do this much. I have a MOSFET Z 2 across gate and drain and Z 1 between gate and ground. What is the impedance looping in? Think for a moment, let us say Z 1 was not there open circuit. So, Z one let us say is very large. If Z 1 is very large then no current flows through Z 2, then the voltage over here and the voltage over here are equal. So, if I apply V over here I get V over here. Now if I apply V over here then the MOSFET responds by pulling g m times V current. Ok? x

Had this voltage been V so I have applied V I am imagining Z 1 is not there ok, if I for now temporarily. I am just trying to understand what happens. So, if I apply V over here I get V over here right? Because no current goes through Z 2, Z 1 is not there open circuit. Now if I apply V over here then the MOSFET responds by pulling g m times V of course, inside the MOSFET there is also some r ds ok, r ds is between the output and ground anyway.

So, I have got g m times V current coming this way and I have got r ds. So, the output impedance is going to be r ds in parallel with one by g m alright. The output conductance is going to be g m plus g ds I have applied V, I am getting g m times V plus g ds times V.

So, the output conductance is g m plus g ds. The output resistance is one by g m in parallel with r ds all right, this is what happens when Z 1 is not there. Now, let us throw Z 1 back into the picture. I apply V, what is the voltage I get over here? I will get a voltage division between Z 1 and Z 2. So, I get V times Z 1 by Z 1 plus Z 2, ok? What is the mosfet going to do? It is going to respond by drawing g m times this voltage. Ok and of course, r ds is there in parallel. What is there is also one more path now for current, current also flows this way ok, the current this way is V divided by Z 1 plus Z 2. All right?

So, the net current that comes in from outside is the sum of these two currents, fine? So, you get V by Z 1 plus Z 2 times g m Z 1 plus 1 ok, that is the sum of the two currents coming in. So, if this is I, actually there is one more because of r ds. So, let us add that also alright.

So, if you look at the output resistance, so this is the total current I is V by r ds plus V by Z 1 plus Z 2 times so much. So, the total output resistance is V divided by I ok. Output conductance is I divided by V, I divided by V let us just do output conductance because it is easier. Ok? So, this is the output conductance, output resistance would be one by of this fine. Now, what is our situation? Our situation has Z 1 as a combination of all of this, Z 2 as C 2,3 let us leave out this g ds for now, it is it is just going to come in parallel later on. Ok?

So, I will have R 2, I will have C 3, I will have r ds 2 and then I will have the rest. So, if I just focus on the rest, then it is just you know that is the output conductance. So, let us not look at the other part. So, it is Z 1 plus Z 2 divided by one plus g m Z 1 and then we will place all of these in parallel. Ok? So, output conductance because of g m, I have got output conductance because of g m and that is so much alright.

In our specific case Z 1 is this complicated quantity, Z 2 is 1 by sC 23. Look at a situation where Z 2 is infinity, just test, test it out. If Z 2 is infinity this output conductance boils down to 0, that is the MOSFET does not respond, if Z 2 happens to be open circuit. Right? Sanity check, this is a sanity check sometimes you need to do these sanity checks just to see that you are in the right path. Ok, you plug in Z 2 equal to infinity, if I plug it in then immediately I see I by V is equal to zero which means that the

MOSFET does not respond when I apply voltage at the output. Ok, I have d embedded r ds completely.

So, in our case Z 1, actually Z 1 is hard, 1 by Z 1 is something that I have readily. Ok, this is one by Z 1, I do not even have Z 1 and I have got one by Z 2, ok. This is what I have. Maybe you want to represent this in terms of one by Z 1 and one by Z 2. So, this output conductance is

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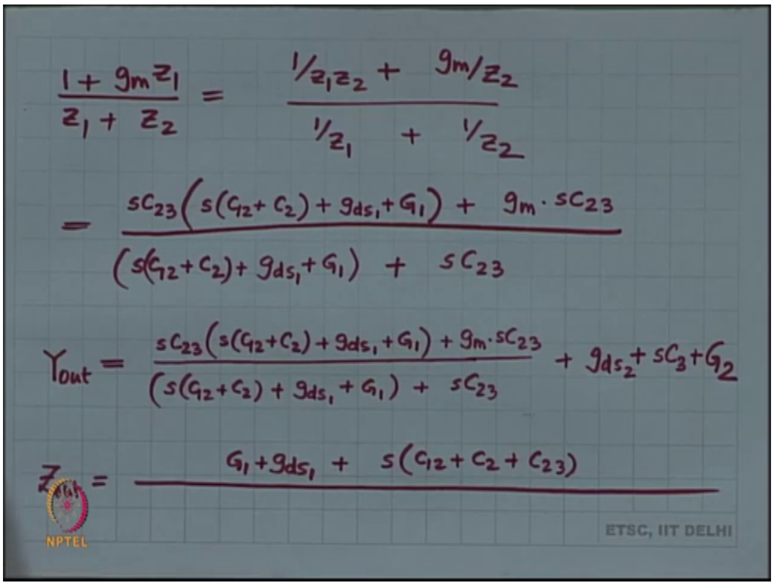

So, let us divide numerator and denominator by Z 1 Z 2. Ok? And what we are now going to do is, we know the value of one by Z 1 and we know the value of one by Z 2. One by Z 1 is the parallel combination of C 12, C 2, rd s 1, R 1. And one by Z 2 is just sC 23. Ok?

So, this is my output conductance because of the MOSFET, and you have to add to this the other terms r ds 1, R 2, and C 3. Fine? And what is my Z out, Z out is one by this entire monster. Ok now, where are we leading to? What are we leading to? can we look at the poles and zeros of Z out? So, it is going to be one divided by this whole thing and naturally you are going to multiply numerator and denominator by this quantity right. So, this quantity will come to the numerator. Let us write it out cleanly, you have g 1 plus g ds 1 plus S times C 12 plus C 2 plus C 23. Ok? This is what will come in the numerator. Right any comments? No comments? There should be a comment. This and the pole of the short circuit current are the same ok?

The short circuit current had a pole one plus S blah blah right. C 12 plus C 2 plus C 23 times the parallel combination of r ds 1 and R 1. Here I have the parallel combination of r ds 1 and R 1 and I have C 12 plus C 2 plus C 23 ok? Of course, I have to take that thing common out right. As soon as I take g 1 plus g ds 1 common right I will get exactly the same thing. I mean you have to take it common, g 1 plus g ds 1 has to come outside and then you get exactly the same thing as the pole of the short circuit current.

So, the pole of the short circuit current cancels out completely with the zero of the output impedance. That is something very interesting, this is exactly what happened in the cascode amplifier as well. Cascode amplifier, the short circuit current had a pole and a zero right, right half plane zero and pole right. It had one right half plane zero one pole. Here we had two right half plane zeros and one pole for the short circuit current. Then, in the cascode amplifier the output impedance had a 0 and then some second order denominator right.

So, a couple of poles which I said you cannot factorize right? So, we do not know where they are as of now right. Here also it is the same story, the output impedance has one zero and then you are going to I mean it is a mess right now it looks like there is a mess over there right. You can write it up, you will get something and trust me you would not be able to factorize it. So, you will get two poles in the output impedance 1 0 and this 0 happens to be exactly the same as that of the pole of the short circuit current alright.

So, what does this mean? This means that to analyze this entire thing so I am not going to write this. You write it all right it is just a waste of time, if some second order polynomial is going to come and trust me you are not going to be able to factorize it neither am I going to try. Alright, so I am not going to write it I do not plan to write it. Ok. Now, what is the deal over here?

The deal is that I apply a voltage at the input, I measure short circuit current. This gives me two zeros, one zero is g m 1 by c gd 1, another zero is g m 2 by c gd 2, both of these are right half plane zeros. Keep these two aside. Then, I am going to apply voltage here and measure the current going in to this particular node it itself to measure the output impedance, but here I am not going to worry about the 0's, I am only going to look at the poles. So, if I try look and what am I going to do with node one at that time? For the output impedance node 1 is going to be at ground. So, for the output impedance c gd this

C 12 is going to come in shunt with C 2. For the output impedance so, I have one capacitor over here, R 1 and g m 1 is 0 right; g m 1 C gs 1 is 0. So, over here all I have is R 1 in shunt with R 1 parallel r ds 1 in shunt with C 2 and C 12. Ok, that is the first stage. I keep that first stage and I am applying voltage at the output and trying to figure out what is the current coming in.

So, here I am not going to look at the 0 this node is an unknown voltage right. So, there is going to be a pole, because of this node or two poles because of this node. Alright, and then I have got R 2 and C 3, they are going to contribute a pole right. So, the resistance at this node and the capacitance at this node they are going to contribute a pole, I do not know what that capacitance what that resistance is. Resistance is clearly, clearly there is some resistance and some capacitance it is going to contribute a pole and then the resistance and capacitance at the first node at node number 2 they are also going to contribute a pole. Ok two poles in the system fine.

Now, we are going to take a little detour and, is this understanding so far? So, any complicated circuit can be broken up right; you are normally not going to get cascade of 3 amplifiers ok, it is not going to come right that that scenario is not going to show up. There, is a reason why we are going to discuss that. There is also this, that more or less if you if you understand so far then using the Norton equivalent method you can solve accurately any circuit. All you have to do is apply Norton correctly and you can solve it. I mean there is going to be some algebra and sometimes the algebra is going to be so messy that it might look very dirty. But you know you just go through it and work out whatever is required alright.

Now, we are going to take a detour, a slight detour actually two detours. Detour number one, so the first detour will just do very quickly right now and the next detour will take in the next class. So, the first detour is like this.

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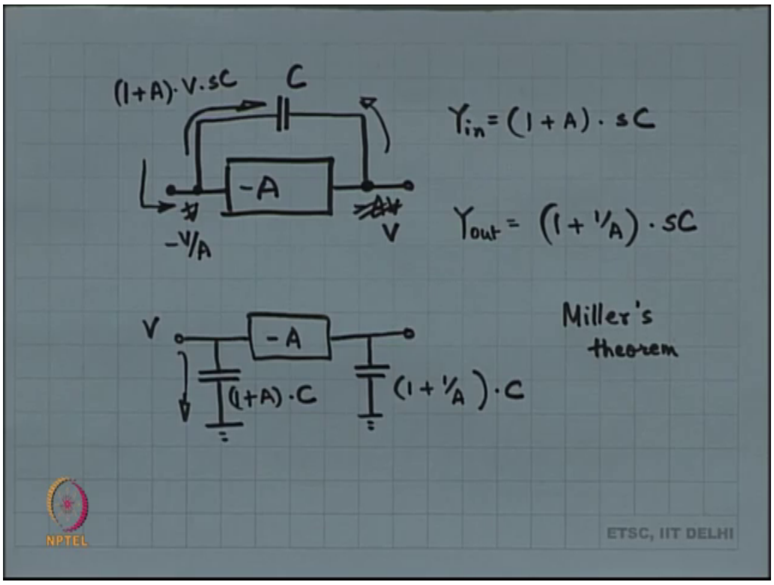

You see this setup where I have got C 23 in shunt is very annoying ok. So, I am going to just try to simplify a little bit. So, suppose I have got an amplifier of gain equal to minus A. Voltage gain which means if the voltage over here is V then the voltage over here is going to be minus A times V. If I have a capacitor C over here and I plan to measure the input impedance, then I have got V over here; how do I measure input impedance? I apply a voltage, measure the current. I apply V over here automatically I get minus AV here.

What is the current that the capacitor takes? It has V on one side, minus AV on the other side right. So, the potential difference is V plus AV or in other words 1 plus A times V times sC. So, the current taken by the capacitor is 1 plus A times V times sC. Ok, or in other words the input impedance I applied V, I got a current of so much. The input admittance is 1 plus A times sC that is the input admittance alright. What this means is, that the effective capacitance with respect to ground is 1 plus A times C. So, I applied a voltage V over here and I got a current 1 plus A times sC times V through the capacitor, as if it was going to ground. So, this could be a model. Likewise if you apply V at the output, then; obviously, the input has got to be minus V divided by A.

Because this is an amplifier of minus A which means that now the potential difference is V times 1 plus 1 by A. And, that means that the current that goes this way is 1 plus 1 by A times V times sC. And, that means that you could simplify a circuit that looks like this and redraw it in this fashion. So, this is called Miller's theorem. It is not really, it should not get the status of a theorem according to me, because there are a lot of fallacies in this I mean these two circuits are not really equivalent at all. In this circuit there was a path from the input to the output in this circuit there is no path from the input to the output, they just cannot be equivalent.

So, although it is called in the books it is called Miller’s theorem I ask you to take it with a pinch of salt it is not a theorem. It is some sort of an approximation. So, this approximation can be made to simplify a lot of circuits and give you insight as to what is going on over there. Right, it only can be used as a tool to gain insight alright. If you want to do precise mathematics then Miller is not for you. So, this is called Miller’s theorem. Although it is should not get the status of theorem as I said ok. So, this can be used to simplify our C 23 and C 12 and all of those you know tricky capacitors right. So, we are going to use this as a tool we will do it later on; before that I am going to take yet another detour right. This was detour number 1 ok.

So, we discussed the cascaded amplifier today. We actually did the complete analysis. I am actually quite happy with the analysis. We also discussed Miller’s theorem. We will come back to Miller’s theorem and the cascade analysis again, right after the next class, ok.

Thank you.