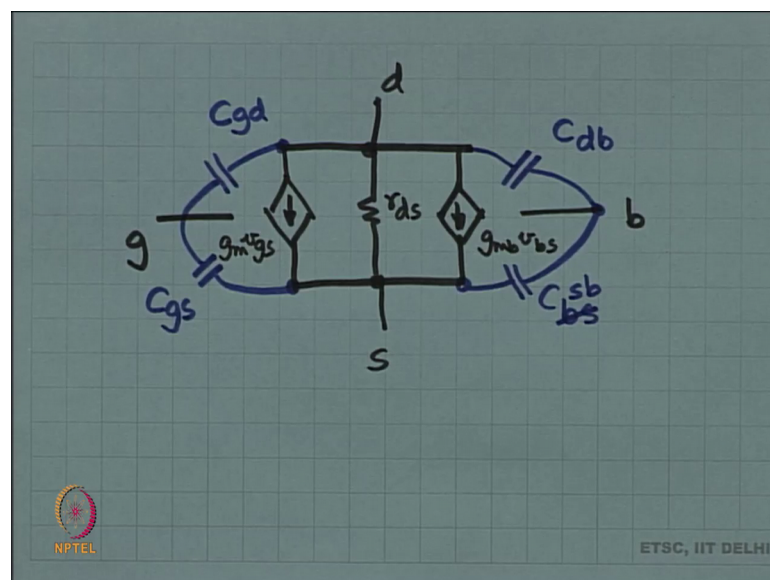


Analog Electronic Circuits
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Lecture - 26
Common source, drain, gate - revisited

Welcome back, this is Analog Electronic Circuits. This is lecture – 26 and today we are going to talk about the common source, common gate, common drain circuits revisiting, ok. So, in the last class we had looked at capacitance exclusively capacitance in the MOSFET and we saw that the MOSFET's small signal model not only has g_m , r_{ds} , g_{mb} .

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So, the MOSFET small signal model not only had these three components g_m , r_{ds} , g_{mb} , right. So, we had $g_m v_{gs}$, $g_{mb} v_{bs}$, r_{ds} , these were the three standard ones that we have been looking at from the beginning and then because of capacitance there are four more elements I have got C_{gd} . C_{gd} is comprised of SIOX one third of SIOX at pinch of plus overlap gate to drain overlap. So, one third of SIOX plus gate to drain overlap C_{gs} comprises of two third of SIOX at pinch of plus gate to source overlap.

Now, at pinch of this is two third of C_{ox} , but beyond pinch of well beyond pinch of it becomes almost all of SIOX and C_{gd} likewise becomes closer to 0 right and you are left with only overlap for C_{gd} . Then you have got C_{bs} and C_{bs} comprises of junction

capacitance between body and source, and this is dependent on the bias voltages of the source and the body. So, body if it if body and source are at equal voltage then you get only the 0 bias depletion width if sources at a higher voltage then the body then the width becomes more the depletion width becomes more and therefore, the capacitance becomes less. So, the maximum capacitance over here is when it is 0 bias, right, when body voltage is equal to source voltage.

And, likewise the drain to body volt capacitance is also there. This is also a junction capacitance and this also depends on the drain voltage as well as the body voltage drain to body bias voltage. Body is the lowest voltage in the NMOS right drain is going to be a reasonably high voltage assuming that you are in the flat region of the MOSFET, right. Is drain a high voltage or no? Drain is reasonably high, I mean the v_{ds} sorry v_{drain} to source has to be more than $v_{gs} - v_t$. So, drain is v_{ds} somewhat large at least more than 0.2, 0.3, right.

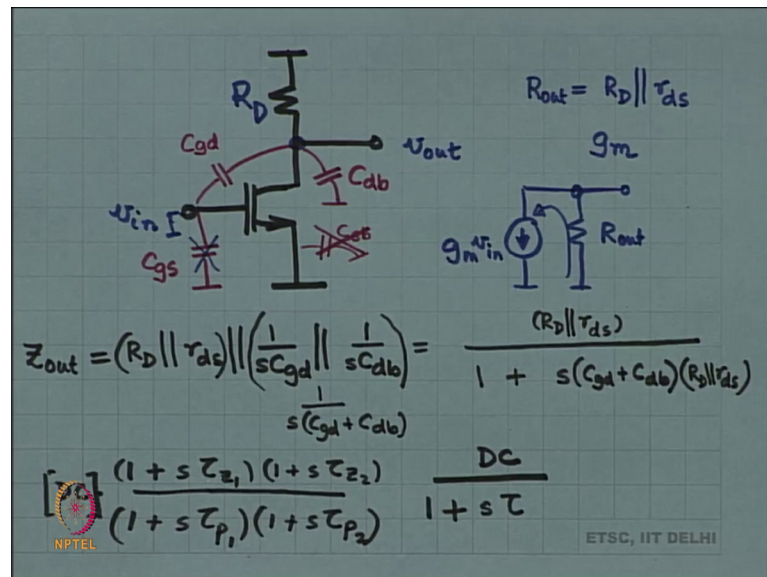
So, drain to body is reverse biased if drain to body is reverse bias then the drain with the C_{db} the junction capacitance is small or large? Small, because the depletion width is more, right when you are reverse biasing the depletion width is increasing, that is the reverse bias right depletion width increasing means it is harder for the carriers to come from this side to that side, right. So, that is why the depletion width is increasing when the reverse bias is increasing, that is how you remember.

Now, if the depletion width is increasing then the capacitance is going down because the insulator has is now bigger, wider thicker alright. So, this is the idea. So, which of these is going to be larger C_{db} or C_{sb} let us call this C_{sb} which is larger C_{db} or C_{sb} C_{sb} is larger because source voltage is smaller than the drain voltage. So, source to body reverse bias is going to be less than drain to body reverse bias, right and in that sense the capacitance is going to be more, right.

So, C_{sb} is going to be more than C_{db} and similarly C_{gs} is always going to be more than C_{gd} , right because the drain is at a higher potential than the source, ok. So, most of SIOX is going to come as part of C_{gs} and not as part of C_{gd} , ok. So, this was the discussion that we had in the last class and now we are going to build on this we are going to use this small signal model to analyze our common source amplifier the very first circuit that we studied the common source amplifier, then will briefly study the

common drain amplifier and then briefly study the common gate amplifier, ok. All three we are going to study and then we are also going to study the cascode after that. So, that is the agenda that is coming up.

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So, first we are going to look at the common source amplifier. So, by now you should be comfortable with the small signal analysis right I am not going to draw the biasing anymore because biasing can be done using a variety of techniques it could have been biased with a current source, biased with voltage division all kinds of things it could be, this could be part of a differential amplifier I do not know what is going on, right. This is the small signal circuit, that I have drawn I am not going to replace the MOSFET right away. In fact, I am not planning to replace the MOSFET at all, right. My strategy is that you should think about what is inside the MOSFET instead of wasting time drawing diagrams, ok. Draw this core diagram that is the MOSFET resistors small signal diagram and then that is it, right, do not bother the you know doing more and more sketches wasting time,.

So, we have this small signal circuit and the way you ordinarily analyze this is with the help of Norton equivalent right how do you do the Norton equivalent you measure the short circuit trans conductance and you measure the output impedance. So, if I measure the output impedance first let us connect v_{in} to ground, ok, v_{in} I imagine it is a ground automatically inside the MOSFET there was a g_m g_m times v_{gs} ; v_{gs} is now 0. So, that

g_m has gone away g_m times v_{bs} body is also at 0 anyway source is at 0. So, that has also gone away all that remains inside the MOSFET is r_{ds} which means that the output impedance looking in from the output is nothing but R_D in parallel with r_{ds} .

So, I am just re collecting the DC analysis all right and the next thing that you do is you also find out the short circuit trans conductance or the short circuit current. So, you apply a short circuit at the output node, apply your input and measure what is the current in the short circuit that is at the output node. So, I apply v_{in} over here ok, output is shorted to ground which means that the element R_D both sides of R_D are at ground and therefore, no current can go through R_D likewise inside of the MOSFET there is r_{ds} both sides of r_{ds} are at ground and therefore, no current can go through r_{ds} g_m anyway does not matter because body is at ground source is at ground, ok.

So, all that I have is g_m g_m times v_{in} is the current right and that current is forced to flow through the come through the short circuit. So, the short circuit current coming inside is g_m times v_{in} that is the current coming inside and if you now think of the trans conductance that is just equal g_m because the trans conductance is the current divided by v_{in} . So, v_{in} cancels out you have only g_m ok, then if you are asked what is the voltage gain the voltage gain is multiplication of the short circuit trans conductance with the output impedance basically it is a Thevenin to Norton transformation, all right.

So, the voltage gain is g_m times R_D in parallel with r_{ds} , but you have to take care of this sign over here the sign is important the current is coming in. So, the sign is going to be a minus all right, that is how you remember or if you do not want to remember it just do a transformation from Thevenin to Norton equivalent the Norton equivalent looks like this you do not have to do anything right this is g_m times v_{in} this is R_{out} , right.

Do not have to do any transformation also you just have to imagine this and therefore, the voltage over here is going to be minus $g_m v_{in} R_{out}$ which means the voltage gain is minus $g_m R_{out}$, ok. So, this is the overall plan of things this is what happens without the capacitors. Now, let us throw in the capacitors. So, first of all I have got C_{gd} between the gate and the drain I have got C_{gs} between the gate and the source I have got c_{drain} to body and body is at ground and I have got c_{source} to body source is at ground body is at ground. So, no current can go through C_{source} to body and therefore, I am not even going to draw it ok, alright. Let me draw it just to make you happy here it is C

source to body body is at ground source is at ground and therefore, this one is irrelevant, it exists, but no current can go through it is irrelevant, fine. So far so good, all right

Now, we are going to do the same two experiments, the short circuit trans conductance and the output impedance. Now, instead of calling it R_{out} we are now going to call it z_{out} because it is now going to be an output impedance, that is all, ok. So, let us first find output impedance and when I do the output impedance experiment v_{in} is going to be at ground, if v_{in} is at ground C_{gs} has no current going through it because both sides of C_{gs} are at ground alright, likewise inside the MOSFET I have got g_m and g_{mb} both are nulled out like last time like in DC.

So, inside the MOSFET all that is there now is r_{ds} that is all that is there then I have got C_{db} , C_{gd} and R_D and these are all between v_{out} and ground between v_{out} and ground I have got C_{gd} , v_{out} and ground I have got C_{db} , v_{out} and ground I have got R_D , v_{out} and ground I have got r_{ds} and therefore, the output impedance is the parallel combination of R_D r_{ds} C_{gd} C_{db} , fine and you know how to write the simplify this. No, I am sure you know how to simplify this given time given no time can you simplify this there is a trick, ok.

So, let us see what that trick is. So, very nice trick the trick is to understand that all of these, each of all right. Let us do it slowly, let us not jump the gun over here we will do it slowly, ok. So, let us re write this as R_D parallel r_{ds} in parallel with this combination, and what is this combination one by sC_{gd} in parallel with 1 by sC_{db} it is two capacitors in parallel they adopt, ok. So, this is nothing but one by sC_{gd} plus C_{db} , all right and you can place these two in parallel these two combinations in parallel and you can do the crunching, the algebraic crunching or what is easier is to do the following this is the DC quantity, ok. So, it is r that is the DC quantity divided by 1 plus sC r ok.

So, you can do the algebra you will come up with this answer, do not you worry about it. All the format always the format is going to be the DC quantity divided by 1 plus s τ typically this is going to be the typical format of things if not it is going to be like this sum DC quantity into 1 plus s τ z by 1 plus s τ pull, ok. If it does not even look like this, it is probably going to look like this and so on and so forth. So, this is the template this is how it is going to look like the expression. So, you have the expression at DC, right, at AC all of this is going to evaluate to a 1 because s is equal to 0 .

So, all these will evaluate to a 1, ok. The other quantities this is going to evaluate to 1 and DC this is going to disappear all gone, right. So, at DC it is just going to be whatever is on the top whatever is the DC parameter. So, it is the DC is stuff, all right this is the template this is how all the impedances all the s parameter all Laplace expressions are going to look like you are going to have a DC quantity, ok. So, there is a subtle difference between what you will find in control theory books and what you will find in analog circuits subtle difference.

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$$\frac{\dots}{(s+a)(s+b)(s+c)}$$

$$A \frac{(s+z_1)(s+z_2)(s+z_3)\dots}{(s+p_1)(s+p_2)(s+p_3)\dots}$$

$$(DC) \cdot \frac{(1+s/z_1)(1+s/z_2)(1+s/z_3)\dots}{(1+s/p_1)(1+s/p_2)(1+s/p_3)\dots}$$

In control theory books if you open any control theory book they are going to write it in this fashion or let us let us not write it like this s plus z 1 into s plus z 2 into s plus z 3 etcetera divided by s plus P 1 into s plus P 2 into s plus P 3, this is what you will find in the control theory books, ok. This whole thing times some random constant some constant some scaling constant this is how a transfer function is going to be written in a control theory book. Now, the same transfer function is going to be written in analog circuit book in a slightly different way, ok, the same transfer function if you ask in analog circuits person to rewrite the same transfer function then he is going to write it in this fashion, ok.

Why does the analog circuits (Refer Time: 20:50) like this format? Because the DC quantity is appearing outside the scaling constant is not some random number it is the DC quantity. So, if you plug in s equal to 0, all of these will evaluate to one and you will

be ending up with just the DC quantity. So, we always like to write we meaning analog circuits people write there Laplace transfer functions in this format this is the format for analog circuits, ok. I do not know about the control theory people why they are like the other one I really do not know, right. It is not important this is an analog circuits course we are going to stick to this as the format for our Laplace transfer functions, ok.

So, this is the format we have a bided by the format, it is always this term is always going to be one fine the constant is always going to be one when you are doing analog circuits the constant term in the Laplace transfer function is going to be a one that is it. So, R_D parallel r_{ds} this is the DC quantity divided by one plus s times a time constant which is nothing but capacitance times resistance is time alright. We all know that and we all saw that the resistance here is R_D in parallel with r_{ds} we saw that the capacitance here is C_{db} plus C_{gd} . Therefore, the expression do not have to do anything, the expression in straight away the DC quantity divided by 1 plus the time s times the time constant the time constant being R_D parallel r_{ds} times the combination of the capacitor C_{db} plus C_{gd} .

So, by inspection you can write it just like by inspection you had written this the same way you can write this, ok. You do not have to do this stuff at all, alright. Now, this is only one experiment so far the next experiment is the short circuit current.

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$$g_m v_{in} - v_{in} \cdot s C_{gd}$$

$$g_m - s C_{gd}$$

$$g_m \left(1 - \frac{s C_{gd}}{g_m} \right)$$

$$\frac{V_{out}(s)}{V_{in}(s)} = -g_m (R_D || r_{ds}) \cdot \frac{1 - s C_{gd} / g_m}{1 + s (C_{gd} + C_{db}) (R_D || r_{ds})}$$

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So, this is the experiment, you are applying v in you are going to measure the current over there and the understanding is that inside the MOSFET r_{ds} carries no current because both sides are at ground g_{mb} carries no current because body and source are at ground, right. So, all that is there inside the MOSFET is one g_m and outside the MOSFET R_D carries no current because both sides are at ground. C_{source} to body was always a irrelevant because both sides were ground source and body C_{drain} to body is also irrelevant because both sides are at ground it does not carry any current drain is at ground body is at ground. The only other thing you have is see gate to drain which is carrying a well defined amount of current this side is v in the other side is ground and you have C_{gs} and it is carrying a well defined current, but that current has no relationship with this short circuit current, it is not really effecting, it is just going over here,.

So, yes there is current through C_{gs} , but it does not matter. So, all that I have over here is C_{gd} and therefore, the current that I have drawn over here is nothing but a g_m times v_{in} , that is the current going down through the MOSFET is g_m times v_{in} , but there is additional current coming in over here which is v_{in} times sC_{gd} and there is a minus sign over here, beware be very careful. Check double check the sign what I have written is correct. This current is v_{in} times sC_{gd} the current over here is g_m times v_{in} , all right and therefore, this combination current is going to be $g_m v_{in}$ minus v_{in} times sC_{gd} check and double check this why is because in circuits normally these minus signs do not come inside expressions, ok.

So, this is an anomaly, this is not something that happens on a routine basis, ok. This minus sign usually triggers a warning it should trigger a warning saying that maybe something is wrong, let me recheck and you have to recheck over here and indeed in this particular case the minus sign happens to be correct. So, the overall trans conductance is g_m minus sC_{gd} this is the trans conductance and as I said before we do not like writing it like this, . We like writing it as the DC quantity times 1 in this case minus sC_{gd} by g_m and clearly this is a pole or a 0 ? This is a 0 , yes. This is a 0 and this 0 is in the left half plane or in the right half plane. This is in the left half plane, this 0 I am sorry yes this is a right, half plain 0 this 0 is positive 0 it is in the right half plane and this also does not normally occur.

So, normally under when things are all nice and regular circuits right you will not see zeros coming in the right half plane if at all a 0 comes it will be a left half plane 0. This is a special circuit, ok. It is a common source amplifier it is a special amplifier, ok. It happens to be your favorite amplifier, but that does not mean that it is not special it is a special circuit that is why you are getting a right half plane 0 over here fine.

So, what is the overall v_{out} by v_{in} in Laplace transform is going to be minus trans conductance times output impedance. So, minus g_m is the DC quantity R_D parallel r_{ds} was the DC output impedance times the poles and the zeros $1 - sC_{gd}$ by g_m that is coming from the trans conductance and coming from the output impedance is $1 + sC_{gate\ to\ drain}$ at the output node you are gate to node capacitance as well as drain to body capacitance and R_D parallel r_{ds} , ok.

So, this is the overall transfer function there is a right half plane 0 and there is a pole. The pole is at the r_c of the output node ok, the right half plane 0 comes because of C_{gd} , fine. This analysis is clean, there is no problem. So, when you analyze like this you will not have any problem usually here analysis is going to be correct, right. There are however, some shortcuts to do the analysis; this analysis is ok. It was quite fast, right. Do you really need a shortcut I do not I do not see the need for a short cut in this particular situation, ok. We do not need a shortcut; let us not worry about the shortcut. There are some you know people have come up with some short cut and the short cut sophisticate things a lot and they are also not accurate you would not end up with this answer when you apply those short cuts you will end up with something else and then it is going to be very hard to justify the shortcut so on and so forth.

So, let us not bother with any short cut, this analysis was quite fast so far, right. All we did we are also trying to learn. So, let us also learn how to do the correct analysis in one shot, ok. This is the correct analysis in one shot; find output impedance, find short circuit trans conductance, you are done, ok. You have found the overall transfer function. Any question so far? So, this is the analysis of our common source amplifier, you can of course, draw pole 0 plot over here a Bode plot for this, right. Should I remind you how to draw a Bode plot? Bode plot had a gain plot and a phase plot, ok. See, Bode plot is nothing but a plot of this having replacing s with $j\omega$.

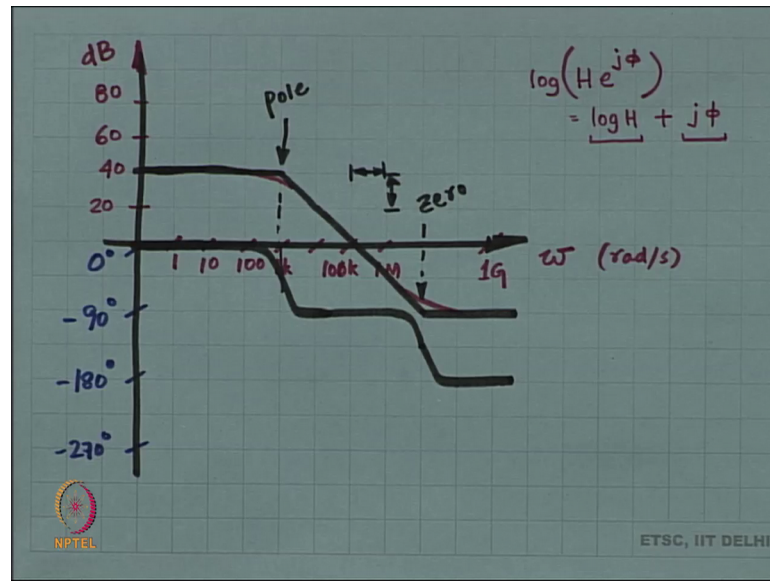
So, I replace s with $g\omega$ and I swipe ω and I plot this quantity. Now, when you try to plot this quantity you are trying to complex number, right. So, it is very hard trying to plot a complex number you can plot real part and imaginary part, but it does not make much sense to a lot of people plotting real and imaginary part. Instead as a engineers what we do is we plot the magnitude and the phase, ok.

So, when you are doing the Bode plot you always need two plots one of the magnitude, one of the phase because it is a plot of this complex number, this complex quantity with ω as the variable, all right. So, this going to be a magnitude plot, this going to be a phase plot. Now, what this gentleman Bode? Bode was one of the last great engineers, ok. He is actually a fantastic engineer from bell labs in the late nineteen thirties, and there a lot of contributions that came from Bode. The circuit design community is indebted to Bode in many ways, ok. So, this Bode plot has come from him and what he figured out is that instead of plotting just the complex number, if we plot the log of the complex number it might make sense more and at the same time it might be easier to plot, ok.

So, two things in one shot; first is, it will make even more sense. Why will it make even more sense? Because the ear hears in decibels, right you can hear a mosquito flying next to your ear when you are sleeping, you can also hear loud fireworks right next to it, ok. So, the ear has a huge dynamic range, right and the sensitivity of the ear is in the log scale. In a lot of places the log scale comes with becomes with the important. For example, in vibrations when you measure an earthquake you measure in the Richter scale which is nothing but a log scale ok. So, lot of places lot of effects come out you appreciate when you when you when you talk about that effect in the log scale. So, sound is one sound is a kind of a vibration all vibrations right, there you see you appreciate the effect of the vibration more in the log scale ok. So, likewise all communication right, electric field magnetic field all of these when you when you look at them when you appreciate them in the log scale the appreciation happens is more.

So, this is what Bode figured out that people will appreciate the graph more if instead of plotting just the complex number I plot the log of that complex number. And then the next thing that he figured out was that not only will people appreciate it more it is also easier to plot. So, this is how. So, it is just a refresher of your Bode plot.

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This is not a really material for this course. So, the y axis is going to be log of the magnitude. Let us just do a little bit of brief analysis over here. If I have a complex number let us call it $H e^{j\phi}$, ok. If I take log of this then it is going to be equal to log of H plus nothing but $j\phi$, fine. So, this quantity is the phase j times ϕ you do not have to plot the j part of it you just plot ϕ and in the other plot you are going to show the log of the magnitude. So, in one case you are going to show log of the magnitude in the other case you are going to show the phase ϕ .

Now, the log of the magnitude the decibel scale is actually 20 times log of the magnitude. So, instead of plotting just the log of the magnitude you can plot 20 times the log of the magnitude and that is the decibel scale. So, what does that mean? So, every 20 decibels is actually a factor of 10, ok. So, that is the decibel scale that every step of 20 decibels is a factor of 10. By the way this is when we are trying to plot something which has which is a ratio of two voltages, ratio of two currents, a ratio of two electric fields, ratio of two magnetic fields all right ratio of two vibration amplitudes, then you are going to use 20 times log of log to the base 10, that is a decibel.

However, when you are trying to express when you are trying to plot the ratio of two powers the power can be because of electricity in which case it is going to be voltage squared by r or it will be I squared by r or it is going to be. So, everywhere it is going to involve a square term, ok. So, either voltage squared ratios I squared ratios or amplitude

square ratios, electric field square ratios, magnetic field square ratios, right vibration amplitude square ratios, all right. So, in all of these cases you will find that there is a square term coming in whenever you are trying to look at power as opposed to the amplitude, right. In such a situation when you convert it to decibels when you convert this ratio to decibels you have to use 10 times log because the square is going to come out of the log and it is going to make the 10 or 20 it is going to make it two times and it is going to become 20 ok. So, ratio of powers is always 10 log, the ratio of amplitudes is always 20 log ok.

And, if it is not a ratio it does not come into the dB scale at all. This is the ratio of two voltages ok; two amplitudes in which case it is going to be 20 log; 20 log to the base 10 that is the idea, ok. So, this is one part the y axis is one part of the Bode plot one feature. Now, what is interesting is that the x axis also has to be a log scale. What is the x axis by the way? Omega, right; remember we replaced s with j omega and said let us plot it as a function of omega that was the entire objective. So, the x axis has to be omega, but in case of the Bode plot we are going to plot omega in the log scale which means that if this is 1 radian per second I am going to call 10 radians per second 100 radians per second 1000, 10000, 100000 no.

So, in the Bode plot every step is a factor, ok. It can be a decade like I have drawn, it could be step of 2 that is called an octave all right something nice about this octaves and decades and so on and that is what is that is what comes out in the Bode plot all right. So, this is the magnitude plot then likewise the phase plot is going to happen on the bottom side. Now, why does the phase come on the bottom side, because normally it is very hard to find the system which has phase more than 0 degrees because that kind of a system would be non causal, ok. Usually your system is going to be a causal system which means that the output is going to be delayed from the input in terms of time and that usually means that the phase is going to be negative. So, always output is always going to lag the input, right.

It is very unlikely that the output is suddenly going to start leading the input even in such a situation you are going to draw it as minus 200, 359 degrees you are not going to show it as plus 1 degree, when output is leading the input you are going to draw it as minus 359 degrees not as plus 1 degree because plus 1 degree appears as if the output knows what the input was input is going to be in future, ok. So, that is why we always draw this

in the bottom half on the negative scale, all right. There is no reason for the phase to be more than 0 degrees plain and simple.

Now, this is the setup for the Bode plot and this log of $H + j\phi$ has to be plotted in this, right. Now, it so happens that it is very easy to plot I would not to show the mathematics right now, but all I am going to tell you is that you locate the pole, right I first of all you need to understand the DC on this on this axis DC is outside the page this is not DC this is only 0.1, next 0.01, 0.001 you can keep going, right DC happens at minus infinity, ok. That is something to appreciate this is the log scale DC is far away, all right.

So, whatever is at DC that continues, that value continues till the frequency starts playing an effect, ok. So, if your DC value is 40 dB there you are it is a straight line till frequency is the free the capacitors start playing a role till the pole or the 0 starts playing a role, ok. Now, what is going to happen at the pole is nothing much the slope of this curve is going to change by minus 20 dB per decade that is all that happens at a pole and all that happens at a 0 so, this is a refresher for the Bode lot right. So, I am not going to discuss the maths, why it happens. It is actually very easy to see why it happens, you just lot out log of a genuine figure it out, but what we are going to do is we are only going to say right now, that at the first pole the slope of this axis this graph changes by minus 20 dB per decade at a 0 the slope of this line changes by plus 20 dB per decade what does decade mean decade is that this unit size you know factor of 10, ok.

So, if the slope changes by 20 dB s let us say your pole is at 1 kilo hertz so, it is flat. So, not 1 kilo hertz 1 kilo radian per second, it is flat till one kilo radian per second at 1 kilo radian per second the slope of this changes by minus 20 dB per decade and minus 20 dB per decade on this graph looks like this ok. So, this is 20 dB this is 20 dB and this great side is 1 decade over here. So, from a slope of 0, I went was slop of minus 20 dB per decade if another pole comes then it is going to the slope is going to decrease to minus 40 dB per decade and so on and so forth. Now, 0 comes right.

So, our transfer function has a pole and also a 0 which of these is going to come first the pole is going to come first because this time constant is much larger than the other one this is $Cgd + Cdb$, ok. So, this capacitance certainly larger than Cgd and 1 by gm is a small resistance compared to R_D parallel r_{ds} which means this is large this is large

this time constant is much larger which means in frequency it is a smaller frequency. So, this pole frequency is smaller than the 0 frequency. So, the pole arrives first and then sooner or later the 0 comes and when the 0 comes the slope increases by 20 dB per decade all right.

Now, when you are doing these log plots and so on things are not going to be such a piecewise linear you know solid straight lines, ok, this is going to be some smooth curve, right. So, all you now have to do is you have to make this curve appear smooth and your done. So, at the corners you have to cut a little bit and the amount to cut is also there you have to cut by 3 dBs at the corners right all of this is part of the Bode plot theory, right, how much to cut the corners by. So, you have to cut the corners and then smoothen the line by 3 dB, all right. Next we also have to plot the phase and the phase plot also happens to be something very easy at DC the phase is going to be 0, ok.

So, we are not going to worry about DC we are going to always start from DC which is at phase 0 and then at the first pole after the first pole you going to get a phase adjustment by minus 90 degrees at every pole the phase is going to drop by 90 degrees, all right this is the idea. Every pole comes one pole 90 degrees, another pole another 90 degrees. So, if a pole arrives then you are going to get a phase delay of 90 degrees phase lag of 90 degrees, all right and again you have to make it a little smooth right it is going to pass through for minus 45 degrees at that precise point and how much to smooth by and so on all of these are you know plus minus 1 decade you have to smooth it by plus minus 1 decade around the pole, ok.

So, this is the idea now what happens at 0 just like in case of a pole the phase goes down by 90 degrees ordinarily in case of a 0 the phase is going to go up by 90 degrees. The only problem is we are not in an ordinary situation, we have a right half plane 0 and in a right half plane 0 phase goes down by 90 degrees, ok. Ordinarily phase goes up by 90 degrees it is opposite of the pole, but in a right half plane 0 phase also goes down by 90 degrees just like a pole. So, this is our Bode plot, ok. Once again at this precise point at the 0 frequency I have adjust made an adjustment of only 45 degrees, ok, not the full 90. The full 90 spreads around over a decade, alright.

So, this is how you draw the Bode plot the principal of drawing the Bode plot remains the same right whatever transfer function you are trying to plot this 40 dB comes from

the DC part, right $g_m R_d$ parallel r_{ds} that gives you this number, right then the pole frequency is 1 by the time constant the 0 frequency is 1 by this time constant.

So, we could not accomplish what we plan to do. We had planned to do common source, common drain, common gate right. Unfortunately, all we have done is just the common source, but that is ok. Because, we also spend some time looking at how to plot we spend some time with the how to what is the template transfer function and so on and so forth, it took a little time the first you know the first time you do it takes a little time. The next few circuits are going to be much faster and easier, alright.

So, let us stop here and we will continue again.

Thank you.