Analog Electronic Circuits
Prof. Shouribrata Chatterjee
Department of Electrical Engineering
Indian Institute of Technology, Delhi

Lecture - 25
Capacitance in MOS devices

Welcome back to analog electronics, today's lecture 25, and we are going to switch gears from what we have been discussing in the past. And we are going to go back to the very basics, in fact, we are going to go back to single transistor amplifiers once again. But this time we are also going to talk about capacitance. In fact, main discussion of ours will be focused on the Capacitances in MOS Devices, ok.

So, to start with let us briefly look at the MOS device. I know this is not a course in MOSFETs, right.

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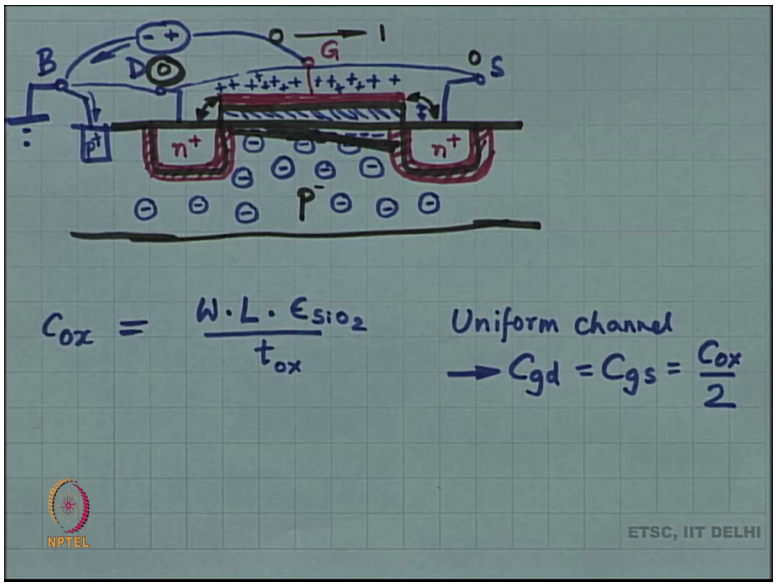

However, since we are discussing the MOSFET, since we are going to use the MOSFET we need to understand how the MOSFET works. And so, far we have had only a very crude understanding of how the MOSFET works. So, we have got a P types substrate. And on the P types substrate, let us call this P minus slightly doped P types substrate on top of this P type substrate, you are going to set up some oxide. This oxide is insulating, and further on top of that you are going to have polysilicon, which is the conducting gate, ok.

So, polysilicon is a conductor, not a very good conductor, but conductor all right. So, this is the first step, right, you have got a lightly doped P minus substrate on top of that you have set up a polysilicon gate. Then what you do is you implant n plus, right, and n plus goes in to the areas where which are exposed. So, you get n plus in the exposed area is not underneath the gate. Underneath the gate it remains as P minus, and these areas this part will be the drain, the other one will be the source, ok. The bottom the rest of the devices the body the P minus area is the body, and the way body is taken out, everything comes out on top.

So, you in plan P plus over here to make a strong connection to P minus and you take out body, ok. So, P plus connects well with P minus, n plus does not connect with P minus at all, a depletion region is form between nmp right all the electrons diffuse and fall in to the holes. Electrons from the D side migrate to the P minus side they diffuse and then they fall in to the holes. So, that is the depletion, and then again some holes from the P minus side migrate with the help of diffusion to the m plus side and they create holes for the electrons to combined with.

So, some electrons from the m plus side and some holes from the P minus side they combined with each other, and this is a space charge region it is charged up right; however, it might be charged up, but there are no carriers there, ok. When I say no carriers it means that, it is an insulator right, because the property of a conductor is that there are charge carriers in the conductor. Whereas, the property of an insulator is that there is nothing that can carry charge. So, if there are no free electrons, no free volts to move around, then this region is going to behave like an insulator. So, at every pn junction, you will naturally have an insulator, this insulator is called the depletion region, ok.

So, this is the initial set up, now you start applying voltages ok. So, we have discussed body long time back, and if you it is an n channel device then the body is going to be connected to 0 volts. If it had been a P channel device then the body, you would have connected the body to the maximum power supply. So, be take care of the body first then so, the entire substrate is now grounded. Now that the substrate is grounded, let us talk about gate drain and source. So, let us connect the gate or other let us do the gate later on, let us connect drain and source, also let us say we connect them to 0 volts both of them.

So, right now I have connected drain and source both to 0 volts. And then what I am planning to do is, I am going to connect the gate first to 0 volts, and then slowly I am going to increase the gate voltage. From 0 volts all the way I will increase it to Vt plus something, something more than Vt. So, let us say Vt is half of volt, I will increase it all the way to 1 volt, ok. So, 2 times Vt, this is the plan. So, body is at 0 volts drain and source are also at 0 volts, and I am going to slowly increase the voltage at the gate from 0 volts to 1 volt, and I know that the Vt of this device is 0.5, and let us see what happens to the (Refer Time: 07:14).

So, first when there when the voltage is 0 volts there are no charges anywhere, ok. Drain is at 0, gate is at 0, source is at 0 everything is clean, alright. Now I increase the voltage at the gate a little bit, what is going to happen? So, remember that there are a lot of holes in the substrate, ok, there are holes in the substrate, because a substrate is doped P minus, there are these volts. If I increase the voltage at the gate, then naturally charge is going to come on to the gate. Some plus charges will come on to the gate, having increase the little bit, ok. Now if I increase the voltage at the gate, a likewise, if I have got plus charge on the gate, a likewise minus charge has to come in somewhere opposite right. So, 4 pieces of plus charge on the gate, need 4 pieces of minus charge somewhere.

And what is going to happen is so this is my voltage source, right. So, B D and S are all connected together, right this is the voltage source between B and G, and this is the voltage source that you have slightly increased. So, the voltage source takes out some electrons from the gate and lives plus charges on the gate. And then it is going to put all those electrons into this terminal, which is B S and S, right? D and S are already full of electrons ok; however, B is full of holes. So, these coming inside B right, the electrons go inside B, because they would like to combine with holes.

So, they go inside B, combined with the holes and which holes will the combined with? So, the first holes that they will combine with are the once closest to the surface, ok. So, this start always from the top, because the electric field is the largest over here, all right. So, the electric field is the largest so, they have to go closest to the surface, as close as possible to the surface. And then they combined with those holes, right when they combined with the hole, the hole is no longer charge mutual, it now has a extra electron, and it has satisfied all valance requirement.

Therefore, it is no longer of mobile charge, and that is indicated in this fashion you put a circle around the minus. It is an extra minus and you put an circle around it to indicate at this can no longer move. It is not a free charge free minus carrier, all right. Now I increase the voltage at the gate by another 10 mili volts, ok. I get a few more plus charges here, and those plus charges again need to come and combined with some more holes that are there in the substitute, ok.

So, little by little, as I keep increasing the voltage at the gate, right, little by little the charges in the substrate, sorry the holes in the substrate get filled up, little by little, till all of them get filled up, ok. So, little by little all of them get filled up, all the holes in the substrate, now the substrate no longer has any mobile carriers, no more holes available, all right? Now what is going to happen? Now the next electron that comes in to this terminal B D S, right, what is it going to do? It has no more holes to fill up, right, it just has to go right, it will come in the next electron that come in that comes in.

So, this is now perfectly balance 1, 2, 3, 6, 9, 11, 13, ok. So, I have got 13 plus charges, 13 minus charges. Now in the 14th one comes, what is going to happen to it? Where is it go into go, it is going to coming inside, and then it is going to go and reside at the surface as an electron, it has no more hole to fill up, it just comes in and sits right at the surface, all right. And hence 4th for every electron that comes in, every positive charge that you set up on the gate, it comes in and sits at the surface, the electrons sits there as is, ok, as close to the surface as possible. Because you know in class 11, or in class 12, we have studied electro statics, if you place charge on a conductor it always comes to the surface, right.

So, likewise you have got you have placed some charge over here, these are mobile carrier so, they are going to go and sit right at the surface as far as possible they can go, right. They have no other place to go, they will go at the surface; this is called the channel ok. So, got the way I am projecting the MOSFET this is are other crude way of projecting it, I am not doing in math's, I am just projecting the MOSFET, I am just showing you the action the behavior of the MOSFET in a crude hand waving manner, right; however, this is this is the true, this is not very far from the truth whatever I am talking about.

So, you have a few things going on here. You have a situation where initially it the electrons come in and occupy the holes, ok. Till the holes can be occupied, here voltage at the gate is less than Vt, ok, at the point that you start having electrons come and making a channel on the surface, that point is Vt, that voltage that you required to start creating a channel that is called Vt, right, actually Vt has some other proper definition, but you can think of it this way also.

Then a beyond Vt every electron that you put into the substrate body drain source combination, every electron that you put in it go straight and sits at the channel, it founds channels, it proves the channels strength, all right. And sooner or later a channel is form between the drain and the source, right, let us say you increase the gate voltage even more right a channel is found between the drain and the source, and the switch is connected, drain and source now are connected to each other with the help of a channel, ok.

So, this is the on state of the MOSFET. So far so good, now what do you see? First thing you see other few capacitors, over here, there are the few capacitors. This is capacitor between the gate and the channel, why? Because there is charge on the gate, then there is an insulator, then there is a charge on the channel, what will this capacitance B? This capacitance will be a epsilon by D, right? A is W times L, width times L is a. So, this capacitance is called C ox oxide capacitance is a epsilon by D, a is W times L. Epsilon is; epsilon of which material? Silicon dioxide, right, because the material in between this oxide material is SiO 2 a epsilon by D, where D is the thickness of the oxide material, fine? This should be straight forward so, there exist the capacitors. This capacitance is shared between the drain and the source, because it is forming a connection between the 2 sites, drain and source.

So, if you try to look at the individual capacitance as between gate and drain and between gate and source, right, it is hard to see them individually. But if you do try to see them individually, then the some of the capacitance between gate and drain and gate and source will be equal to C ox, because the channel is just a connection between the drain and source right. So, the capacitances is actually between the gate and the channel, right. If someone says what is the capacitance between gate and source, then you can only say that the capacitance between gate and source, plus the capacitance between gate and drain is equal to C ox, ok. That is all you can claim right now, right. In fact, with the

shape of the channel as it is, right the channel right now is uniform, because drain is at 0 volts, source is also at 0 volts both are at 0 volts. So, the channel is uniform right.

So, there is no reason for the drain capacitance to be more or less than the source capacitance; which means that with the set-up, right now the gate to drain capacitance is equal to the gate to source capacitance, and that is equal to C ox by 2. So, uniform channel, this implies C gate to drain is equal to C gate to source is equal to C ox by 2, fine? Now what we are going to do is, let us look at drain and body. If you look at drain and body, in between right so, drain is full of electrons, right it is full of electrons body, all right. Let us assume the body is not depleted because of Vt, if the body is not depleted of V t it is still has some holes, right, there are some holes in the body, right so, you have got electrons in the drain.

So, the drain is a conductor you have got some depletion region, because of the P n junction between drain and body. And then you have probably got some more holes in the body. So, you have got conductor insulator and then again conductor, right. Now what this implies is that this is going to look like a capacitor, whenever you have conductor insulator conductor it is a capacitor, ok, any depletion region is an insulator, any other doped semi-conductor region is a conductor, right or metal it is a conductor.

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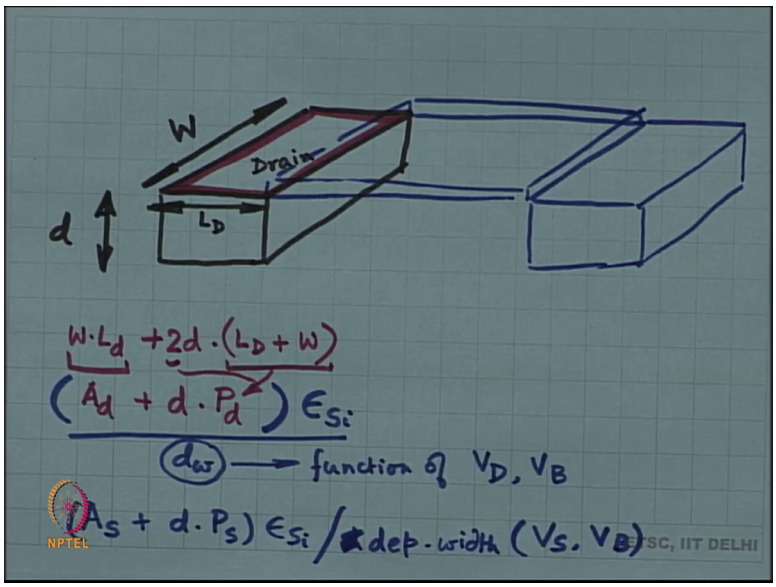

So, conductor insulator conductor means automatically that you have got a capacitor over there. So, let us take a brief look, let us draw this in 3 D. So, suppose this is the

drain, this is the width of the transistor of the MOSFET, and then the gate comes over here right and then the source comes over here.

So, let us not look at the blue portion at all, let us only focus on the drain region, ok. Let us not look at the rest of this staff, only the drain region it has a width, and let us say this has a depth. And let us say it has a length L D, all right, now when we talk about this depletion region capacitance, ok. Where is it going to be? It is going to be on all sides of drain except for the top side, right. The top side is exposed to the outside, right all the other sides there are 5 more sides, right. In this rectangular a what is called? Rectangular parallel o piped right in this structure there are 5 more sides, right all those 5 sides are exposed to the body, right the top is exposed to the outside.

So, the area of those 5 sides have to be taken into account, right all of those will form the depletion region, that is your pn junction, ok. So, when you try to calculate a epsilon by D in this particular capacitance, a is the area of these 5 sides taken together, ok. So, what is that area of these 5 sides? You have got W times Ld that is the bottom. Plus, so, bottom side is non then the 4 walls. The 4 walls are D times Ld for the front, Ld for the back, W for the inside and W for the outside, fine? This is the complete area of the 5 sides taken together.

So, W times Ld, we are going to call this Ad, right where Ad stands for the area of the drain, 2 times Ld plus W we are going to call this Pd, where Pd stands for the perimeter of the drain. This perimeter, this perimeter is 2 times Ld plus 2 times W fine? So, the size of the wall the complete area of these 5 sides is Ad which is the area of the drain, plus depth times the perimeter of the drain. And I am not going to count the top side, because the top side is expose to the outside not to the pn junction, there is no pn junction over there.

So, when you do here a epsilon by D calculation, this is A, this whole thing is A. And then we have to account for epsilon and here what epsilon is this what is the material? Silicon, by D is the depletion width, right? Now the depletion width is a function of the bias voltages, it is a pn junction right if I apply 0 volts and 0 volts I get some depletion width, right depending on the doping and so on and so forth, but then if, I increase voltage on one side depletion width changes if I reverse bias depletion width increases, if I forward bias depletion width decreases, right, you remember all of this.

So, this depletion width is a function of voltages, ok. So, function of the absolute voltage, at the drain and the absolute voltage at the body; however, you have got a capacitance over there between drain and body. Now exactly the same thing is going to happen to the source. Exactly the same thing, it is something happens to the drain something very similar is going to happen to the source. And we are going to call it the capacitance is going to be area of source plus depth times perimeter of source, the whole thing times epsilon silicon divided by depletion width again, which is a function of VS and VB, fine.

So, we have found that there is exists the capacitance between gate and a channel. So, this capacitance between gate and a channel, there is also capacitance between drain and body, as well as source and body. The capacitance between gate and channel is shared between gate and drain and gate and source. This sharing is equal in the case of a uniform channel, ok, each gates only 50 percent of the share the drain and the source, if the channel is uniform. Now if the channel is not uniform what is going to happen? They are not going to get 50 percent anymore, and then there is going to be a struggle, who is going to get more who is going to get less, right, this is going to be some bargain. Now right now we have applied 0 volts and 0 volts at the drain and at the source so, let us change things, ok.

So, what we are going do now is you are going to increase the drain voltage. So, let us make let us start increasing the drain voltage. What is going to happen? When I increase the drain voltage, then electrons that are on the drain side are going to rush in to the drain, because they like the high voltage at the drain. So, these electrons over here are going to get sucked out into the drain, then I am starting to increase the voltage at the drain. And if the electrons are going to get otherwise, they are going to crowed towards the source.

So, there will be more electrons on the source side, less electrons on the drain side, because if there is an electron on the drain side it has no reason to sitting there idling there, it should go into the drain because that has a higher voltage, ok. So, what happens is the way we see it is that the channel tilts towards the source. So, the shape of the channel is now tilted towards the source.

It is heavier towards the source lighter towards the drain, ok. And this tilting effect keeps happening till a point where the channel gets pinched t off you heard of pinch off, right. The channel gets pinched off so, the tilting tilts more and more and more, till if you are at the drain then there is no reason for you to be there you immediately zip across from the drain, right, you zip into the drain right. So, there is no channel per say in the drain, if you place a electron over there immediately it is zips right across, ok.

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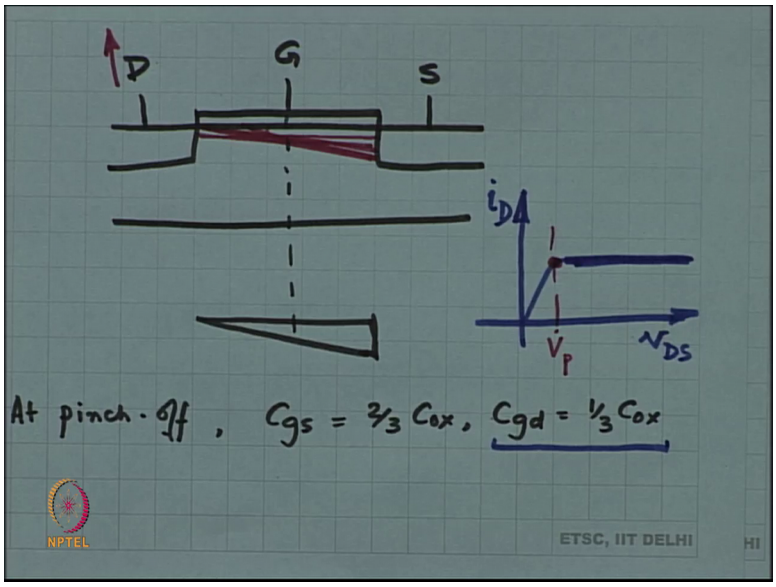

So, that is called pinch off so, at pinch off the channel becomes smaller. So, the shape of the channel, it is make a fresh drawing. So, this is the gate, drain, source right, so, I am increasing the voltage at the drain. So, initially the channel was uniform, then the channel started tilting right, tilting even more, tilting even more, at pinch off it is just here, right. Beyond pinch off the channel tilts so much to the source that there is nothing at the drain, ok.

So, there is really no channel at the drain, but if you place a charge over there, immediately it will zip across, all right, is this understood? Fine, now what; that means is, if you do a calculation, how does the split between gate to drain capacitance and gate to source capacitance work out. So, you have to integrate the number of charges, right.

So, we draw some arbitrary 50-50 line and then find the center of gravity, right you can think of it that waits now looking like a triangle, right, can do your geometry, and then what you are going to end up with is something like a one third two-thirds ratio. Does

not look exactly like that in this picture, but what we normally you know short thumb rule is that at pinch off, C gate to source is two-third of C ox, C gate drain is one third of C ox, ok. This is our thumb rule, off course you have to do a lot of work to arrive at this, but this is sort of a thumb rule, that we use. In any case the channel keeps tilting depending on the voltages that you have applied.

So, there is nothing sacrosanct about this two-third and 1 third. However, when we talk about analog circuits, we always operate beyond pinch off. In the MOSFET curve, in the iD VDS curve, where are V? We are always biased in this flat region, ok, drain to source voltage drain to source voltage is always such that is so high in that we are in the flat region, always that was our thumb rule from day 1, right we said that we have to have a drain to source voltage.

So, high that we are in the flat region, the flat region is very important to us, ok. Automatically, that means, that we are pin beyond pinch off, because pinch off is this point, right. So, we are always beyond pinch off, which means that for us the large as Cgd that we will see is one third C ox. Cgd is always going to be smaller than one third C ox. It depends on the voltage, all right, when it certainly going to be smaller than one third C ox, as long as we are in the flat region of the MOSFET, is this ok? These more or less understood, all right, now we have one more effect to were wary about, this is the last one.

So, this is called overlap, this last effect is called overlap. So, the problem is that even without all these charges, here and there, there would be some overlap possibly, some overlap between the gate and the drain. Little bit of the drain might come underneath the gate, like defuse underneath the gate, actually we never no for sure, all right.

It could also be that there is some fringe capacitance between the gate and the drain. And there would be some fringe capacitance between the gate and the source, right? This is something intrinsic to the structure of the MOSFET, this has nothing to do with voltages, and this an act, right. These are not changing varying capacitors right these are static capacitors, either because of fringing between fringe electric field between gate and drain gate and source or because of actual physical overlap.

So, maybe they was some n plus defuse, defused into the P minus some more, you know, it was not. So, the geometry was not so nice. May be some got defused underneath the

gate, right, maybe it was wider then you anticipated, in which case you will get some overlap between the gate and drain, some overlap between the gate and source fine. So, this causes some intrinsic capacitance between gate and drain and between gate and source.

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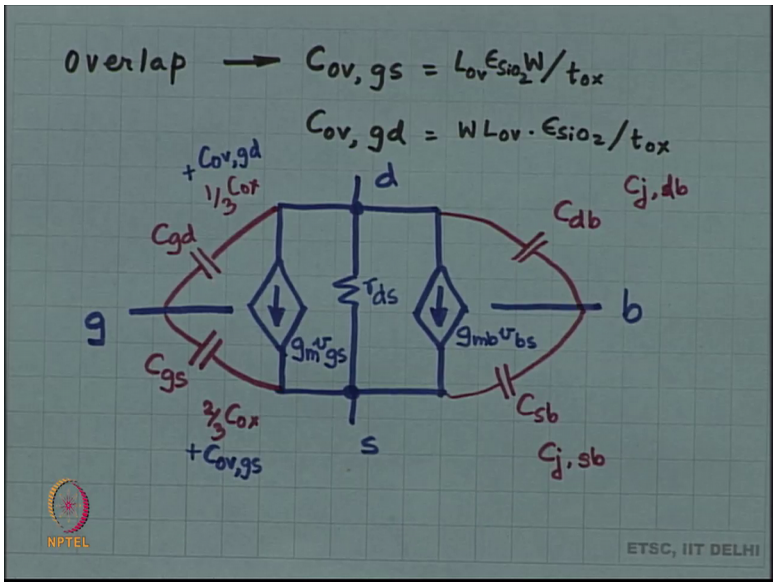

So, we called this overlap, could be because of actual overlap, it could also be because of fringe.

So, if got overlap capacitance between gate source, overlap capacitance between gate and drain, and what is this proportional to? What would the overlap be proportional to? Would it be proportional to W, it will be proportional to W; obviously, because it has to be the area of the overlap, and the area is proportional to W it would also be inversely proportional to the thickness of the gate oxide, all right. There has we do not know so, it is proportional to W, it is inversely proportional to t ox, it is proportional to epsilon silicon dioxide. And then there is going to be some unknown factor over here, which we are going to call L overlap.

So, L overlap times W gives you the area of the overlap, this need not be overlap actually this could be fringe also, we are just calling it overlap, L overlap times W is the area overlap that divided by t ox, is the t ox is thickness times epsilon silicon dioxide, gives you the overlap capacitance between gate and source, and between gate and drain gate, and drain there is no reason for it not to be identical. So, it will be exactly the same, fine.

Great, now that we understand the that MOSFET has all these capacitors, what is the model for the MOSFET going to look like.

So, our earlier small signal model for the MOSFET, look like this. So, this is what we had earlier, ok, we had a voltage controlled current source, gm times vgs, instant with a resistance between drain and source, and instant with another voltage controlled current source gmb times Vbs, ok. So, this is the body effect, this is a the slop in the flat region, rds is the slop in the flat region, it is coming from things like channel length modulation and so on right.

We do not need to know, why it is there it is there, and then I gm times vgs is they actual trans conductance of the MOSFET, ok. Now we have a number of capacitors, first we have C ox. C ox is shared between gate drain and gate to source. It is actually gate to channel right, but there is no channel terminal unfortunately. So, we have to draw it as shared between gate to drain and gate to source, ok.

So, this is C ox, this sharing could be uniform that is 50 50 sharing, if drain and source are at the same voltage, right. If drain and source are at the same voltage, then they are indistinguishable which means that they sharing between Cgd and Cgs will be 50 50, because they are in indistinguishable. However, if the sharing is unequal, that is if the voltages voltage at the drain is higher than the voltage at the source.

Other ways never going to happen, voltage at the source will never be higher than the voltage at the drain, because then you are going to start calling the source as the drain that is all, ok. So, MOSFET is a symmetric device, whichever voltage is higher you call it the drain. So, if the voltage at the drain is higher than the higher the source. Then the split between Cgd, and Cgs is no longer 50 50. At pinch off it is one third two-third that is Cgd is one third of C ox, Cgs is two-third of C ox at pinch off. And in analog circuits we are usually going to operate beyond pinch off, which means that Cgd is typically going to be smaller than one third of C ox.

So, bench mark is one third C ox, and bench mark for Cgs is two-third C ox, typically this is going to be larger, Cgs is going to be larger Cgd is going to be smaller than this then these 2 numbers, fine? Then Cgs also has some overlap, because of fringe or actual overlap so, Cgs also includes C overlap, fine.

So, this is Cgs and Cgd are done, and now there are 2 more capacitors one between drain and body, a depletion capacitance and a depletion capacitance between source and body. So, we call it so, this is actually C junction between source and body, and this is actually C junction sorry between drain and body. This is C junction between source and body, fine? These 2 capacitors also change with voltage, right, different voltages at source and drain will change, then if I increase the voltage at the source, body is at ground, if I increase the voltage at the source, what is going to happen? Source is n type material, body is P type if I increase at n type, then the P n junctions is more reverse biased, when it is reverse biased, the depletion width is going to increase. If the depletion width increases then the junction capacitance is going to decrease, all right.

So, this is commonly understood, if I increase the voltage at drain the junction capacitance is going to go down, if I decrease the voltage at the drain junction capacitance is going to go up. Like, the same thing with the source, if I increase voltage at source, junction capacitance is going to go down. If I decrease voltage at source junction capacitance is going to go up.

And all of this can be workout from the exact pn junction formulation; I recommend that you check it up once at least, what that formulation is that is your homework do checkup what is the pn junction formulation, all right? This is fine any other capacitance that we are missing? Could there be a capacitance between drain and source? Look there are there are 4 terminals ok. And you can always think of 4 C 2 a capacitor needs 2 terminals, right? Choose any 2 terminals right we are chosen gate and source done gate, and drain done drain and body done source and body done, right? The only 2 remaining are gate and body and drain and source.

So, could there D a capacitance between drain and source? And the typical answer is no, the reason why is because when the MOSFET is working when there is a channel between the drain and source. And that short circuit, right, there is a channel between drain and source full of electrons, there is no structure which has a conductor insulator conductor there is no insulator between drain and source, these actually a vire between drain and source, ok. So, there is no reason for it to have any capacitance. What about between gate and body? Gate and body could actually have a capacitance, ok. So, gate is a conductor then there is an insulator, then there is a body which is a huge P minus block of material and tip P minus is a conductor. So, you have got conductor insulator

conductor you have got that natural structure; however, as you increase the voltage at the gate, the conductor is depleted of all it is carriers, right.

So, the carriers go further and further away from the conductor from the from the gate, right. So, the thickness of this of the insulator is not just this much, it is the center of gravity of the carriers in the P minus, right? Now the carriers as they keep filling up as the holes keep filling up, the cg of the holes the center of gravity of the holes keep shifting downwards, further and further away from the gate. And the gate to body capacitance rapidly diminutions, right. So, there is actually a gate to body capacitance, but for all practical purposes, we do not need to wary about, it is very small. Because the body is far away from the gate, the conducting part of the body is far away from the gate, so, we do not have to wary about it.

However, if the device is off, ok, if the device is completely off, then there the gate to body capacitance actually is prominent; significant there is a significant gate to body capacitance, if the device is totally off; however, as soon as you start applying some gate voltage, right, the gate to body capacitance rapidly goes down, fine? So, for us in analog circuits where gate voltages is going to be something significant gate to body capacitance is not something that we are going to wary about right away, ok. It actually exists, but not at the movement, at the movement we are going to ignore gate to body capacitance, because a it does not matter fine.

So, from now onwards, this is our model for the MOSFET, the one on this picture, right you have got gm, rds, gmb and then you have got Cgs, Cgd, Cdb and Csb. This is going to be our model for the MOSFET, right? At D see the model for the MOSFET is just 3 elements; however, as you increase frequency, this becomes the model for the MOSFET, if you go at very high frequency, then you have to start taking into account all these other small things, that you did not take into account.

For example, in rf so, if you are going to wary about very, very high frequency is 20 gigahertz, ok. Not even 20 gigahertz, even a 2 gigahertz, right that is going to be called rf. So, at ready of frequencies you are going to start varying about other small niggling things. Like for example, the drain has a contract registers, you going to put a little extra resistance over here. The source has a contact registers, the gate is a dis has a distributed contact resistance. So, you are going to distribute some resistance, and then there will be

rc, right, it is no longer just C, it is going to be rc distributed rc, ok. Then you are going to start saying that o, the rds the channel also has some inductance, because it is a very thin wire.

So, you are going to put some inductance since series over here. So, all these all these things are going into be modeled, these are going to come into the model, when you are going to talk about very high frequencies? For example, 2 gigahertz 20, gigahertz, 100 gigahertz, then you have going to put an inductor in the channel, going to put contract resistances on all sides, the gate is going to be a distributed contact resistance. So, rc, rc, rc you are going to distribute the capacitance the resistance all over the place, all these other complications will come in to the model. This is our model for medium frequencies. So, for 100s of megahertz this is going to surface for example.

So, let us stop here, today we have discussed capacitance in the MOSFET, we have found out gate to drain gate to source capacitance, we have found out overlap as well as oxide capacitance, then we have looked at drain to body, source to body capacitance, because of the junction, right. The junction area is area of the source plus perimeter of the source times the depth. So, you do not really need to know, the individual sides, all you need to know is the area as well as the perimeter, and the depth, ok.

So, let us stop here. And we will start with our circuits that use this model using this model. We will analyze our circuits from the next class.

Thank you.