Analog Electronic Circuits
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Lecture - 21
Diff. Cascode amplifier, two stage amplifiers

Welcome back, to Analog Electronic Circuits and today's lecture number – 21. We are going to discuss the cascode differential amplifier as well as two stage amplifiers. This is stuff that we have learned in the single ended dwelt, but now we are going to make differential cascode amplifiers as opposed to single ended.

So, let me actually modify the title: Differential Cascode Amplifier and Two Stage Amplifiers, because you have already we have already done the single ended cascode amplifiers once.

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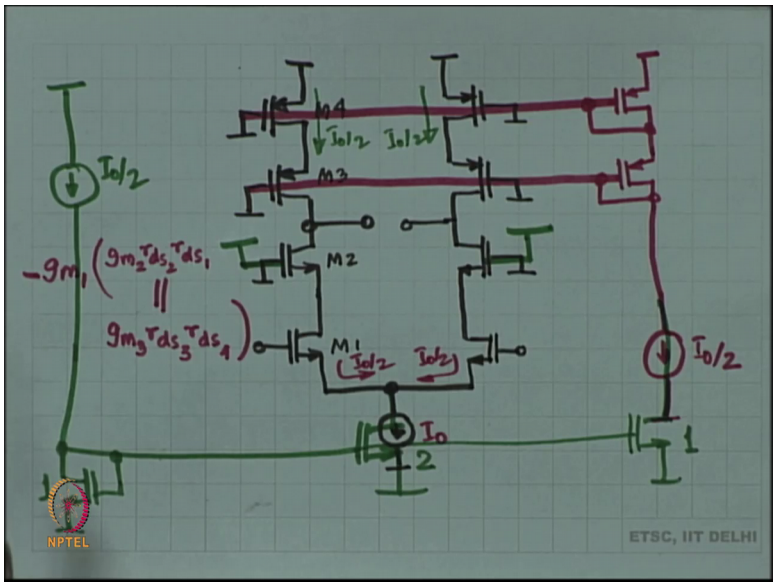

And then, yesterday, in the last class we were working on this differential cascode amplifier we said that the small signal circuit is just like the small signal differential mode half circuit is just like the regular cascode amplifier. In fact, it has to be the same, right that is the entire point, ok.

It has to look like this point is ground, but I am not marking in ground right now, because I am just going to change it, right. This is ground in the small signal half circuit, ok. This

is the regular cascode amplifier you apply your signal here you get g m times the signal as the current this signal tries to. So, we are looking at short circuit current, right. So, in the short circuit current experiment we have shorter the output you applied voltage here that created g m times the current this g m times the current is trying to split between r ds and between and what you see looking into the source.

Now, what do you see looking in to the source? You see 1 over the g m of this devise one over g m of this device is a low impedance r ds of the bottom device is a high impedance which means that affectively almost all of the current that was created by this voltage that is g m times input voltage is going to go into the source. And therefore, into the short circuit. So, the short circuit current is almost equal to g m times v in and if you want to figure out exactly what it is then you have to work out the current division ratio that is the current division between r ds and 1 by g m in parallel with r ds, right of the second transistor.

So, this current division you work out and that is the ratio by which g m is going to be reduced slightly. So, affectively the short circuit trans conductance is nothing but g m second experiment is output impedance when you look in from the output you see you can look upwards you can look downwards. So, it is the up resistance in parallel with the down resistance. The up portion of the resistance is intrinsic gain of this MOSFET times r ds of the second one plus r ds of the first one, ok, that is the up resistance and the down resistance is nothing but intrinsic gain of this MOSFET times r ds of the second one plus r ds of the second one plus r ds of the first one.

So, this is generally going to be a large impedance you can approximate it as the intrinsic gain of this device times r ds in parallel with intrinsic gain of this device times r ds, ok. So, you can approximate it and therefore, your gain your voltage gain is effectively. So, now, let us so, if you want to work out the approximate voltage gain it is nothing but g m 1 is the trans conductance approximately and the output impedance is g m 2, r ds 2 times r ds 1 approximately in parallel with g m 3 r ds 3 times r ds 4 ok. So, this is there will be a minus sign because the short circuit current is coming backwards.

So, this is affectively the small signal voltage gain. Now, this is the small signal voltage gain of the differential mod half circuit. So, therefore, what is the complete circuit the complete circuit probably can look like this? These are the complete circuit is going to

look like. Any questions over here? ok. So, one question is that why am I not connecting these two together, they are the can be connected you can do whatever you want is just one of the many possibilities you can do, you can place a current source in between these two. Also, it makes no difference, ok. Actually you cannot pull current through gates, but anyway, you can do whatever other things fancy things you like, no problem any other question? You can be creative, any other question?

So, be creative you can put a current source on the top also if you want. No problems, alright. Now, this is still the small signal picture you are going to apply we in positive over here we in negative over here in the small signal this is still the small signal picture and now, you have to incorporate the operating point conditions. How will you incorporate the operating point? I mean are you going to connect these two ground actually? No right? Here going into connected to just right voltage such that half of these current flows through it ok.

So, in other words what you are going to do is going to connect these gates together you going to assume I naught by 2 is coming this way I naught by 2 is coming this way, this is I naught and that means, that this get voltage has to be just write such that the PMOS current is I naught by 2, right which means that you probably are going to use something like this, fine. Now, this is this is ok, I have not yet connected this portion of this is a straight line and this is this is I mean imagine this to be connected.

Now, the biasing of these devices is done. What about m 3? Are you going to ground? It is to ground, but ground is not optimal right. Ground is not the optimal voltage for example, you could have done a Wilson current mirror you could have done modified Wilson current mirror you could have done a something more optimal than the Wilson current mirror ok, less accurate, but more optimal you can do all kinds of those things. So, let us just imagine Wilson for now in which case this is what is there now I am drawn the full line, ok.

So, both of these voltages they are not really ground they are some voltage which is created by a current source, ok. These two current sources have to be matched now, right. If this is I naught this needs to be I naught by 2. How will you do that? this is also going to come from some reference current source let us say I naught by 2 and then you are

going to mirror it with the MOSFET and this is going to be a size I am sorry, what did I do object ok.

So, we have got a mirror over here this is going to be of size 2 2 x of this size. So, that if this is I naught by 2 then this is double. So, I naught I am this is the same, ok, done what about these two? These two nodes what should that be that can be anything actually it can be anything as long as it is larger than a certain value right, but then you can be optimal. So, that you get the maximum possible swing over here at the output.

So, we can try to optimize once again you know you have to work out what is the input common mode voltage. So, given an input common mode voltage then only you have to set that for example, ok. So, for now for example, this could be VDD this is going to work no problem VDD is perfectly acceptable. Why is VDD acceptable, ok? Let us let us draw it up, let us draw up this entire thing on the next page on a clean slate and let us you know take some numbers in analyze the circuit. So, I am going to draw up of the whole thing ok.

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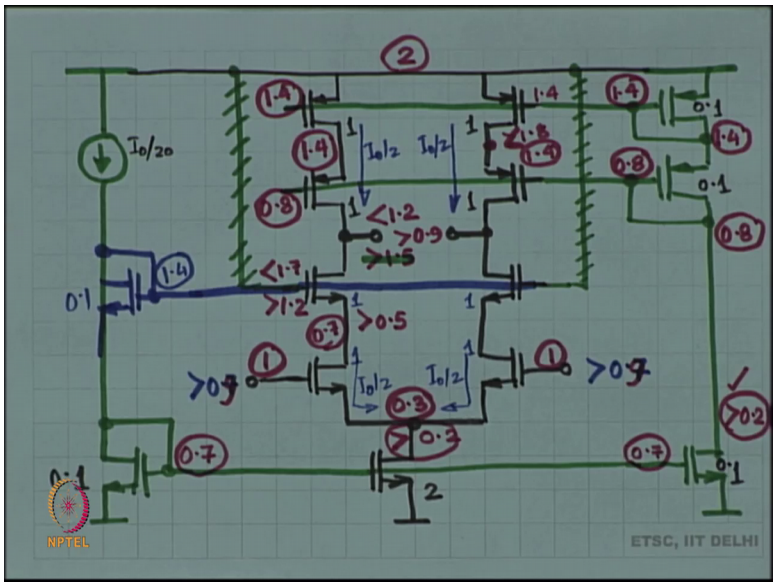

So, this is my set up alright, this is my amplifier where of the outputs two inputs two outputs, fine. Now, let us put some numbers, let say my power supply is 2 volts, and let us say that I like Vgst of 0.2 volts and let us say VT is 0.5 volts these are just numbers that I am throwing at you I will just because I like these numbers, ok.

So, for my given current source I would like this node to be at 0.7, alright. So, I am going to a size this device such that this node is 0.7, 0.5 plus 0.2 of Vgst this device will required 0.2 volts of Vgst which means that took place this nicely infatuation the minimum voltage here is 0.2, this is also at 0.7 and likewise the minimum voltage here is 0.2, ok.

So, this voltage is have to be greater than 0.2 to make sure that the devices having saturation; alright. And let us say that the PMOS also happens to have Vt of 0.5 volts, you want a different number, ok, fine. Let us say the PMOS has Vt of 0.4 volts, just throwing numbers. So, 0.4 volts of Vt and I would like the PMOS to also have a Vgst that is Vgs minus Vst minus VT of 0.2 volts which means that I want Vsg to be source to get voltage to be about 0.6 volts which means that when I pull this I naught by 2 of current just by the way this is 1 unit, this is 2 units, this is 1 unit, these are all 1 units each and normally what is done is you scale these down and you scale these down. So, that you do not waste current ok.

So, you might want to make this 0.1 unit instead of 0.1, and then again you might want to make this also 0.1 unit. When I say 0.1 unit, what is 0.1? This is the ratio of the w by l's. So, w by l is not 0.1, ok. If this has a w by l of 100 then this will have a w by l of 5, 20 times only, that is what I mean ok, that is all. So, for example, if this has a w by l of 50 then this should have a w by l of 5, and if this current is I naught by 20 then this current will be I naught by I naught this current will be I naught by 10, I naught by 20, right. This current will be I naught by 2 and so on. So, this is something that would actually be done we would not really keep things that equal.

So, this is my overall scheme of things minimum voltage here is 0.2 ok, but the PMOS this particular PMOS will require 0.6 volts of Vsg, right because we picked VT is 0.4 which means that the voltage here at the gate of the top PMOS is required to be one 0.4 ok.

So, the drain of the top PMOS is also 1.4 which means the gate of the second PMOS is 0.8 and this is satisfying this requirement ok. So, all these are happy over here right now great next let us look up over here this is at 1.4, what is the maximum voltage at this node maximum and we will just figure out what it is exactly? What is the maximum allowed? The maximum allowed is 1.8 because I have 0.2 volts of Vsg minus VT, sorry

it should be less than 1.8, but what is it actually? This node is 0.8 this requires Vgst of 0.2 that means, this is 0.6 volts above.

So, this is actually 1.4, ok. So, this node is actually at work 0.4 and it is satisfying the fact that it is less than 1.8. So, it is not really optimal. For an optimal situation it would have been exactly at 1.8, it is not optimal over here. In reason why it is not optimal because of this Wilson current mirror you can make a better current mirror. So, this node is exactly at 1.4, this is also at 1.4, this is at 0.8, alright.

Next, let us figure out what is the maximum voltage over here. This is at 1.4, Vsg required is 0.6, Vsg minus Vt is 0.2 which means that v source to drain has to be at least 0.2 volts which means the maximum voltage at this node is 1.2, ok. It cannot go higher, because if it does go higher then these this device falls out of saturation. It does not really damage things that much because there is graceful degradation, this is a nice Wilson current mirror. However, you can say that this is the maximum that you are going to tolerate for best performance, alright. What is the voltage over here? 2, ok. 2 volts, I hope it up straight up straight up. So, 2 volts is the voltage over here. What is the minimum at the output? 2 minus Vt, right? If this is 2, then this is 1.3, 0.7 volts of Vgs.

So, this is 1.3 means that this can be this has to be at least 1.5. So, we have a violation, right. This NMOS saying that the voltage here has to be more than 1.5, the PMOS is saying that no, no the voltage here has to be less than 1.2. So, in either case you have a conflict and therefore, this cannot be at 2 volts this has to be placed lower so that is why I said is it really to have 2 volts over there? No, it is not ok. You need a lower voltage, all right.

So, we will place a voltage over there let us be go from bottom up ok. So, what is the lowest voltage over here at the input? Input common mode has to be more than 0.7 ok, as long as it is something more than 0.7 then this node is gone to keep the bottom tail current source happy, alright. So, let us assume some number. Let say that the input common mode voltage I have set it to 1 volt. Suppose, a 2 volts is the power supply, let us keep the input common mode at 1 volt half of the power supply and this is coming from outside all right.

So, the bottom device is happy. Why, because Vgs is how much? 0.7 volts, so this node is actually at 0.3 which keeps the bottom device happy because it is more than 0.2 great

now what is the lowest voltage at this node lowest allowed voltage this is at one. So, this must be at least 0.5, if not more, ok. Now, supposing it exactly at 0.5 then this device is just about happy, right, there is no flexibility just about happy in that case what is the what will you apply at the voltage over here, as the voltage over here 1.2, right. If this is exactly at 0.5, this has to be exactly at 1.2.

So, the voltage here has to be certainly more than 1.2 in that case, we try with 2 volts which was more than 1.2, but with 2 volts I did not have an output. So, if I apply exactly 1.2 then what is the lowest voltage at the output? The lowest voltage at the output is 0.7, ok. So, let us not apply let us not be so tight, let us make it a 1.5 let us say or you want 1.7, ok. So, let us make it 1.7 if I apply 1.7 volts over here, then what is going to happen the voltage here will be one volts which is perfectly fine 1.7 here, 1 volt here what is the least voltage over here, 1.2 ok. So, the voltage here cannot be lower than 1.2 which means if you have 1.2 you add just about right there is no possible swing which means the voltage out here has to be actually less than 1.7.

So, 1.7 if I keep the voltage here at 1.7, then that is really so high that no swing is allowed at the output, ok. So, you have to you have to you know place this judicially, place these voltages you know intelligently you cannot just place random voltages, ok. In that cases how do I generate this voltage? How you are going to generate this voltage? Is for example, how will I get a number between 1.7 and 1.2? Well place one more. So, I have got 0.7 then I will get 1.4 over here 1.4 is very reasonable ok.

So, you have to do these things a little smartly, it is all on a case by case basis and you have to be a little creative about it, right. You have to see what is the Vt of the device. So, you have to work out all the swings, you have to work out all the Vt's, workout all the swings the Vgs minus Vt, see exactly what is required and accordingly creatively make your circle design, your circle and these are the general guidelines. The general guidelines are that you need some swing right, a cascode. You can use cascode to generate other voltages. I naught by 20 current is going through. So, this has to be of size 0.1, right because then only it is going to generate 0.7 volts of Vgs minus Vt, sorry 0.7 volts of Vgs that is what you need, and then you apply this is of course, of size 1 alright.

This is your telescopic cascode amplifier, now that I have placed 1.4 volts over here which is less than 1.7 more than 1.2. Is this node what is the voltage here in that case?

1.4 minus 0.7. So, this is exactly at 0.7 which is fine and the lowest voltage over here now is 0.9. So, the output voltage can now swing between 0.9 volts and 1.2 volts just 300 millivolts of room at the output not very much ok, it is not lot of room and that too my input is exactly at 1 volt, right. It is not at the lowest limit, it is not it just 100 millivolt above the lowest limit. The lowest limit was, what was the lowest limit, sorry this is not 0.7 it should be 0.9 ok, the lowest limit is 0.9. So, it is a little bit above the lowest limit this device is barely in saturation ok. So, 100 millivolt you can increase over here may be right on that bottom side you might be able to increase by 100 millivolts, but it is not much room, alright.

So, what is there are; this is a good design or not? This is generally a good design just that there are too many devices in a stack, and each of these devices are eating up head room, right, they are all eating up head room which is living not much room for the output nodes to swing, ok. So, if you want the output nodes to swing more what do you have to do? You have to somehow re-engineer the circuit such that the stack size is not five devices, it is less. The stack size cannot be five devices. If you reduce the stack size let us say if I make if I manage to make it four devices, immediately I will get a performance benefit over here the swings are going to right now the swing is just 300 millivolts at each output; if I can reduced by one transistor in the stack then immediately that 300 millivolts might become 500 or 600 millivolts, ok. So, we are going to see that, alright.

So, this is called the telescopic cascode amplifier. Why is it called telescopic cascade, because it is like you have stage after stage you know the telescope opens out. So, that is it is just a name. So, this is this is called the telescopic cascode in this case differential amplifier fully differential amplifier. Next what we are going to study is called a folded cascode differential amplifier. What we are going do is we are going to try to reduce one out of these five, can be fold it let us say can be make this one of these as the PMOS, right and then fold the structure in a way that it still works ok. So, let us go back to my half circuit.

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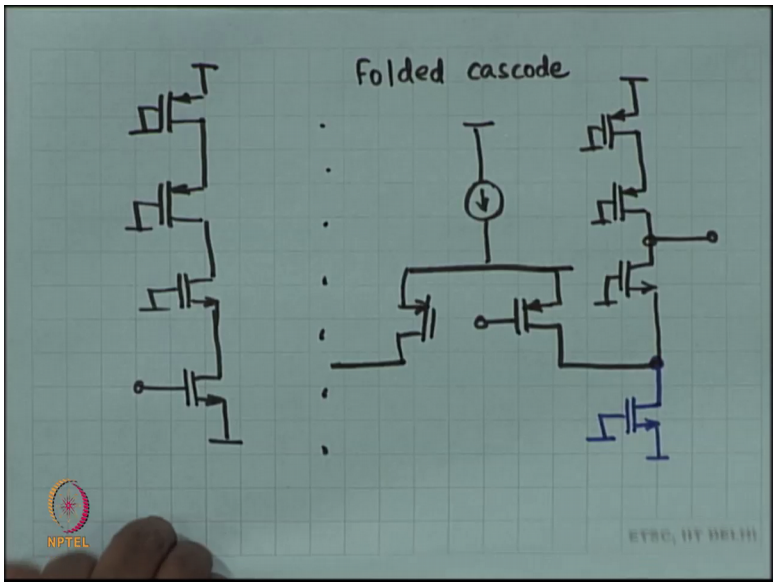

My half circuit look like this alright. Now, what if I say let us twist this and can I make this as the half circuit also? Is this also good half circuit? Of course, this is also a good half circuit, because it is exactly the same, ok. Just that I have twisted this bottom device up, right and in the small signal picture incremental picture there is no difference between nMOS and PMOS.

So, this is also an equally good half circuit and if you place a current source over here. You can go ahead and place a current source then this will also work a current source would be an nMOS in this case, ok. This is also good circuit reasonably good circuit, alright. So, now, what we are going to do is we are going to make redesign our circuit with this as the basis this is going to be the half circuit, alright.

So, the plan is that I will have this as my half circuit and then regenerate the complete circuit, ok. Where is the tail current source going to be? So, the tail current source used to be over here, now it is going to be here and then you mirror, alright. So, this structure is call the folded cascode. Let us look at it let us draw it nicely.

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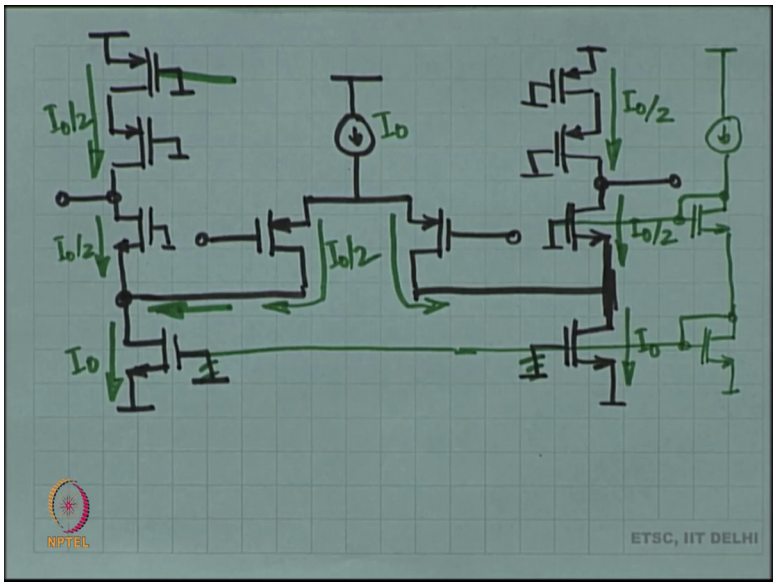

So, these are my two inputs I am sorry ok. So, the first thing you should notice is that my stacks size has reduced, I have now got a stack only of four transistors, ok. This is not the complete thing, this is still the small signal incremental picture I have converted the differential half circuit into a full circuit, alright. Next, we have to do the bias the DC operating 0 this is fine, right, you can ok.

So, for the DC operating 0 what is the plan if this is I naught, if the tail current is I naught then you expect, these two current should be I naught by 2 each ok. So, I naught by 2 current is flowing this way and remember in the earlier case in this particular case you wanted the same current to flow through the load, the active load, right which means that you would want so, this is your active load right; these two currents also to be I naught by 2, which means that these two MOSFETs these are current sources. Remember, this was this 0 we said. Let us add a current source here, ok. This MOSFET is actually a current source.

So, these two MOSFETs should be drawing I naught each, of course, you can rework this. This is does not have to be the case, this could be you know two times I naught then in that case this would be 5, I naught by 2 and so on and so forth. You can rework the numbers according to your design, but this is the overall strategy, alright. In that case what do you have to do you have to make all of these current out of current mirrors once again, alright. So, you are going to have this current mirror it is going to mirror out I

naught over here and then similarly, you are going to create the voltage here the voltage here. The voltage here, you want me to redraw it, redraw the whole thing want me to draw it just like we did last time and discuss the swings, yes ok.

So, let us draw the whole thing. The plan is that these two would not be grounds these two will come from a current source right and likewise these two will also come from a current source, and then may be a mirror of that is going to generate I naught by 2, ok. So, another mirror a cascode mirror copy of copy and then you are going to generate these voltages, ok. Let us draw it there is no space on this page anymore. So, let us draw it nicely.

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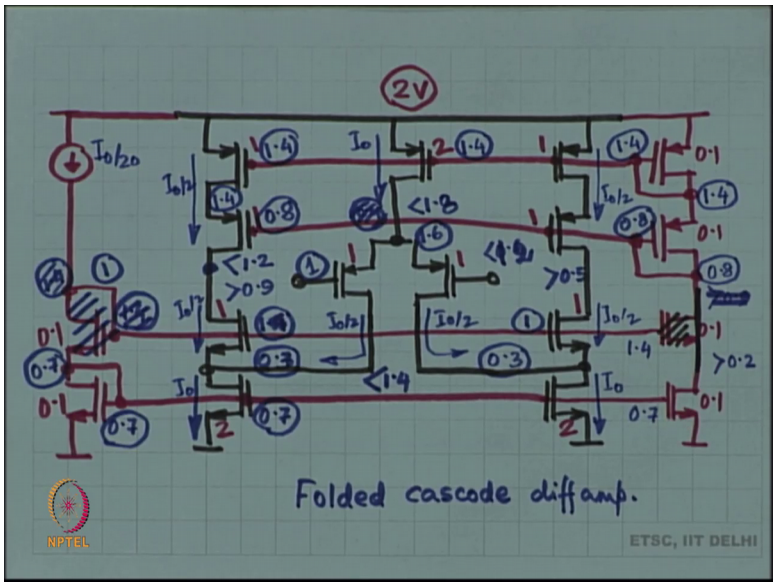

So this is my output stage where is the current coming in the currents is coming in over here from the input stage, and let us make my input stage. These are my two inputs joint together to make a current source. Current source will also be a p channel MOSFET that is the tail current source, alright. So, this is my structure and now, I have to work out all these individual get voltages, ok. So, let us take out a reference current, we always start with the reference current and where is this? What is the insight? This reference current it is one of those you know the refer g constant g m. Let us say the reference current source, ok. So, that is now you are going to make that reference current ok.

So, we start again with the reference current and we do a Wilson current mirror. Let us say you can do a more optimal design instead of Wilson, you it is all creativity, you have

to be a little creative, and then we have to work out a PMOS version of this. Once again let us do a Wilson current mirror to create the remaining voltages fine; yes, this is also connected, these are all connected.

So, this is my circuit, ok. I have drawn all the details now let us put some values, let us say this is you know you want to start with I naught by 20 ok, I naught by 20, ok. Replace this at 2 volts just like earlier and let us say all the PMOS's have required Vgst of 0.2 volts they have Vt of 0.4 and therefore, they require all source get voltage of 0.6 and let us say all the nMOS's requires get source voltage of 0.7, alright.

So, I generate 0.7 over here, 1.4 over here, I hope by now you are getting used to this, this sort of you know the design here you should be getting used to this design. So, the gate over here is at 0.7, what should be the size? What should be the current here? The current here has to be I naught. Remember, whereas the current here there has to be I naught by 2 and the remaining I naught by 2 is coming from here and this is I naught.

So, this immediately tells you the relative sizes if this is I naught by 20, and let us say I keep this relative size as 0.1 this as 0.1 then automatically, that means, that this should be should have a relative size of this is 0.1 I naught by 20 what should be the size of this relatively 2 2 what about here this is I naught by 2.

So, therefore, the relative size of this should be 1 unit, this should be 1 unit about here, 1 unit, 1 unit about here, 1 unit, 1 unit, 2 units, 1 unit each, ok. In this branch you do not want to waste much current, right. You want everything to be no low current because this is a silent this is just for DC operating point conditions you have created this branch. So, therefore, this these sizes should be similar. So, 0.1, 0.1, 0.1, 0.1, so that here also the current is I naught by 20 is this, alright. Let us now check out the numbers.

So, the voltage here is 0.7 here it is 1.4. So, the lowest voltage here can be 0.9, 0.5 less than 1.4 ok, but does this workout for your PMOS, you need 0.6, 0.6 and as the result you are getting voltage here required voltage is 0.8. So, you have a problem even before you start you have a problem, ok. So, this Wilson business is not quite working out, this Wilson current mirror is no good, alright. You need to be a little more aggressive, you cannot be you cannot be using Wilson. May be you can skip this device, one possibilities skip this device all together, you do not really need this device in which case you do not need be more than 0.9, ok. This voltage here is being generated from this, right.

So, this device is not needed at all this is just occupying some area and some head room, ok. So, if this is 0.7 then the voltage here is minimum voltage here is 0.2 which is alright, because here you will get 1.4, here you will get 0.8, and that is certainly more than 0.2, which is fine. So, the voltage here is 1.4, the voltage here is 0.8 and this device what is what is the voltage here 0.8 minus 0.6. So, it is 0.2. So, I am sorry plus 0.6.

So, this is also at 1.4 now this is the Wilson action, right. The Wilson action makes sure that current reflected current is exactly identical to the reference right and that is because both gate and drain are at the same voltage as that of the reference branch, ok. So, that is why this was 1.4, this is also 1.4, this is also 1.4, fine ok. What is the maximum here? Therefore, if this is at 0.8, what is the maximum, this is the output. The output is flexible, right. You will always see that the output is flexible, you would not be able to pin point what is the exact voltage there. If you do that then that is wrong, ok. The output needs flexibility. What is the voltage here? Maximum. Maximum voltage here is if this is 1.4 the maximum voltage here is 1.2, alright. Now, let us what bottom up I have got 0.7 here, alright I got 1.4 here and that tells me what is the voltage over here. At the source if this is 1.4, this is got to be 0.7, ok. I have already decided that voltage 0.7 it is at the drain of the input.

So, be a little careful over there, but it is already pre decided because of the Wilson action, ok. So, if this is at 0.7, what is the minimum voltage over here? 0.9, alright. So, you have got a swing from 1.2 volt to 0.9 volt now, you had nothing you, earlier also it was 1.2 volt to 0.9 volt now also it is 1.2 volt to 0.9 volt and I had promised you that we will get better, right and we have not really got any better because of this Wilson action, right. This is no good, this is 1.4 volt is no good. Why do you need 1.4 over here? right, this voltage can easily be lower.

So, let us now do 1.4 volts. Let us make sure the somehow, not this way, some other way, ok. They are going to make sure that this voltage is not 1.4, we have to be creative remember, we did all those optimal current sources and current mirrors and so on. So, this one is no good, right. Let us make sure that we do a little better job over here and instead of 1.4, I make it let us say 1 volt in which case this is 1 volt, in which case this voltage is set to 0.3, right and if this is 1, then the lowest voltage at the output is 0.5 and suddenly you have got much more swing available at the output, a what about the input.

So, I keep this at 0.3, right what should be the input? The input has to be anything such that.

So, this if this voltage is at 0.3 what is Vds? Vds has to be more than Vgs minus Vt, Vs Vsd has to be more than Vsg minus Vt. In this case the maximum voltage over here is 1.2, alright. So, the maximum gate voltage at the input the maximum input common mode voltage is 1.2 minus 0.6. So, the maximum input common mode voltage is 0.6 you cannot have more than 0.6 volts, because if you have more than 0.6 this is more than oh I am sorry, this is not 1.2, this is 1.8. So, the maximum here is 1.8, the maximum here is 0.6, less than 1.8.

So, less than anything less than 1.2 we had picked you know let us say 1 volt as the input common mode voltage which is less than 1.2 which is a perfectly good input common mode voltage because it is half way between the two power drills. So, let us say the input common mode voltage is 1 volt in which case what is the maximum allowed voltage here this 1 volt. So, the voltage here is 0.4 set, I am sorry 1 plus 0.6. So, 1.6 ok, which is less than 1.8 and therefore, the maximum voltage here is 1.4 and 0.3 is you know well, below 1.4.

So, you are doing a pretty decent job, anyway. So, this is the folded cascode amplifier you have to set this side, right. So, we remove this device, we remove this devices well, we need have a lower voltage over here, right. How do we get a lower voltage? How do you get a lower voltage? You can do other tricks, you can you know have other current sourc,e small current source and pull a large amount where have a large device have a lesser Vgs minus Vt all kinds of other tricks you can implement to get a lower voltage out here. It just has to be stable voltage that is all that is needed, alright. So, this is the folded cascode amplifier.

So, today what we have discussed is swing essentially, right. We have essentially discussed all these voltages, we have discussed head rooms, we have discussed swing and we have I have tried to give you a complete picture of what this fully differential amplifier is going to look like. This is fairly complex right you have got. We started our course with the one transistor set up and now, suddenly you have a set up over here that has you know 4 plus 4, 8 plus 3, 11 plus another 4 that is 15; 15 transistors on this picture right. Another two more that I have deleted, right and then you have to count more inside

this and so on. So, from one we have built up at least 15, if not more, ok. So, we have come a long way.

So, let us stop over here. And in the next class, we are going to proceed further and get more ideas of how the amplifier is going to look like.

Thank you.