Analog Electronic Circuits
Prof. Shouribrata Chatterjee
Department of Electrical Engineering
Indian Institute of Technology, Delhi

Lecture - 20
Self biased active load diff. amp

Hello welcome to Analog Electronic Circuits lecture 20. So, today we are going to talk about the self biased active load, differential amplifier differential input single ended output, the circuit.

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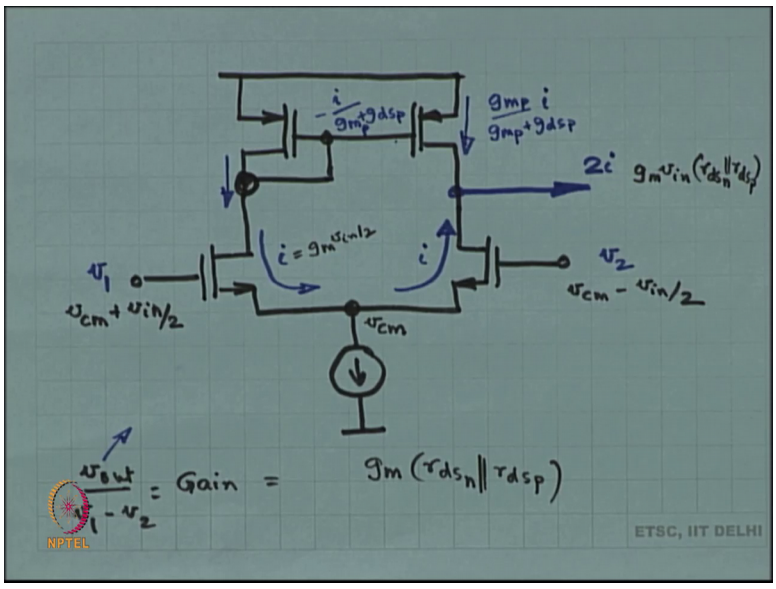

We were discussing in the last class was setup, where I had a differential amplifier, but the load was a current mirror as opposed to regular active load P MOS on each output, right.

So, this was the circuit we were discussing and, let us assume that this current source the tail current source is an ideal current source, we applied at the two inputs, we applied some common mode plus v in by 2 and the same common mode minus v in by 2, then in the last class we solved a little bit right, we did the little KCL and figured out that if this is i in the same i has to go the other way because, the current source does not take any signal current then. That means, that the voltage over here will be exactly equal to v cm which means v in by 2 drop will be created here minus v in by 2 drop will be created across the other v G S and. I will be equal to g m times v in by 2 here, we did not take

into account r ds of this particular MOSFET, we have forgotten about r ds of that MOSFET ok.

So, that is problem, however that that is minor problem according to me that we have for so, that is any inaccuracy in this analysis. So, one inaccuracy is that we forgot about r ds between these 2 terminals. We are just saying i is g m times v in by 2, that i is creating a voltage drop over here because, this is a diode connected MOSFET right. So, the voltage drop over here will be minus i by g m plus g d s g m p plus g d s p ok, that is the voltage drop over here, here I have taken into account the resistance of the P MOS.

Alright, I forgot to take into account resistance of the N MOS, but here I have taken into account resistance of the P MOS. So, we have forgotten this remember ok. So, if you want to take into account resistance of the N MOS, then one more so, this i current will also drop across that extra g d s n. So, that is going to get adder into this denominator let us not worried about it now ok.

So, this drop in this voltage creates a response in this current, in this MOSFET which is g m times that ok. So, i current is pushed this way and this also is approximately i so, i current is pushed the other way. And therefore, the current going out into the load is two times i and this two times i, if the if there is no load then this two times i is going to drop through, the r ds of the N MOS as well as the adieus of the P MOS. And therefore, your voltage over here is going to be two times i times r ds of N MOS in parallel with r ds of P MOS ok.

So, this was our analysis in the last class. And clearly there are some inaccuracies over here right, there is an inaccuracy i forgot r ds of this I did not even bother with it ok, is not going to make much of a difference trust me, because r ds is anyway very large ok. It is minor change in the expression is going to happen right and, then over here also i assume that this v cm is a constant is not necessarily a constant right, v cm could be changing in which case the impedance looking down over, here is not r ds of N MOS alright.

So, all kinds of problems are there and, I had a question in the meantime that from one of the students, I had a question that why do not we just you know why are we doing it so hard, we know that that the there are two inputs let us call this v 1 and v 2 and like, we solved in the class before the last class let us just to brute force analysis and the circuit is

not symmetric anyway, why we bothering why we trying so, hard let us just do a brute force analysis and see what happens ok.

So, this is what one of the students has said and let us try. So, the way you are going to do the brute force analysis is like this.

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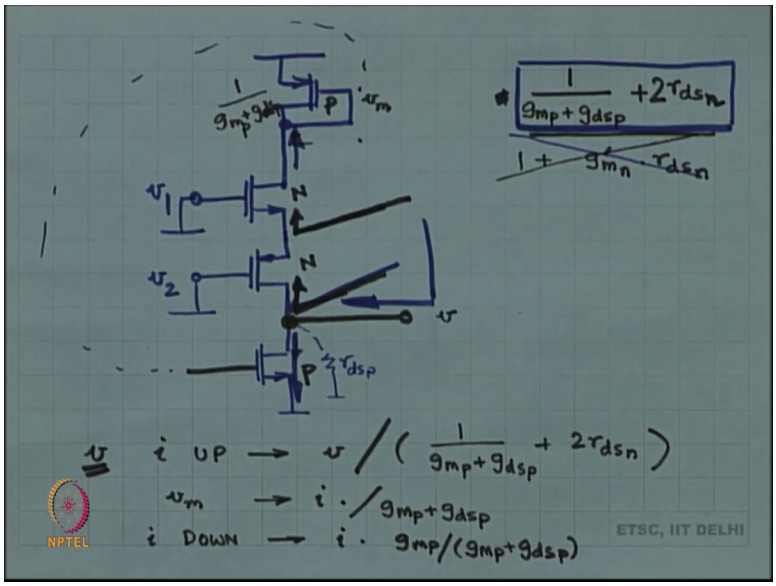

So, this is my top P MOS, which happens to be diode connected and, this is my input let us call this input v 1 with the understanding that v 1 is nothing but v cm plus v in by 2 and v 2 is nothing but v cm minus v in by 2 ok. So, this is what were going to do and, then over here I have got the current source, which I am not going to drop because, this is a small signal diagram that I am sketch that I am drawing.

Then over here I have got the second input device, which I am going to fold downwards and draw as P MOS ok. And then finally, on top there was a P MOS device right, and I will fold that also down words and, now I will draw it as an N MOS because, it looks nice with the caveat that the gate of this N MOS is actually connected up here.

And suddenly the drawing looks very bad right and, when these drawings look very bad invariably the analysis is also going to be very bad, it is not going to be so, straight forward anymore. We are no longer interested in 2 output voltages, we are interested only in 1, we are only interested in this one and only this one output voltage ok, unlike in

our earlier brute force analysis where we had two output voltages here we have only one ok.

So, we are going to apply v 1 over here measure the output, we are going to apply v 2 over here measure the output overall, it is going to be the combine response of v 1 and v 2 this is the plan ok. So, I have got v 1 in the first intense what we are going to do is we are going to connect v 2 to ground ok. And to measure the voltage at the output instead of measuring the voltage at the output, 1 the way we have been doing is by using the Norton equivalent method, that is we look in from outside and measure the impedance number 1 and number 2, we apply H short over here and measure the current ok.

So, these are the two things that we are going to do fine ok. Now, in step one you want to look in from outside and measure the impedance. So, this is the bummer this is a very difficult step over here, in this particular case this long wire this feedback wire is going to create a problem ok, because looking down you are not so, sure what is the impedance looking up, you have some idea, but looking down it is different ok. So, let us be careful about it, but let us do it anyway ok. So, I am going to connect both v 1 and v 2 to ground, looking from outside and measured the impedance. So, I look in from outside, I apply a voltage over here measure the current that is the idea right, looking from outside portion of the current will go up, portion of the current will go down.

Now, just by the way whatever current goes up get is pushed right it creates a voltage, that same voltage is applied on this. So, the same current is going to be pulled down ok, that is the current mirror action remember we have just fold it up. And, it now looks this looks like an N MOS, but this is actually the other half of the current mirror ok. So, looking up whatever current goes looking down exactly the same current will go. So, effectively approximately the same current will go. So, effectively looking up whatever impedance you see, looking down you will see more or less the same impedance, which means that the net impedance is going to be half ok.

I apply a voltage some current goes up equal current goes down right. So, the net impedance is going to be half of the impedance that you see looking up fine almost, let us work it up. So, let us first look up and only up, when you look up you are looking in from the drain of this P MOS, where the source is terminated by something.

So it is a formulae what is the source terminated with. So, you look in first over here and then you are looking in from the source of this N moss, where the drain is terminated by something and what is this something this is a resistor of value 1 by g m approximately ok, or of value 1 by g m plus g m p ok. So, looking in over here what do you see, looking into the source you are going to see whatever, you had at the drain class r ds divided by 1 plus intrinsic gain of the N MOS, by the way this is actually a P MOS this is actually an N MOS, this is also an N MOS, this is a P MOS in the actual circuits ok.

So, right now I have drawn it differently, but these are actually these are the N MOS's and P MOS's. So, the impedance looking up over here is what I have written the imp this impedance is, this prime over here indicates there it is actually g m plus g m b. So, this is the impedance looking in from the source of the N MOS ok. Now, when I looking from the drain of this bottom device, then it is whatever was on the source times 1 plus the interns gain. So, this entire factor cancels plus r ds N fine, I hope by now you have memorize the 2 formula.

Those, 2 you see how we are applying the formulae like, you know it is bread and butter ok. So, this is the impedance looking up into the drain of this particular MOSFET alright. So, I apply a voltage v the current going up is v divided by so much. Now, this current eventually makes it is way through this, the same current goes through this alright.

And it is going to create some potential over here, the same potential is going to be applied on to this MOSFET alright. And therefore, this current remember this also r ds of this P MOS, this current is going to be the same current times this g m divided by g m p plus g d s p alright. So, I apply a voltage v over here the current going up so, v is the voltage I have applied the current going up is v divided by this much ok. The voltage at the gate let us call it something v v mirror is this current times that impedance, that is the voltage at the mirror. So, the current coming downwards is going to be that voltage times g m p fine is this ok.

And there is now an additional factor, there is also an additional resistance of r ds p over here ok, that is also there you are forgotten that alright. So, therefore, what is the net impedance, the net impedance is the impedance looking up divided by not a factor of 2, but by a factor of 1 plus g m p by g d s this factor ok. This is almost equal to 1. So, it is

not going to be divided by 2, it is going to be divided by 1 plus almost 1, further in parallel with r ds p. So, my final output impedance.

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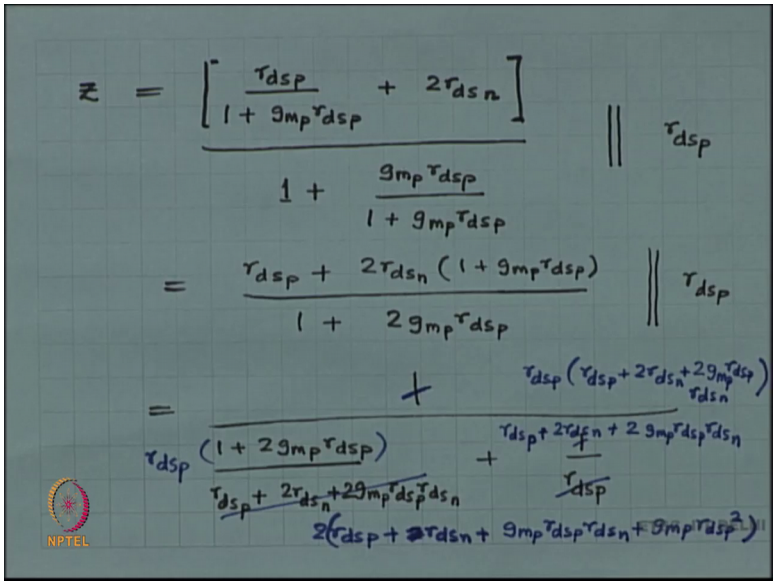

This the impedance looking up, divided by a factor of 1 plus ok, this is the combination of the impedance looking up, in the impedance looking down. Further in parallel with r ds p is this analysis ok, this the impedance looking in and this suffices this, this experiment is going to suffice for both application of v 1 as well as application of v 2 for both, you get the same answer ok, two experiments in one shot the output impedance.

Then we are going to apply v 1 measure the short circuits current, applied v 2 measure the short circuit current. And, then you know finally, will applied will see the net response, when I apply both v 1 and v 2 at the same time, this is the plan this is the first experiment in the three part experiment, first part this is ok, you want to simplify this, I like simplify right I do not like such huge complicated expressions right.

So, you can multiply numerator and denominator by 1 plus g m p r ds p that looks, the obvious think to do and, when you do that this is what you end up with, further in parallel with r ds p ok. So, this is little more tractable and then how will you deal with this, you want to place it in parallel ok. And, then generally what is done is you are going to multiply by these two factors numerator as well as denominator so, then and then add is just algebra and, then you can combine the 2 so, you get two times r ds p in the

denominator, 2 r ds n 2 times this. So, the two factor actually can come out and 2 times g m p. r ds p squared ok.

And in the numerator what do you have you got r ds p, 2 r ds n plus 2 g m p r ds p r ds n ok, the whole thing times r ds p fine. This is this is pretty much the impedance notice, there is a factor of half right that tells you that the impedance is half of the output of the impedance looking up. So, that is why that factor of half showed up really alright.

So, the impedance these are small numbers compare to g m p, r ds p, r ds n and g m p r ds p, r d sp. So, the net denominator is nothing but g m p, r ds p times r ds N plus r ds p times 2 that is the denominator. And in the numerator what do you have these two are again small. So, you do not worry about it you have got g m p, r ds p times 2 r ds n times r ds p alright.

And then you have to look at what remakes ok. So, lots of things are going to cancel out alright. So, let us this is the output impedance story. So, let us keep this on the stack. And, now we are going to do the remaining two experiments. And the remaining two experiments, you see this is much harder right. This business this brute force business is much harder than our hand analysis, our earlier analysis where we just you know did the little bit of approximation. So, being accurate always comes at a cost right, in this case the penalty is lot more right, you really have to work hard on the problem to be precise ok. So, lot of times this precision is so, costly that you do not bother about it and you just do engineering.

So, if you want to do engineering that is the way, if you want to do maths and you want to be absolutely accurate, then you know this is what we are doing right now we should not be doing this. And this is something that I am doing because someone said over here that you know, why do not we do it the brute force method, is also appointed to see how hard to the problems becomes ok. So, now short circuit current.

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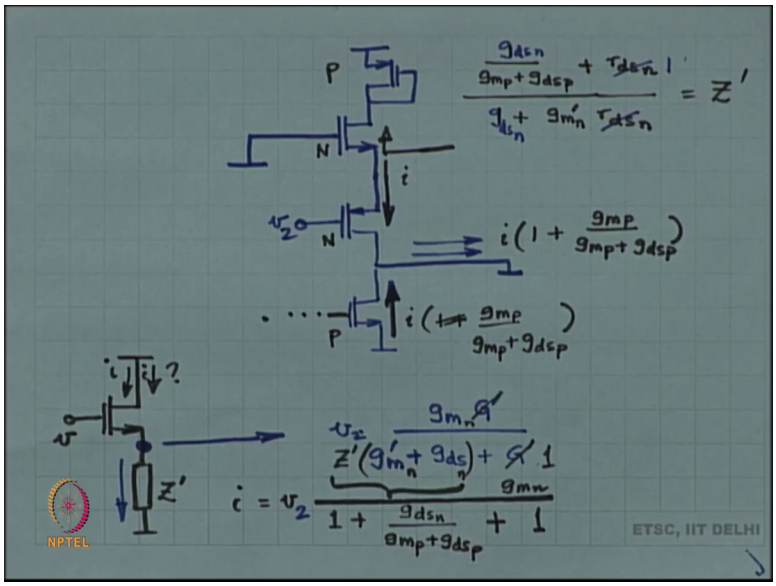

So, this gate is actually connect hooked back over here alright, now what we have done is we have applied v, and v is going to create some current over here we do not, let us not worry about what that value is going to create some current. That current is certainly going to go through the short circuit, but this current is going to create a voltage, the same voltage is applied here.

So, an identical mirror copy of the current is going to be created here. So, the current here is coming downwards right, the mirror will also do a downwards, but when you turn it is going to be an upwards current fine. So, you have two components to the current, one is coming because of the P MOS, the other is coming because of the mirror alright.

So, the net short circuit current is going to be double approximately and, by now you have figured out the mirror ratio, that is if this current is some i, then this current is going to be i times 1 plus sorry i times g m p by g m p plus g d s p right is there going to be current in r ds no because, it is a shorter no current in r ds. So, at least that part is gone and that is it ok. So, the net current is going to be i times 1 plus g m p divided by g m p plus g d s p ok.

Now, all I have to work out is what is this i current and this is nothing but the bottom side of the common drain circuits, the drain is at ground right this is the bottom side, think of this as an N MOS you apply a voltage at the gate of the N MOS. The drain is at ground, the source is terminated with some impedance, what is that impedance by the

way what is the impedance looking up over here, you are looking into the source of the MOSFET, the drain is terminated with something that impedance is nothing but we had computed it earlier right.

So, the drain is terminated with 1 by g m p plus g d s p that is what the drain is terminated by, but looking in from the source, what you have is this divided by so, this plus r ds n at the end of the day this is N MOS this is also N MOS. So, be careful this is P MOS. So, what is whatever is on that? So, I am looking in from the source to find the impedance, what is on the drain divided by what is on the drain plus r ds n divided by 1 plus the intrinsic gain that is this impedance.

So, my problem looks like this, this is i current what is the value of I: if I apply v over here and, i terminate the source the source is terminated with this impedance. Let us call this impedance, you know Z prime. This is the common drain circuit and me know how to solve this, because we know the voltage over here, what is the voltage over there the voltage has an approximate gain of 1 ok.

So, if this is v the voltage over here is v times g m by g m plus non idealities, biggest non ideality over here is g mb which make this makes this g m prime g m plus g m p I am writing test g m prime plus, the other non idealities g d s and the other non ideality is that prime ok, that is the voltage over there. Now, if that is the voltage over there then the current i is this voltage times g prime and, generally a good idea is to multiply numerator and denominator by Z prime, when you have got both ok.

So, this is what we have the other thing is sometimes you got g d s, this is g d s of n ok, here you got r ds of n. So, one thing that you can do is just alright you want to change this, or this it does not matter multiply numerator and denominator by g d s n over here ok. Now, Z prime has a denominator and that is being multiplied by the same denominator. So, Z prime times this factor is nothing but whatever is in the numerator over here and, then you got 1 ok. So, this is my i, but my final short circuit current is i times 1 plus so much ok.

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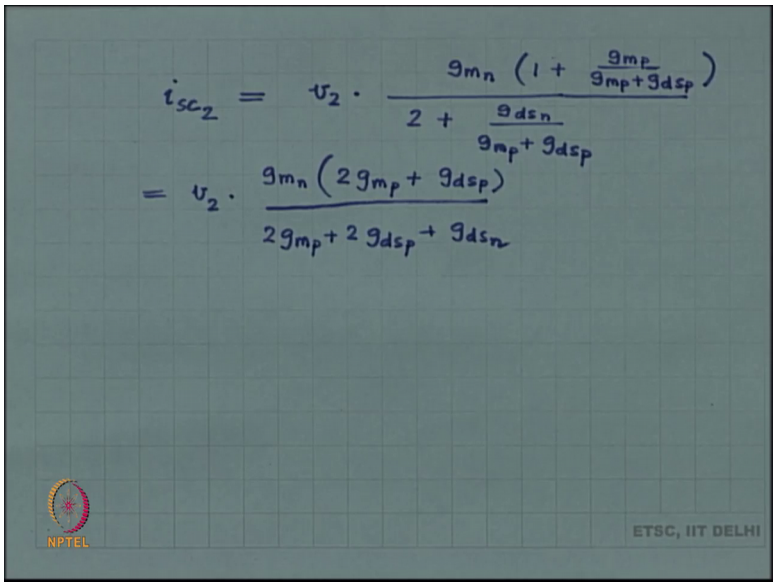

So, let us write it out so my i short circuit, when I have applied v 1 or v 2 which 1 did I apply I have applied v 2. So, I have applied v 2 and I got a current i in this case, first I applied v 2 and I got a current i ok. This was the current that i got, when i applied v 2. Now, this current times 1 plus g m p by g m p plus g d s p is the total short circuit current. And obviously, what you are going to do is multiply numerator and denominator by g m p plus g d s p fine. So, I applied v 2 I got a short circuit current, in the next step what we are going to do is we are going to apply v 1 and find out a similar short circuit current.

And then we are going to combine the two short circuit currents. I already have the output impedance come put all of these together finally, you will come at an expression which gives you the gain, lot of hard work do you want to continue doing that, you want to continue because it is it is really a lot of hard work that we are doing and finally, you will come up with an expression we can do it ok.

This brute force method will work ok, will apply v 1 drain is terminated with resistance ok. On the source side you have some complicated resistance. So, this is going to look like a source de generated amplifier, look this is how the analysis goes. The analysis is always going to boil down to a one transistor circuit right, then you recall what you did for that one transistor circuit and plate out on paper ok.

Let us how it is gone to work out. So, I am not going to bother with this your answer is finally, going to come down to the same thing to something close by right, it is not going to be exactly equal to our initial result is not going to be exactly equal to this, but it is going to be close alright is this ok. So, this is some the idea of the self biased active load differential amplifier, this is what we did right.

We wanted to do a brute force method. So, in the brute force method we applied v 1 found out the short circuit current over here applied v 2, found out the short circuit current over here, we did not really we actually only did v 2, we did not really do v 1 right v 1 was harder because, v 1 if I apply then on the source side, I have got something more complicated, there is all of this on the source side right on the drain side I have got this and, then I have got the current mirror ok.

So, every time I have got the current mirror, you know an extra current is going to get pushed in to the short circuit fine, eventually you will do all of this analysis will come up with exactly the same answer. And therefore, what I am trying to says let us not worry about it, you do these analysis in your free time I am telling you how to do it, but I do not want to do it in active class time class minutes.

Alright, maybe one possibility would be that as a as a handout I could solve this entire thing and give it to you as reference material. So, that you see how the whole analysis has been done ok. So, next we have learnt a few things first thing, that we have learnt is our basic differential amplifier, resistor differential amplifier. Then we said let us get rid of the resistor place an active load over there ok. We did the analysis of input common mode range, we figured out what are what are the swing issues over here what is the largest voltage smallest voltage, what are what is the voltage range at the input and correspondingly what is the voltage range at the output, we figured of this thing out.

Then be also studied the self biased active load differential amplifier, where we do not need an extra current mirror the current mirror is built into the circuit but of course, this circuit breaks the symmetry invents mean symmetry is broken the analysis becomes very hard, but in this particular case the answer can still be worked out with some sort of intuitive symmetry ok. Your answer, what is the final gain of the circuit sorry, what is the final gain of these circuits. If this is v in by 2 input signal, this i is g m times v in by 2 the same i g m v in by 2 g m v in by 2, what goes out is what goes out g m v in current goes

up and, this g m v in current develops across the load. So, your answer is in terms of voltage, this is your voltage at the output ok.

So, you are gain is still g m times r ds n in parallel with r ds p, your gain in terms of output voltage divided by input differential voltage, output voltage divided by v 1 minus v 2 is going to be g m times r ds n in parallel with r ds p fine, what would have happened if this was symmetric, if this was symmetric you would have broken it up into half circuits right.

In each half circuit we are applying v in by 2 this is now ground, you have applied v in by 2 ok. So, the short circuit current is g m v in by 2 output impedance is r ds of n in parallel with r ds of p this is not there ok. So, output impedance is r ds n in parallel with r ds p short circuit current is g m v in by 2 ok. So, the voltage at the output is going to be minus g m v in by 2 times r ds n parallel with r ds p the differential voltage in 1 here, we applied v in by 2 in the other you applied minus v in by 2.

So, the differential voltage will be double and therefore, you will get exactly the same differential voltage in the other case, in the symmetric case you will get exactly the same differential voltage. So, in that case also we out it is no longer just one node voltage, it is the difference between 2 voltages that will also be exactly the same, it will be g m v in r ds n in parallel with r ds p ok.

And therefore, the gain between the differential output and the differential input is going to be exactly the same ok, in this case it is single ended voltage by differential input, in that case it is going to be differential output by deferential input. The gains happen to be equal how strange is that. So, effectively it is almost as if this is this will have double the gain almost as if ok, it is not quite right is does not have double the gain, this has the same gain. Just that 1 node is swinging double what the other node other 2 nodes were swinging each.

This 1 node has a voltage which is double of the in the individual nodes in the other case, but the difference between the individual nodes in the other case is the same as this voltage in this case ok, what about this node, what about this node, is this node moving, this node is not moving around at all ok, I am producing i current this i current is coming through a diode. The diode has a low impedance the impedance is 1 by g m p ok.

So, the voltage that it produces is almost nothing, it is v in by 2 times g m that is the current divided by g m p plus g d s p ok. So, if I apply v in by 2 signal over here, this node is swinging I mean changing by g m the g m by g m p times v in by 2, which is almost as if saying it is not swinging at all, it is amplitude is similar to the input amplitude. The input amplitude is small this amplitude is also very small ok.

So, the gain between here and here is nothing almost nothing ok. So, what happens over here, in this circuit this node is more or less static, this node goes double where as in the symmetric case, this node comes down this node goes up by equal amounts alright is this you know are you getting the clarity over here, what is happening what is the difference between this self bias load and, the ordinary un you know ordinary load you are understanding the difference.

In this case the voltage here is more or less constant. This is oscillating or this has a gain of two times, in the other case this has a gain of minus, this has a gain of plus 1 net difference is 2 alright. So, this is yourself biased active load op amps active load amplifier. Now, what is it is going to take you see I just mentioned op amps, what is it is going to take for us to make an op amp. We now know how to make a differential amplifier ok a differential amplifier is amplifying difference between 2 inputs.

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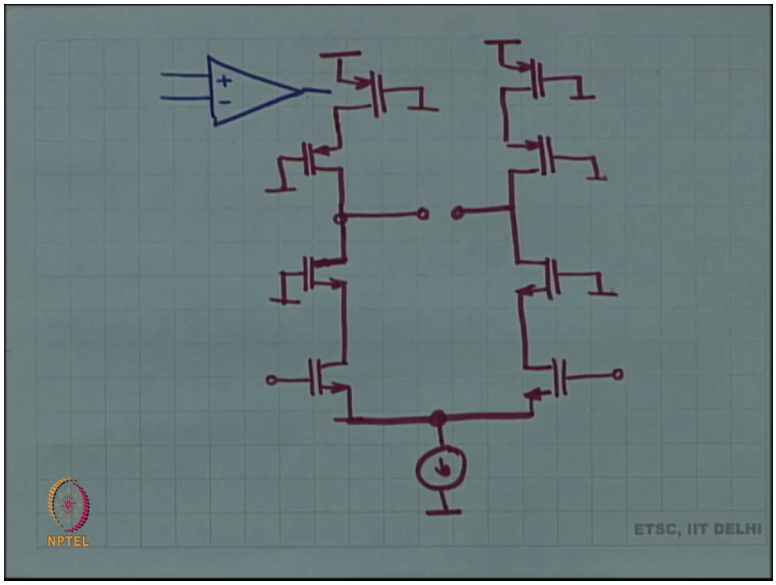

And it is almost as if we have managed to make this triangle, right our objective of the course is to make this, one important objective of the course is to know how to make this particular building block what is inside this triangle.

Now, is that it could this be what is inside this triangle, or do you need more you need more, why because you need more gain, this will provide you a gain of g m times r ds n in parallel with r ds p right, which is less than the intrinsic gain of the MOSFET. If the intrinsic gain of the MOSFET is 100, then maybe this amplifier over here will get you a gain 50. We did not we do not want 50 we want 1000 we do not even want 100, we want 1000 we want 5000's, we want a large gain 1000 again of a 1000, this you know probably bad op amp right gain of 10000 will give is a reasonably good op amp right, gain of 1000 is the lower limit of what the gain of an op amp should be ok.

So, we need to increase the gain of this circuit, how are we going to increase the gain of the circuit there are two ways one is cascade the other is cascode right, we studied long back one cascade the other cascode ok. So, the cascade is rather straight forward you just put to diff amps one after the other alright, the cascode let us look at the cascode because the cascade is so, easy.

Let us look at the cascode you see in case of the cascade, the small signal circuit, the small signal half circuit needs to look like a cascode amplifier. And my cascode amplifier look like, this normally this is drawn flipped ok, I flipped it around because there is no space, but this is the normal structure of the cascode amplifier.

Now what is the benefit? The benefit is that the output impedance is very large, output impedance over here is the output impedance looking down, which is intrinsic gain of this MOSFET times r ds of the lower 1 plus r ds of the top 1, in parallel with intrinsic gain of this MOSFET times r ds of the topmost 1 plus r ds of the lower 1 plus r ds of the lower 1. So, this is a large output impedance.

At the same time the short circuit current is approximately g m of the bottom transistor why, because I apply a voltage v it produces a current g m times v, this current has to choose between going through r ds and, looking into the source of the second MOSFET. And looking into the source of the second MOSFET it sees a low impedance, because all of this is shorted right it sees a low impedance.

Looking into the source of the second MOSFET, how low is it is proper it is 1 by g m of this MOSFET as a post to going through r ds of this? So, approximately g m is the transconductance ok, g m of this bottom MOSFET is approximately the transconductance, output impedance is g m of top device times r ds of top device times r ds of bottom device, in parallel with g m of this one, r ds of this one r ds of this one that is the output impedance.

So, net gain is g m of N MOS times the output impedance, which is the second g m the intrinsic gain of the second device times r ds n, in parallel with intrinsic gain of this device, in parallel with r ds in times r ds p fine. So, this was the cascode amplifier and, is there a way that I can make this cascode amplifier, as a differential amplifier and the answer is yes, very easily all I have to do is make sure that this is the differential mode half circuit, which means that I just make other branch over here which is a mirror image and places current source have the bottom. And now I will apply a differential input signal, common mode input signal, the differential input will be amplified, the common mode input will be suppressed right and all of this is going to happen exactly the same way as before.

Now, we are going to study this further, there are certain limitations of this, this is very good circuits, but there are a lot of limitations. So, we will study this further in the next class.

Thank you.