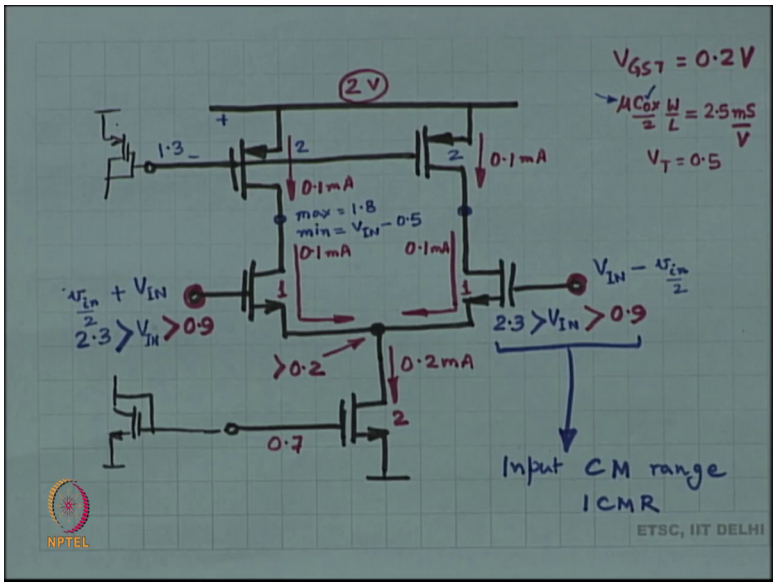
Analog Electronic Circuits
Prof. Shouribrata Chatterjee
Department of Electrical Engineering
Indian institute of Technology, Delhi

Lecture – 19
Differential amplifiers-III

Welcome to Analog Electronic Circuits. This is lecture 19 and we are going to continue from our, what we did in the last class. So, we are going to continue with differential amplifiers. So, in the last class we had studied the differential amplifier and we analyzed the differential amplifier from a brute-force point of view that is we analysis it by using superposition, one at a time we applied the two voltage sources and found the outcome.

Now what I am going to do today is so, that that is one thing that we did in the last class. The other thing that we did in the last class was we replaced the load that is the resistor on top of the differential amplifier with the PMOS device and that is called an active load and the PMOS device is very nice because it is a it behaves like a current source. So, at DC it provides just the right amount of current where as for the signal it provides a large resistance which is exactly what you wanted. And that basically takes over the role of the resistor and therefore, it allows for better swing hopefully.

(Refer Slide Time: 01:52)



So, let us let us take a look, at that relook at that structure and let us try to understand the performance limitations. By now I hope you understand that there is nothing special

about PMOS devices. PMOS devices are just like NMOS devices. They are in fact, the same as for as the small signal incremental picture goes; however, when you analyze it at DC operating point, then instead of taking source gate to source voltage, you take source to gate voltage. Instead of taking grain to voltage, you apply source to grain voltage that is all. Otherwise there is absolutely no difference just that the current flows backwards. Current does not flow backwards in the increment picture. In the operating point, current flows backwards that is all right.

So, I want to point out that there is nothing special about the PMOS device. Do not be afraid of it. Lot of you are genuinely afraid of the PMOS device. Whenever PMOS device pops up, you feel scared; should not be the case. So, there is a current source over here. This is called tail current source. In reality this current source going to be made with the MOSFET with the current mirror ok. So, these nodes I have marked out. Let us point out the values at these nodes.

Let us first take some numbers ok. Let us I will write some numbers ok. So, let us say I want to keep V GST as 0.2 volts and let us say ordinarily the W by L of the devices is such that for this V GST of 0.2 volts, the current through this device, the current through this particular device; how much do you want to keep it? k times 0.04 k into V GST squared ok.

So, let us keep it at you know water, 100 microampere 0.1 million ampere ok. So, k times 0.04 is 0.1 million ampere. So therefore k is mu C OX by 2 W by L. Let us keep that as 0.1 million ampere by 0.04. So, that is 2.5 millisiemens per volt ok. If I keep mu C OX by 2 W by L as 2.5 millisiemens per volt, then the current through this I apply V GST of 0.2 volts will be this times 0.2 squared that is this times 0.4 4 ok; that is 0.1 milliampere ok.

So, I will choose. So, there is some value of mu C OX by 2. I will choose W by L such that this is 2.5 millisiemens per volt. Is that ok? Fine. Now I have decided, what are the sizes of this 2 transistors, size means W and L W by L ratio right. I would like the current here to be 0. 2 milliamperes and for 0.2 milliamperes, I still want I means V GST of 2 volt is nice clean number ok. So, therefore, I will choose W by L is equals 2 times. So, let us say this is 1 time W by L 1 time W by L, then this 1 should have 2 times the W by L of those.

So, that V GST of this device is the same 0.2 volts ok. And let us say V T is 0.5 in which case I need to somehow apply 0.7 volts over here. So, if I apply 0.7 at this node, then automatically that conducts 0.2 milliamperes. If it conducts 0.2, it splats up into 0.1 and 0.1; If 0.1 as to come this way, then this will develop a V GST of 0.2 volts that is VGS of 0.7 volts or so. But I do not know the source voltage. This source voltage can be anything, right anything more than 0.2 because this needs to be in saturation; for it to behave like a current source ok. If this in saturation when V G S minus V T 0.2 volts rights.

So, V G S has to be more then 0.2, then 0.2 volts. If V D S is more than 0.2 volts then, that means, this node over here has to be greater than 0.2 all right; that sets a lower limit for both of these nodes at how much 0.2 plus another 0.7. So, this node has to be greater than 0.9 ok, any anything larger than 0.9 seems to be all right with us. Any questions? Ok great.

Now we will see, we need to also work out how much larger can it be. Can it be? We have not decided, what is doing to a volt here. Let us say the voltage here is you know what let it be 2 volts power supply. By the way how will you generate this 0.7? Will you apply a voltage source of 0.7 here? Will you? No voltage sources ok. The only one battery is allow 2 volts, that is it. You will have a 0. 1 million ampere current source or a 0.2 million current source or any other current source reflected with the current mirror and generate 0.7 volts, that is how you will do it. Not with the voltage source never. Is that understood? Ok.

So, this is not a voltage source. This is coming from somewhere. Let us get that clear in our head ok. Right now, it appears that I have put a number over there. It appears like it is a voltage source. It is not a voltage source at all. It is coming from something else. Current is being pushed into this device that is generating volt diode voltage right and how much current will decide; what is the size of this diode volt because you want V GST of 0. 2 volts for that diode volt and that is how you are going to generate 0.7.

Why are we doing this? Because V T changes with temperature ok; you think V T is 0. 5 volts, it need not have been 0.5 volts. If it was 0.4, even then this will work, but if you apply 0.7 volts and V T is suddenly 0.4, then suddenly now you have got different currents all over the place. Your currents are all wrong. So, you are always going to bias

it using current mirror not with voltage sources all right. Now what next? What about these two PMOSes? This two PMOSes also need to conduct 0.1 million ampere at DC. And for 0.1 million amperes, V S G has to be more than V T by a certain amount ok; according to the k of the PMOS.

So, let us say let us say usually mu of the PMOS, usually what happens is that the C OX of the PMOS is the same. C OX of the NMOS, C OX of the PMOS are equal usually. mu of the PMOS is usually is much lower than the mu of the NMOS and this much lower could be a factor of 2 lower. It could be a factor of 3 lower; however, in modern you know nanometer technology nodes, it not necessarily lower. It could also be equal or even higher sometimes. So, this PMOS mu of the holes versus mu of the electrons, mu of the electrons is the mu in the NMOS mu of the holes; the mobility of the holes is this parameter in the PMOS ok.

So, in the PMOS the mobility is usually lower. Holes are usually less mobile then the electrons; however, it so happens that in very fine technologies, modern technologies 28 nanometer, 22 nanometer 15 nanometer. It so, happens that the hole mobility is more or less at par with the electron mobility and sometimes even higher ok. In olden technologies, the whole mobility is substantially lower; 3 times, lower 2 times lower something like that. So, it all depends on which technology you are using, where you are and we are not doing to discuss the physics of the mobility. So, do not ask the questions whys. Do not ask me.

So, this is out of the scope of this particular course. We will take a value and deal with that value. So, let us say let us assume that the whole mobility is two times smaller than the electron mobility in which case, this mu C OX by 2 is half the NMOS mu C OX by 2 ok.

Suppose in which case, to have 0.1 million ampere with the V GST that is VSG minus VT right. So, we should actually call it VSGT for the PMOS. So, VSGT of 0.2 volts, if you want that kind of a source to get voltage, then this device requires a size of 2 W by L should be 2 times the W by L of the original because the whole mobility is half of the electron mobility.

So, it all depends. So, if the hole mobility is 3 times smaller than this would have been the number 3. If the whole mobility is 1.5 times smaller, this could have being 1.5 and so

on. All right in such a case we will get 0.2 volts of VST minus VT. If you 1 again say that VT is 0.5 volts. So, VT of the PMOS is different from the VT of the NMOS normally. They are not related to each other. However they might be of similar values.

So, if VT of the PMOS is also 0. 5 then; that means, that I need a drop of 0.7 VSG has to be 0.7 which means which means this node has to be at 1.3 roughly and it all depends on all of these various assumptions that we have made in our calculation.

Now, how are you going to make that 1.3 volts, with the voltage source, with another battery? No right I hope not right. Do not use batteries over here. You are again going to use a current mirror. You are going to draw exactly the same amount of current through another PMOS and that is going to mirror it.

So, this is something that is not being drawn right now because that is not our focus right. Our focus is not over here you are going to generate the 1. 3 volts not with voltage source; certainly not with the voltage source not with the resistive divider, not with any of those techniques you are going to use. A diode connected MOSFET, pull a current through a diode connected MOSFET and generate the right voltage fine.

Now, the question is what is the maximum voltage over here? What is this swing? What is the maximum swing at the 2 outputs? What are the maximum and minimum voltages at the 2 outputs? So, what is the maximum voltage? Maximum voltage at which these 3 PMOSes still behave like a current source ok; As long as PMOS is behave like the current sources, you will get gain in the amplifier.

So, the voltage at which the PMOS still behaves like a current source is 1.8, why? Because VSG minus VT was 0.2 volts that is what we had chosen right and therefore, we source to drain, not grain to source has to be more than 0.2 which means if the sources at 2 volts then, the maximum tolerable voltage at the drain is 1.8 ok. And whatever is happening on the this side and same thing will happen on the other side is this fine.

So, now I know that the maximum voltage here is 1.8, is there a minimum. If I lower the voltage, the PMOS is happy. So, we do not look at the PMOS, who is going to start feeling unhappy; if I lower this voltage. The constraints are now going to come from the input device as well as the tail current source ok. This these 3 devices will start becoming unhappy, if I lower the voltage at the output all right. So, what is the minimum voltage?.

So, depends on the input. So, the minimum voltage now starts depending on the input voltage. Input voltage I just said, it as to be greater than 0.9 ok. I have not declared a maximum of the input voltage, but you see this to keep to keep the input device instauration, VDS of the input device has to be more than 2; Because VGS minus VT is 0.2.

So, if I want to keep VDS of the input device more than 0.2 and the gate is at a certain voltage then; that means, the drain, the lowest voltage at the drain is the gate voltage minus VT. Do you see at my point? If this is at 0.9, suppose if this is at 0.9, this is at 0.2; then the lowest voltage here is 0.4, but this is not necessarily at 0.9. If this is at 0.9, this is 0.4 which is 0.9 minus 0.5.

Suppose this was 1.2, this can be any voltage greater than 0.9 right. You are saying that I do not know what the gate voltage is. It can be anything that coming from the input. Input can be anything more than 0.9. Suppose this input is you know 1.5 volts ok. If the input is 1.5, then what is going to be the voltage at the source? 1.5 minus 0.7 0.8 at the source.

Now if the source is 0.8, then the lowest voltage at the drain is 1 which happens to be gate minus 0.5; gate minus VT ok. If the input difference of the 2 outputs, let us say small v in that is my input differential signal. If the difference between the 2 inputs is small v in; this is the plus terminal, this is the minus terminal. The operating point voltage over here is capital V IN capital V IN right. So, then this voltage is capital V IN plus v in by 2. This is capital V IN minus small v in by 2. Is this fine? So, far so good.

Now, I do not know the value of capital V IN, it can be anything more than 0.9. What is the voltage at which this minimum and the maximum are equal? Could it be that the minimum and maximum are equal? In basically there is no condition; in such a case there is going to be no condition, there is going to be no swing at the output. Output cannot I mean there is no condition at which both the top device as well as the bottom device are in saturation. Could it be? Could it be the maximum and minimum are equal? In that case V IN is 2.3 volts ok.

So, for example, if this is at 2.3, if capital V IN is 2.3; then what happens this is at 1.6. If this is at 1.6, then the lowest voltage over here is 1.8. The highest voltage here is also 1.8

which means that if I apply any signal at the input 1 of the 2 devices collapses, it is all gone back all right.

So, there is no flexibility at the input. You cannot really apply a signal at the input and hope that the amplifier works ok. So, this capital V IN has a maximum as well. So, it is limited in terms of range; limited from the top side, limited from the bottom side. If it is too large, then there is no output which will satisfy saturation of all the devices. If it is too small if this voltage is small, then the current source below is going to collapse and not behave like a current source.

So, this is the constraint at the two inputs. The input is constraint, not just the output. Now depending on the voltage, the actual voltage at the input the actual operating point voltage at the input; depending on that I get a swing at the output all right. Is this understood? So, the output swing limit actually it depends on the operating point at the input all right. Now this operating point is not necessarily a constant value. This could also be a common mode signal, a common mode an inference.

So, this capital V IN over here right; now I have written in capital letters indicating that it is a static value ok. But does this have to be static? As long as these 2 are equal that is can this be any interfere, can this be a common mode interfere? Can it be a sine wave both moving together? The answer is yes. It could be a sine wave, but if it is indeed a sine wave, then it should be in this range ok.

Whatever happens over there, whatever it is right whatever that common mode signal is interfere is; it should be within this range. Because outside the bounds the amplifier collapses, does not amplify any more. It does not amplifier, the differential input anymore all right. So, this is called the input common mode range. In short it is called ICMR.

So, this is the input common mode range. So, for this range of input common modes, this amplifier is actually going to amplify. If V IN is more than 2.3, then there is no output at which the things are in saturation and if V IN is less than 0.9, then once again the tail current source is outside of saturation and things are not really working.

So, this is called the input common mode range. This is the DC operating point value at the input for which the amplifier is going to work. This is not the input signal range. This

is this is not telling you, what is v in small v in ok. This is not this is not no bearing on small v in ok. This is we are only talking about capital V IN and we said that capital V IN does not have to be a static value, it could also be something which is changing with time. In any case whatever is changing with time that is that is an interfere and that will be rejected right. The rejection ratio is called the Common Mode Rejection Ratio CMRR.

Remember, we discuss it. Yeah CMRR ratio of common mode differential mode gain and common mode gain right; how much is signal to interfere at the output versus how much is the signal to interference ratio at the inputs all right. So, let us how much you are rejecting the input common mode signal? So, this input common mode does not have to be a static value ok.

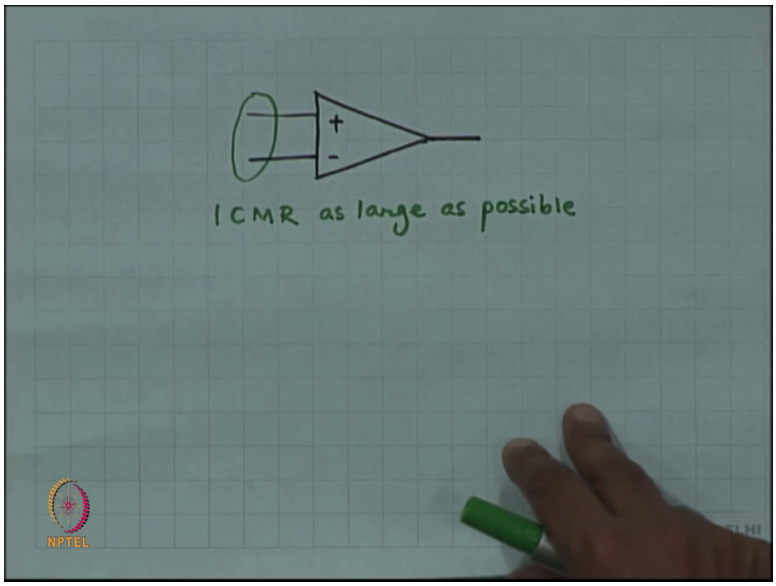
What is the input common mode? It is the average of these 2 inputs. The average of these 2 inputs right now looks like capital V IN and capital V IN therefore, need not be a static signal. It could be something which is changing with time and how much can it change? This is the input common mode range. As long as the input common mode changes within this range, I will be able to reject it.

Outside of this range, the input common mode, the amplifier will no longer behave like an amplifier which means that kinds of other things are going to happen. Differential gain is going to become much smaller right. Common mode gain is probably going to become larger in which case signal to interfere ratio at the output by signal interfere ratio of the input is no longer going to be large right; in which case the common mode signal will propagate to the output.

So, all kinds of bad things are going to happen outside of this range. Within this range, the amplifier will behave itself. Is this alright? Is this discussion ok? So, this has no bearing on small v in. How big or small v in can be? We are not talking about it. We are not talking about the difference the actual swing at the output the actual swing at the output is related to the value at the input right now ok.

Whatever I pick value capital V IN of capital V IN of accordingly, the actual swing of the output. The actual swings limits at the output will change ok. It all depends on what is the actual input common mode value is this ok; So far so, good all right great. So, this is an important discussion all right.

(Refer Slide Time: 31:08)



Lot of people want an amplifier. So, ideally you are trying to make this amplifier right. This is you something that you aware of. This is your op-amp right. The objective of this course is to make this op-amp, this amplifier where the output is proportional to the is a large game times the difference between the two inputs. This is what you are trying to make.

Now, this object is not going to be ideal. It is not just proportional to the difference between the two inputs right. There are constraints on the actual values of the two inputs. What is that constraint? The average of the two inputs has to be within this range, the ICMR range. Ok otherwise difference of the two inputs is not going to be amplified.

So, for example, for example, if my two inputs over here are 0.5 volt and 0.6 volt, then this amplifier is not going to amplify it; amplify the difference. Even though this is 0.5 this is 0.6 right. This device is now out of saturation. So, this difference of 0.1 is not going to be reflected in the truth sense at the output. So, I apply 0.5, 0.6; I expect this op-amp to work. It is not going to work because there is a range of inputs for which it will work. There is an input common mode range.

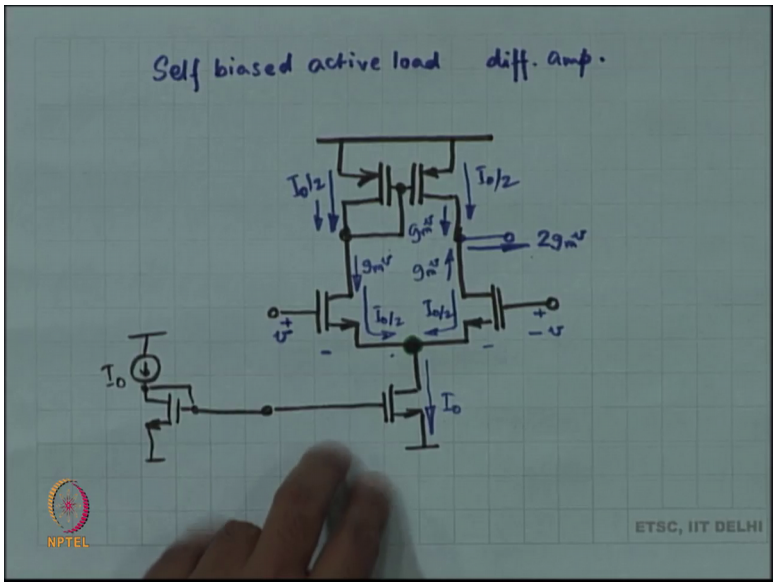
So, ordinarily when you are designing an op-amp, if you are planning to design a good op-amp. When you want to see input common mode range to be as large as possible that has not happened over here, that has not happened here because this device went out of saturation. All kinds of bad things happened right. We do not know; this has a lower

limit, this also has an upper limit fine. Are you going to try to solve the problem? No we are not right.

Now, we are not right now just exploring circuits. So, this is one circuit that we explore right. Now, I am not going attempt even attempt to solve the ICMR range problem right. We are not going to do it right away. We will do it later on.

So, there is one more strategy right. So, as you see when you are trying to make an op-amp, the output if you are trying to make the output could be single. The output could be double right. So, you could have two outputs, you could have one output. Ordinarily op-amp has only 1 output right. So, you do not really have to make two outputs like in this circuit. So, this circuit had two outputs. Do not required two outputs just one output is sufficient.

(Refer Slide Time: 34:59)



So, one other possibility; can we modify this op-amp and you know get some benefit, if I have only one output as opposed to two. So, now, all I am saying is am not interested in two outputs, I am interested only in one output ok. I can pick either one. I have picked this one today ok.

Today I have picked pick this one. Tomorrow I might slip over to the other side. It does not matter. So, only one output in the op-amp, can I take some? Can I make some

changes and take advantage? And the answer is yes, you can. Why not? Put a current mirror instead of two current sources, why not put current mirror on the load ok?

So, this is my plan. What is the plan? The plan is this is some current I naught. This is I naught by 2, I naught by 2 and then whatever this current is I naught by 2 that gets mirrored by the current mirror and I get I naught by 2 over here all right. And that way, you know remember in the earlier circuit you had to create this 1.3 volts right. This way I do not have to create that 1.3, it already self-created, itself biased. The load is self-biased, I just have to create this particular voltage which I do with a with the current mirror from outside. Some reference current with the mirror I create that I naught ok. The rest of it itself biased. Is there any advantage to this? Well there is, think about it.

So, if let us let us assume that this node is a constant fixed voltage. Remember when we talked about differential circuits, you did the half circuit and then the midpoint of the half circuit; if my two inputs are anti-symmetric that is plus delta V and minus delta V, then the node in between does not move ok. So, let us assume that the node in between does not move. Here this circuit is no longer symmetric right. The symmetry is broken, 1 half is no longer the mirror image of the other half ok

So, really I cannot apply that same principal over here, but let us assume let us assume that I apply delta V or small v, I apply and minus small v, I apply on the other side and this node let us assume does not move. Now if this node does not move, then this current is going to be g m times v. This current is going to be g m times v. And then on top I have got a current mirror. Now the correct mirror not only mirrors the dc, the operating point current. It will also mirror the signal right.

So, this current is now g m times v. So, therefore, this current is also going to be g m times v which means that 2 times g m times v is going to be pushed out on to the load ok. And the load in this case is nothing, but the combination of RDS of the NMOS and RDS of the PMOS ok, as long as you have not really placed an actual load.

If you place an actual load then fine, but if you do not place an actual load, then its radius of the PMOS in parallel with the RDS of the NMOS and therefore, the gain of the circuit is 2 times g m times RDS of PMOS times parallel with RDS of NMOS. So, you get an extra factor of 2, in the gain. Earlier what was happening ? Earlier this connection was

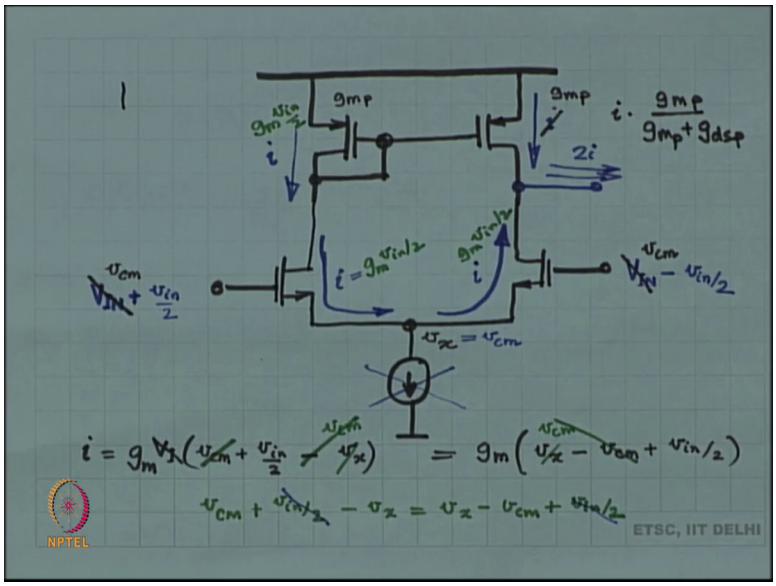
not there I naught by 2, I naught by 2 buys from outside. I had plus v over here, minus v over here.

So, when I have plus v this was static. So, this created g m times v; g m times v came through that load and created a voltage. Here I had g m v going by other way. If you think that this is a current source, then it goes out into the load ok. If you think of RDS, then that g m times v times RDS of the PMOS in parallel with the NMOS gives you the voltage at this node.

So, the voltage at this node is something; the voltage at the other node is minus of that something and that something is g m times RDS of PMOS in parallel with the RDS of NMOS. So, 1 is plus, the other is minus difference is 2 times. Here this one forget it. This current whatever is happening whatever signal current goes through gets reflected on the other one, 2 times g m v, it gets pushed out into the load which is RDS of PMOS in parallel with ideas of NMOS. And therefore, you get the same as the difference in the earlier case. In the earlier case, you got a differential output of 2 times g m times v times RDS of PMOS in parallel with RDS of NMOS.

Now just this voltage is 2 times g m times v times RDS of PMOS in parallel with RDS of NMOS all right. So, clearly there seems to be an advantage, seems to we have to analysis it nicely right. There is some scope in the circuit. Clearly this is this is a circuit that that no has potential all right. So, this is called the self-biased active load differential amplifier ok. So, the active load is self-biased basically with a current mirror and it is differential input single ended output.

(Refer Slide Time: 43:44)



So, this is what we are going to study next. So, this is going to be our agenda right now. So, let us study it in a little more detail ok. So, my two inputs are some common mode or and the same DC operating point plus v in by 2 and the same DC operating point or common mode minus v in by 2. And in the small signal, there could be a small signal part in this right the common mode interfere is a small signal.

So, potentially there is small signal here. But this is an open circuit in the small signal ok. In that case whatever current comes this way has to go up the other way. Whatever the current comes this way, this has to it has no choice this is open circuit in the small signal. Let us assume it is a open circuit not just a MOSFET.

Let us assume it is a good current source over here. In which case whatever current comes this way has no choice it has to make its exit, the other way. Nothing doing and then if you assume this is a good current mirror, then whatever current comes this way has to be mirrored the other way and therefore, the net output current is 2 times this current; the current created. So, you got some circulating current. So, if I create i over here, this is also i this is also i and this is i which means 2 i goes out into the load; this is our analysis right now.

Let us see let us assume the voltage over here is something some in the small signal. Let assume the voltage here is v x. So, if this voltage is v x in the small signal, then what is i? So, let us call it some common mode signal.

Now, this is i and minus i. So, i is going the other way for this particular one all right. This is so, g m times. So, what are your unknowns over here? Your unknown is v x and i. This are your two unknowns. The knowns are v c m and v in ok. You have applied v c m v in from outside and the circuit responded by creating a v x and generating an i and I want to know what is the value of v x. What is the value of i? What are they?

So, you got two equations i equal to so much and i equal to so much and this is equal to this; two equations, two unknowns. So, first of all you got this one equation where you got v x as an unknown and therefore, v x can easily be computed ok; g m times so much is equal to g m time so much, cancel out gm right that automatically tells you what? v x has to be equal to v c m ok; g m g m cancelled out, in which case this voltage over here is equal to this voltage here; v in by 2 politely cancels out; v c m you get 2 times v c m is equal to 2 times v x and therefore, v x has to be equal to v c m ok.

So, you have got no choice; v x has to be equal to v c m v x has to be equal to v c m and therefore, v c m minus v c m is all 0, v c m minus v c m is all 0. So, i is nothing, but g m times v in by 2. So, I applied v c m plus v in by 2 over here. v c m minus v in over here. v x was the same as v c m just by the way.

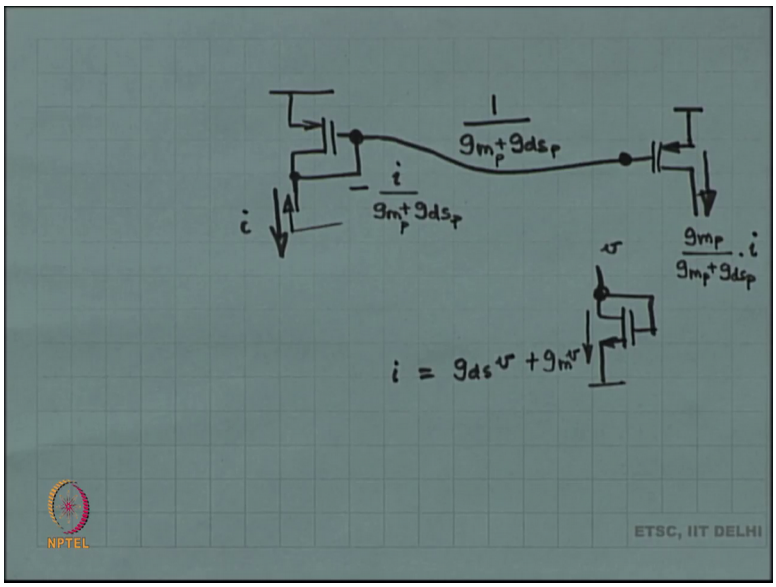
We assumed over here that the signal current through this current source is 0. Is that correct? If this current source was not ideal, if this there was a resistance here; what would be the signal current? The signal current would be v c m by the output impedance of the current source right. So, that would not be correct; however, v c m is a interference; If I say that there is no interference, if I assume that the interferer has already been gotten rid off; suppose.

Suppose the interferer is already not there, then this signal current is actually 0. So, if v c m happens to 0, this signal current is actually 0. In the other extreme, if I make a very good current source over here; then I can tolerate interference right. If I make a really good current source, then you know that is the same current this element completely disappears all right. So, i over here is nothing, but g m times v in by 2 that is the signal current i. The same current follows through it cannot go through the current source. So, it follows through and then what is going to happen?

When there is my current mirror over here all right. So, the current mirror needs to mirror the current. So, if I pull i equal to gm, if I pull some i current through the current

mirror; what is going to happen? What is going to be the voltage of the gate? So, suppose this PMOS has some g m ok. Suppose this PMOS has some g m all right. This is a diode connected PMOS. Diode connected PMOS means we have studies the diode. The MOSFET has gm MOSFET has RDS or GTS whatever you want to call it ok, in which case the impedance looking in over here right.

(Refer Slide Time: 53:45)



If I draw current i through this MOSFET, then the voltage here is going to dip by a certain amount. How much is that? What is the resistance of this? Resistance of this is 1 by oh you have forgotten everything ok. You want me to do this all right. Let us first of all you are not comfortable with PMOS and all growing about the PMOS fine. Let us draw it with an NMOS. It is the same thing ok; the PMOS and the NMOS have no difference alright. So, do not worry about it. So, let us look at an NMOS.

Now, to find the impedance of this circuit, you can do it in two ways. You can push our current measure the voltage or you can apply of voltage measure the current. Both are ok. Which one do you want to do? Let us apply the voltage and measure the current. So, let us apply a voltage v here. If I apply a voltage v at the gate, then g m times v current is pulled through the drain, but also remember there is an RDS from the drain to the source. I have applied v voltage across that RDS which means that that will also create a current, a drain current.

So, the net drain current is g d s times plus g m times v which means if I applied v, I get a current of so much all right and therefore, the resistance is 1 by g m plus g d s v by i ok.

So, let us hammer this in your head. Approximately this looks like 1 by g m. So, whenever you have a diode connected MOSFET. It is approximate impedance is 1 by g m. If you want to be accurate, then it is 1 by g m plus g d s; no g m b is not playing any role over here at all because the body is ground the source is also at ground, small signal ground. So, g m b is not making doing anything. So, the impedance of this MOSFET is of this diode connected MOSFET is 1 by g m plus g ds. I pulled the current i and therefore, the voltage over here has to drop because I am pulling the current out. So, the voltage over here is going to drop by current times the resistance fine.

Now, this same voltage is being applied to another MOSFET. The same voltage is being applied to another MOSFET. How is that one going to respond? This is the voltage I have given the voltage value of the voltage. So, this MOSFET is going to try to push a current which is g m times this voltage. So, the current that is being pushed is nothing, but g m p by g m p plus g d s p times i. So, I am pulling a current i through this MOSFET. It responds by dipping this voltage ok.

Now when the voltage has dipped, the other one tries to push a current which is g m p times the dip. So, this is not really i. This is i times g m p by g m p plus g d s p. If you want to be accurate, all right. And now you sum the 2 currents; you got the i, the other one and this sum which is almost to i, but not exactly is going to be pushed across the Norton equivalent impedance right. Remember this did not move

So, the Norton equivalent impedance is RDS n in parallel with RDSP and that will create a voltage ok. So, let us stop here and we are going to discuss further maybe analyze the circuit in even more detail. Lot of you are unhappy about this analysis that you do not like it fine. We will analyze it in more detail in the next class.

Thank you.