Analog Electronic Circuits
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Lecture – 14
Current sources / mirrors contd

Welcome back to the Analog Electronic Circuits lecture series. Today is going to be lecture 14 and we are going to continue where we left off on our discussion on Current Sources and Current Mirrors.

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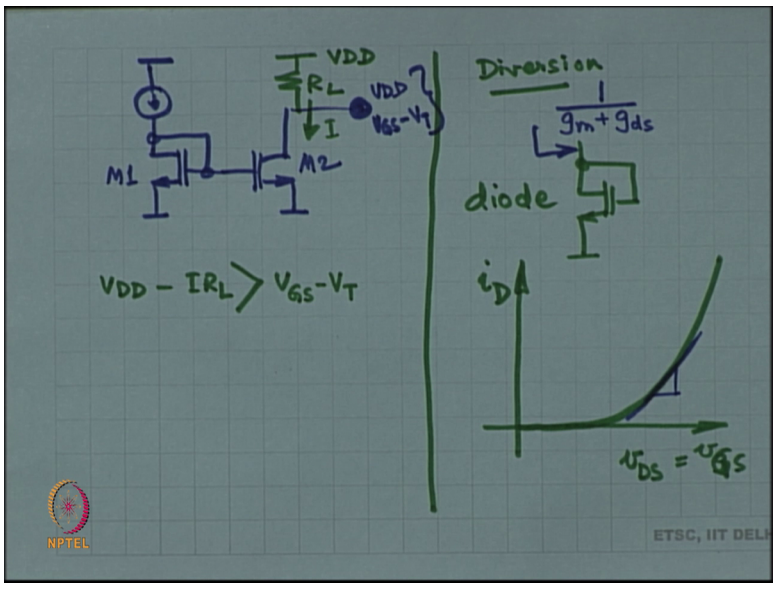

So, in the last class we looked at a basic current source the basic current source was just the MOSFET as long as it remains in saturation and then we said that we need to sort out a few problems. One is what is the value of this current source; so, then what we what did we do? We placed it around the mirror. So, I used a reference current source. The reference current source provided the value it. It created the right voltage VGS for M 1 such that it conducts the reference current and then that right voltage VGS is applied across M 2 across VGS of M 2 to create a copy of the reference current.

Now, this copy of the reference current need not be an exact copy, it could be a proportional copy. So, for example, this 1 milliampere, this we could make 0.1 milliampere. We could make 1 milliampere, we could make 10 milliamperes, 100 milliamperes whatever you want. So, this is as far as we had discussed.

The next thing is what about its output impedance and then we measured the output impedance of the circuit looking in from outside, the small signal output impedance of the circuit happened to be just about r d x and nothing else ok. A brief note, this structure this structure is called the diode connected MOSFET, why? Because it somewhat behave like a diode. If you look at the VGS i D versus VGS curve right, you are guaranteed to be in saturation which means it is guaranteed to follow this particular curve right. An i D sorry VGS happens to be equal to VDS in this case.

So, now this is a VDS equal to VGS on the x axis, on the you know axis its i D. So, this looks like the curve of a diode. So, this particular structure is also called a diode or a diode connected MOSFET. What is the impedance of this? The impedance of this is the slope of this curve right and what is the slope of this curve? What is the slope of this curve? This is k times VGS minus v t the whole squared.

So, the slope of this curve is the same as g m. So, the conductance between these two nodes is gm. The resistance is 1 by g m. If you look at the small signal equivalent picture of this, you will see that it is not just g m. There is g m because of the current voltage controlled current source. There is also g d s because of the resistor. So, the effective impedance is g m plus g d s effective conductance. Looking into the node is 1 by g sorry; the effective conductance is g m plus g d s when you look into the drain terminal drain or gate terminal ok; g d s is just a small edition on top of g m.

So, this analysis is more or less correct ok. The slope of this curve is g m, gds is a small addition on top of it alright. So, this is side note. This is just for future diversion alright. So, getting back to our current mirror circuit. So, we looked at two things; number one, we looked at was value. The value is obtained from the reference. Number 2, we looked at is the output impedance; the output impedance of this is nothing, but rds ok. Number 3 is what is the set of voltages for which M 2 remains in saturation and the device actually works like a current source? And for this we have to work out the load.

So, suppose you got a load to a voltage VDD ok. So, VDD minus I times R L has to be more that is VGS that VDS that has to be more than VGS minus T ok. Now what this automatically means is that if VDD is large than this range increases right. I can have more I can have more R L. If VDD is fixed and then and RL is fixed, then I have a limited choice of the values of I. If VDD is fixed and I is fixed, then I have a limited set

of values of R L for which the circuit will work as a current source ok. So, basically the range of voltages over here maximum VDD is minimum VGS minus VT right. In this range, it has to be there. If I increases, then R L has to be lower. If VDD increases, then very good VDD decreases. These have to be smaller and so on and so forth alright. Is this understood? Ok.

Now the big question is it is not what you see is what you get. You should be able to improve right. So, if your boss tomorrow says that ok, I do not like and output resistance of RDS may give me a better current source, what will you do?

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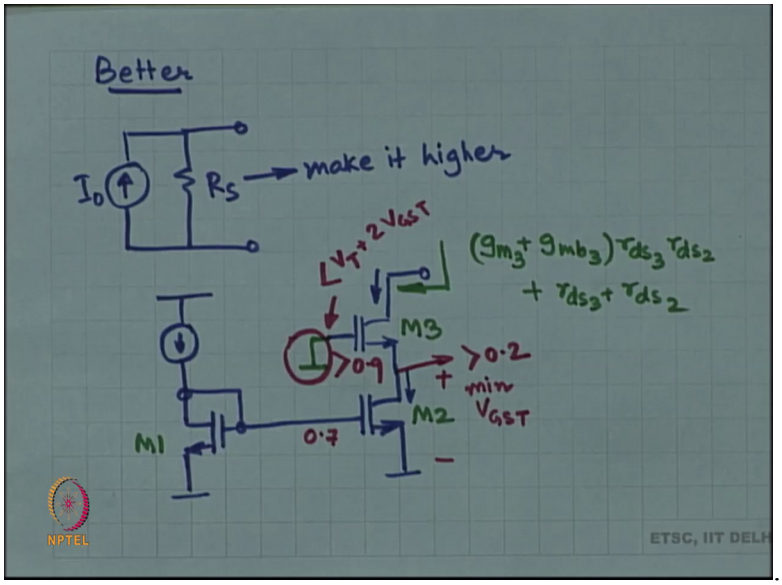

So, if I want to make a better current source, I have to improve upon the value of the source impedance right. The model of the current source is like this. If I want to make the current source better then R S has to be made higher in value for the same value of current. How will you do that? How will you get a higher impedance? By adding a common gate stage right; common gate stage was the current controlled current source.

So, if I add a common gate stage on top of this basic current source, then what is going to happen? The output impedance that I see now is going to increase because now the output impedance is the intrinsic gain of M 3 times r d s 2 plus r d s 3. So, this output impedance is nothing, but g m 3 plus g m b 3 times r d s 3 this is the intrinsic gain of m 3 times r d s 2 plus r d s 3 plus r d s 2 and g m 3. This intrinsic gain is large right. It could be something like a 100. If this is 100, then I have 100 times r d s 2 which is much larger

when r d s 2 right. What about the current? The value of the current remains the same. This current continuous to come up through the drain right; There is no change in the value of the current all that changed is that the impedance became a lot higher. So, this suddenly is a much better current mirror than original one. All I did was added M 3 and cascode.

Now, if you are not if you want to make it even better, even better would be to add even one more device in another cascode right. Put M 4 in for the cascode on top and now you have an even higher output impedance and then you could keep going right. This what people used to do long time back right. Unfortunately you are going to pay a price. The price is that when you add this one device on top in cascode.

Now the range of voltages for which it works, this range is going to become even more limited. Your swing allowable swing on this node is more limited ok. We will look at that later on. But for now, do you understand that the impedance became a lot higher just by adding M 3 in cascode ok. We already studied the cascode just by adding this common gate stage on top.

I have got a much higher impedance great. What is the potential over here? Should it be ground? Ground is the small signal picture in the small signal incremental picture. It should be ground, but ideally it should not be ground. It should be a value. If I put ground over here, really if I put ground, this is above ground. So, VGS is negative. So, this M 3 is not going to conduct any current; that is going to be disaster ok. It is not going to work, if I place work ground over there. Ideally this should be some voltage which is reasonably high such that M 2 remains in saturation. M 2 requires a minimum voltage ok. How much voltage does M 2 required? It requires VGS minus V T alright. So, this is called VGS minus V T is called VGST alright. So, M 2 requires VGST of voltage across drain to source. This node should be a voltage; high enough that the voltage at the source is more than VGST. This is the minimum. The minimum voltage across drain and source of M 2 is VGST ok. It can be anything higher than that.

So, this should be such that if I drop out one v GS, then I have at least VGST. So, this node should be VGST plus VGST of M 3 plus VT of M3. So, in other words, if I assume that all these devises are identical VT is also identical. Suppose I assume ok, then this

voltage should at least be VT plus times VGST; at least anything more than that is ok, anything more than that is.

For example, if a you know your VGST is 0.2 volts and VT is 0.5 volts, then the voltage here is 0.7 right. The minimum allowed over here is 0.2 which means that the minimum allowed over here is 0.9, but then there is no maximum. It can be anything about 0.9 ok. If I do keep you know, if I keep let us say I keep 1.5 instead of 0.9 right. It can be anything about 0.9. Suppose I place it at 1.5 that is write again.

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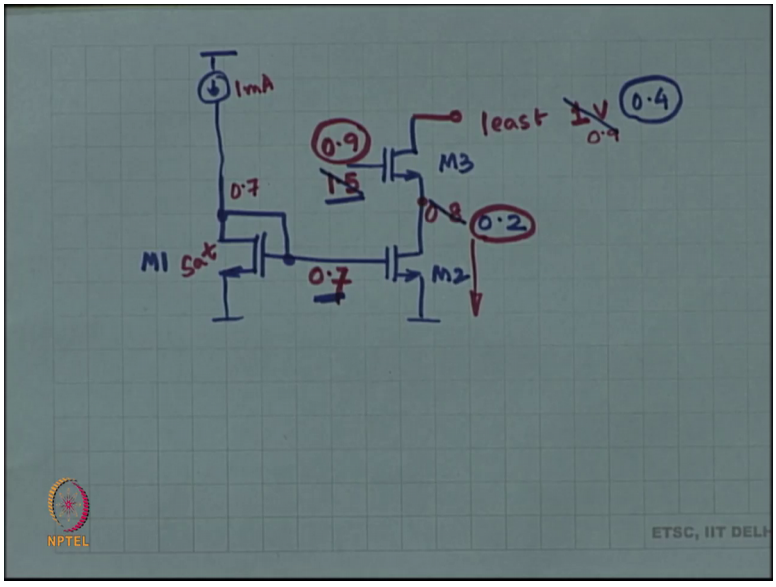

So, what have done so far is I have declared that VT is 0.5, then VGST is 0.2 so, for all the devices. So, these particular nodes is at point 7 the minimum over here is 0.2, but let us keep it at point 0.8 and let us place this at 1.5 right. How I place this? At 1.5 is you know you do your thing. You put your resistor. Do whatever you want. Place this node at 1.54 ok. So, this node is biased at 1.5 volts. Automatically this is a small signal ground. Alright this is at 1.5, this is at 0.8.

Now what is the least possible voltage at the output such that both of these devices are maintained in saturation. I have fixed this at 1.5. As soon as I fix this at 1.5, by the way this is 0.7 ok, 0.7. This is also 0.7. This device is never going to go out of saturation. This is permanently in saturation all the time. You do not have choice about here. If this is at 0.8, this device is also certainly in saturation which is fantastic ok.

Now, if I drop the voltage here, how low I can drop? To maintain M 3 in saturation, what is the least voltage at the drain of M 3? How much? 1 volt is the least ok. If you go below 1 volt, then what is going to happen? M 3 is going to go out of saturation. Is that right? Ok. But then what is going to happen? Suppose I do go below 1 volt, what is going to happen? M 3 is going to drop out of saturation, but M 2 is still trying to conduct the same current right because M 2 still has 0.7 volts across VGS right; VDS we do not know, but hopefully let us make this you know 0.9. Let us drop it 2.9 ok. When I have dropped it to 0.9, the now the VDS over here is 0.1 ok.

So, for VDS of 0.1 and VGS of so much, the current works out something smaller than the required 1 milliampere. So, then VDS has to increase slightly VGS has to increase slightly right. So, let us increase the VGS are little bit, in which case instead of you know 0.7 v GS, I now need a little more v GS. Let us say I need 0.75 VGS right. So, this is going to drop to 0.75. If I drop this 20.75, then this device is still in saturation. So, it is still conducting 1 milliampere. This I have given a little more margin, I have increased it 2.75 as opposed to 0.7 and over here VDS is now 0.9 minus 0. 8, 0.15 ok. So, very adjust.

So, the source drops in voltage a little bit. So, when I decrease this, below 1 volt; this source is now going to dropped from 0.8. It is no longer going to 0.8. It is going to go down right. How much it goes down depends on, these other voltages the device parameters and so on, but M 2 is still in saturation which means that 1 milliampere is still being conducted ok. What about the output impedance?

The quality of the output impedance has become a litter verse, why? Because this device is no longer in saturation; so g m 3 times r d s 3 has dropped. The intrinsic gain of the device has dropped right. It is no longer that large 100 number that it use to be right. The output impedance is the intrinsic gain of M 3 times r d s 2 right. That is the biggest factor right, the remaining portions are small.

So, intrinsic gain of M3 times r d s 2 plus r d s 2 plus r d s 3 right, forget the plus portions; intrinsic gain of M 3 times r d s 2. If this device drops out of saturation, then the intrinsic gain of M 3 reduces substantially which means that the output impedance of the entire circuit reduces right. It would not be as large as it use to be; however, it still conducting the same current. So, that is very nice right. So, this degradation is very

graceful right. You will find that you go down to 0.9, then 0.8, 0.7, 0.6. It is still going to conduct the same amount of current right; just that the impedance now is dropping right. The amount of incremental change that you are going to get is going to be more. The impedance, the output impedance is going to drop, but the degradation is very graceful alright. Is this understood? ok.

So, next let us see what happens; if I do not place this at 1.5, if I place this exactly at. So, the minimum I needed over here was 0.2. So, I want to place this exactly at 0.2 and therefore, I place the gate over here exactly at 0.9. Now what is going to happen? The least is no longer 1 volt. The least is 0.4 volt. Now when I drop below 0.4 volt immediately, this source is going to drop.

But when this source drops M 2, no longer is in saturation which means that this also drops out from being a current source ok. So, the graceful the degradation is no longer there right. The entire circuit collapses as soon as you go below 0.4 volts alright. Is this ok? So, there is some positive, some negative. You can keep this exactly at 0.9 and this exactly at 0.2. In which case, you have more range instead of the least being 1 volt. Now the least is 0.4 volts from the top. So, that is more room on the top; more head room we call it ok.

So, this gives me more head room, but then as soon as it goes below this the circuit collapses, it is no longer a current source whereas, in the earlier case, I kept the set 1.5 and this at 0.8.

So, now the least was at 1 volt much higher than 0.4; however, I had room right. I had room for degradation that is at if the voltage here was above 1 volt, then the output impedance would be fantastic; however, as I keep decreasing the voltage below 1 volt the output impedance deteriorates; however, the functionality of the circuit remains. It still remains a current source ok.

So, you have to look at the pros and cons of the 1 1 1 case. You have a positive and upside right that you have got graceful degradation. On the other hand, you have a down side that the range is much more limited right and in this case the upside is that the range is much more the voltage range, the head room is much more; however, there is no graceful degradation as soon as you cross below 0.4; your done for ok. So, these are the pros and cons.

The next question would be how do I make this 0.9 volts and this I had you know brushed aside I said that you do whatever you want. You can place your resistors and so, on and so forth and create 0.9 volts, but do not in general do whatever you want right. There are some nice ways to generate the requisite voltage over here at the gate of M 3. So, one very nice way to generate the gate voltage of M 3 is as follows.

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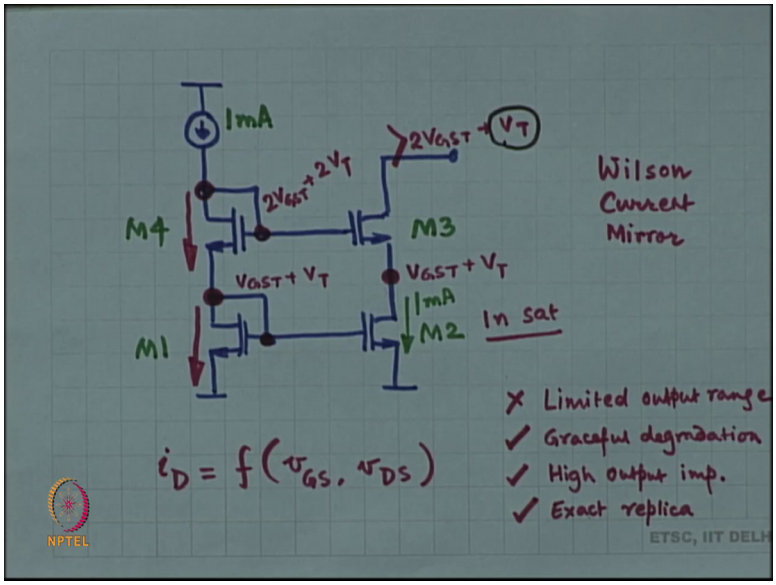

Assume all the devices are identical. So from this page, what is the difference? I have added one more device on this side on the reference side alright.

So, let us look at the reference side quickly. This my reference current. Let us say 1 milliampere. Where does it go? Does go through this square? No, it does not because the gate current is 0. So, all of that current goes right through and all of that current goes right through. This is a diode, This is yet another diode. So, I have got one diode, another diode. This voltage at let us label the MOSFETs ok.

So, the voltage across at the gate of M 1 is just the right voltage that M 2 will conduct the reference; 1 milliampere. So, this is 1 milliampere. This voltage is just correct; such that the current over here is also 1 milliampere as long as M 2 remains in saturation. What about M 4? What is this voltage at? This voltage is at V GST plus VT ok.

Now, let us assume all devices of the same V GST and the same VT, in which case what is the voltage here at the gate and drain of M 4? This is a diode, this is also a diode. So,

the same diode drop is going to come across M 4. So, this is going to be 2 V GST plus 2 times VT alright

Now, M 3 is going to conduct 1 milliampere; the same1 milliampere and therefore, the gate source voltage of M 3 is also V GST plus VT which means that the voltage over here, this is 2 V GST plus 2 VT. So, what is the voltage over here? V GST plus VT fantastic right; V GST plus VT. What does this mean? Is M 2 in saturation or not? M 2 is in saturation why because drain to source voltage is equal to V GST plus VT which is certainly more than V GST ok.

So, M 2 is certainly in saturation guaranteed to in saturation ok. M 2 is in saturation. What is the minimum voltage that you can tolerate at the drain of M 3? V GST plus VT is the source of M 3. So, the drain of M 3 can go all the way to 2 V GST plus VT. So, as long as you are greater than this limit, then M 3 is in saturation M 2 is also in saturation right. Then if you surpass this limit, what is going to happen? This voltage is going to the source of M 3 is going to drop. It is going to drop a little; however, M 2 will remain in saturation. So, this the graceful degradation that is going on.

You have got some room right. The lowest possible voltage here is just V GST, but actually the voltage is V GST plus VT which means you have got room for graceful degradation of up to VT.

Now, there is one more thing to observe;one more very nice feature of this socket. Really nice feature of this socket is as follows. This device the MOSFET right, the mosefet id is some function of VGS and VDS alright. Now i D 1 has VGS and VDS both equal to be V GST plus VT. M 2 also has VGS and VDS both equal to V GST plus VT which means that the current in M 2 is exactly equal to the current in M 1. They are identical because both VGS and VDS are equal in the 2 devices.

Now this feature was not there earlier. Earlier whatever we did right here, this drain was at 0.2 this drain was at point 7. So, VDS was different VGS was equal, but VDS was different which mean that there could be a slight difference between the actual current in M 2 and the current in M 1 right. Here in the other case VGS was 0.8 VDS was 0.8 VGS was 0.7 for M 2. But in the reference device VGS and VDS are both 0.7. So, once again the currents are not exactly identical ok, about in the one transistor situation.

In the one transistor situation, once again in the reference VDS and VGS are equal, but in the output device VGS is something, but VDS is completely depending on the load resistor ok. So, VDS is totally different which means that the current will have a lot of error. Where as in this case both in M1 and M 2 VGS and VDS are identical and therefore, the current is going to be exactly precisely equal alright. Is this understood? So, this is also a very nice feature. So, this particular current mirror is called the Wilson current mirror named after the gentleman who designed the circuit for the first time.

So, this particular current mirror has one important features that both M1 and M 2 conduct exactly the same current unlike in the other versions. If this is one milliampere, this is exactly one milliampere that is one important feature. Then the next important feature is that have got graceful degradation in terms of the limit for the output voltage. The output impedance is generally very high right. You have got a cascode. So, therefore, the output impedance is very high; however, this output impedance is going to go down. It is not going to be remain as high, if you go below this limit to V GST plus VT alright.

The next the only problem is that this limit is fairly high. It is 2 V GST plus VT or rather 2 V GST, this factor is extra right; 2 V GST plus a VT. Whereas, in the optimal case, I only need V GST across drain and source and another V GST across drain and source bit which means that in the optimal case, the lowest possible output should just be 2 V GST right. In the optimal case, in this case it is 2 V GST plus VT. So, the output range is suboptimal; however, it promises graceful degradation beyond the output range. So, this is a bad, then good is graceful degradation and then another good is high output impedance and then another good is exact replica alright.

So, there are some good things. There is this extra cost ok. So, this is very popular current mirror. It has a name Wilson current mirror. It is used very frequently in a lot of circuit. There is an extension to the Wilson current mirror. It is called the modified Wilson current mirror and I will briefly draw it over here. But this is a fantastic circuit and I am not going to explain how it works ok.

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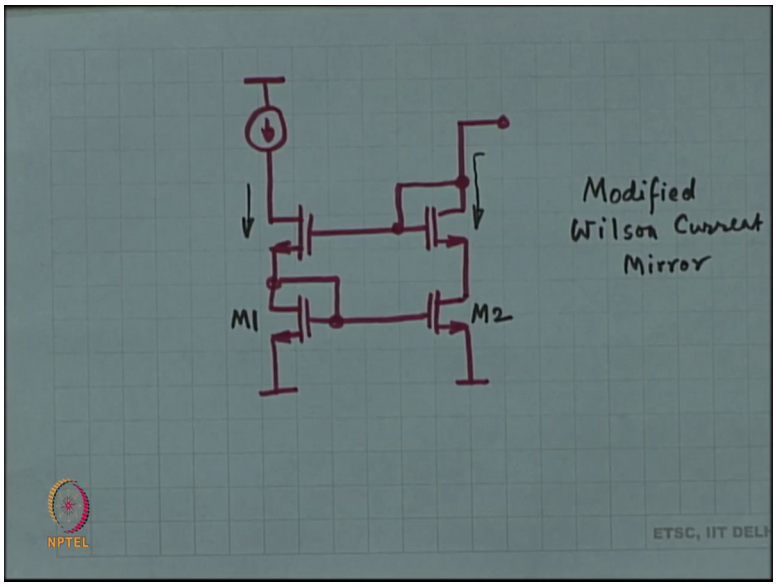

So, this is called the modified Wilson current mirror. This is just an extension to the original Wilson current mirror right. The only difference being that this connection is now on the other side and this also behaves very similar, the performance is very similar to the original Wilson current mirror. If you look at it carefully, you got the reference current; the reference current comes right through creates a drop across M1 right and this is mirrored in M 2 fine. But then what is this doing and what is the other do ok. So, that is just making sure that this current, this output current is equal to the reference correct. So, it is mirroring this current. It is copying this current over on this side ok.

So, anyways so, this is something that we are I am not going to explain right now, but this is called the modified current mirror. This you can think about it. But we are going to explain it later on. We are going to study it, just not right now. It is going to be towards well towards the end of two-thirds of this course ok.

So, in the first two-thirds of this course, we are not going to study be able to study this. We need to learn a lot more before which we can analyze the circuit. Right now I cannot do it. So, these are my current mirrors. Now if you think about it very carefully, you can add more stages alright and that is only going to give you more output impedance at the cost of even more limited output range ok. You can add keep adding more stages ok. One popular question is this is a suboptimal in terms of output range; this Wilson current mirror is not really optimal instead of in terms of output range, I wanted v G exactly 2 V

GST and not 2 V GST plus VT. Can that be arranged? Ok and the answer is possibly we can arrange that also.

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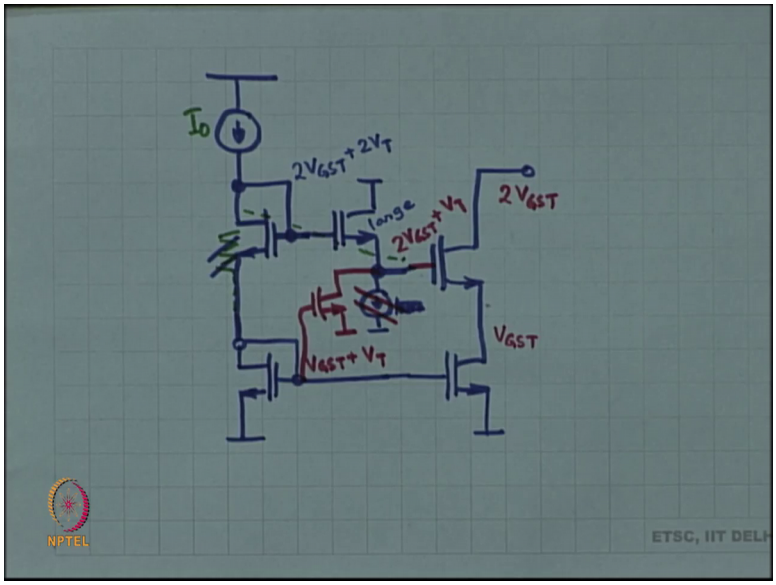

It is not very difficult; however, we are going to be unable to carry on with this exact replica criteria. It is no longer going to be an exact replica because this is now going to come 0.2, this is point ok. So, this is the basic premise. I am going to push this reference current right through this device and then mirror it and then common gate all right and now I have to make sure that this is at VGST which means that this node is at 2 VGST plus VT and the lowest this and therefore, go to is that 2 VGST. This is what I have to make sure the voltage here is VGST plus VT.

So, one easy way one easy way is to you know place a resistor over here, right of value VGST by I naught and connect this hope this. So, this is now exactly VGST. So, this is 2 VGST plus VT right, but then you need to know exactly what is VGST and what is I naught and therefore, this resistor has limit has limited value alright. So, that that becomes a problem. What are the possibility is there? Another possibility is that; let us not bother about this. We have this MOSFET and we know that this creates a voltage over here of 2 times VGST plus 2 times VT, but I need to draw VT below that alright and one easy way of doing that is to push to pull a large current through a MOSFET sorry; to push a current through a large MOSFET ok. So, if I push a small current through a large MOSFET in the VGST required is going to be minimal. Almost equal to 0 in which case

I will just get a VT drop. All that I now have to do is pull a current through this very large MOSFET.

So, you may take a very large MOSFET w by l is very large as opposed to these 4 having equal w by l, over here you pick w by l to be very very large ok. When w by l is very large that k factor is very large right. If I pull the same current through it, then what is going to happen? If I full the same current or a similar current through a very large k then VGS minus VT the whole squared is small which means that VGS minus VT VGS is more or less equal to VT

So, this drop is going to be equal to a VT. All I now have to do is pull a very large current. How will you pull a very large current? I am sorry reasonable current more or less equal to this. So, put in other mirror over here oming from the same reference alright. So, what have we done?.

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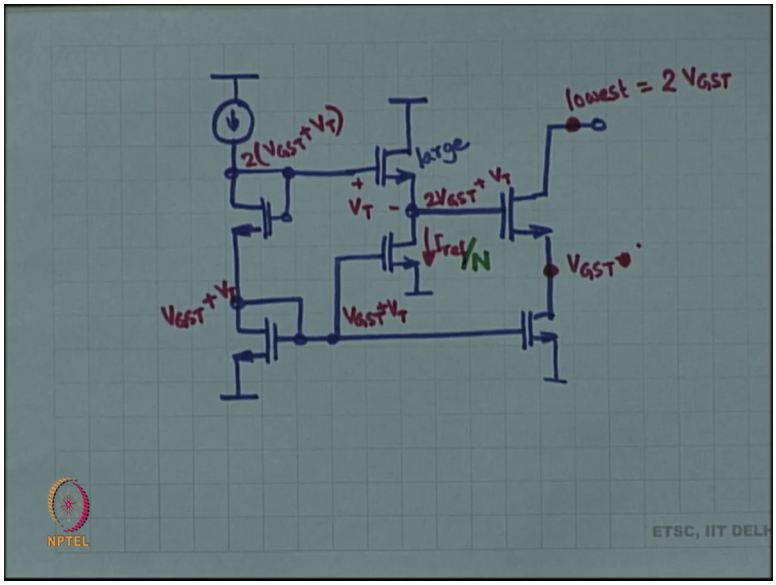

So, this was my reference current. This is my final device ok. Now I do not like this voltage. I take this voltage and I pull it down by VT volts and the way I do it is with the help of a device very large device with very large w by l the ratio. So, that VGS minus VT is almost equal to 0 which means that this is just a VT below the voltage over here. So, all these other devices are equal in size. So, the voltage over here is VGST plus VT. The voltage over here is 2 times VGST plus VT. The voltage over here is VGST plus VT. This current is also I ref more or less ok. It does not matter if it is a little less, it does not

matter because this device has to be large that is all. This drop has to be VT which means the voltage here is VGST 2 times VGST and that automatically means that the voltage over here is VGST which is the lower optimal limit at which this voltage can be.

So, this maintains this device in saturation and therefore, the lowest voltage that this can go to is 2 times VGST ok. Is this more or less clear this setup? So, these are all more and more optimized current mirror circuits that you can make. You can design your own current mirror circuit, I mean you do not have to have I ref over here for that matter right. I ref means now you are you have one reference current, another reference current, a third reference current. You are wasting a lot of current.

So, make this one very large. So, that this current is very small ok. You need you need a very small current over here. So, you do not really need I ref. You can have Iref by a large factor n right and you will save some current you will dissipate less current. This will still drop of a VT and that automatically means that you will get 2 VGST plus VT voltage over here. Is this alright? Ok.

So, we are more or less done with the current mirrors. So, these are a variety of current mirrors. Now I want to discuss one more socket. A lot of times people say that you want to make a reference current source. So, everywhere I have been drawing this reference current source right. I mean all the activities are being pinned on this reference current source. Everything is proportional to this reference current source. How do I make this reference current source?

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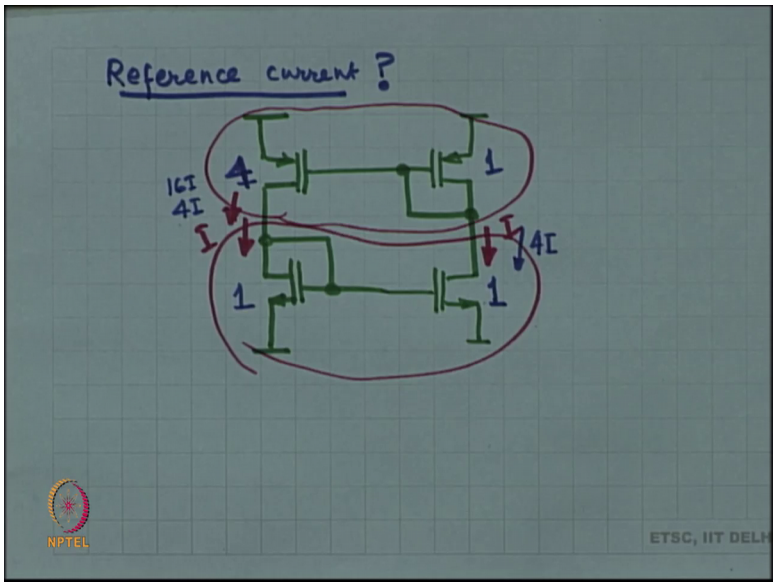

How do I make it? Any idea? ok. So what I am going to do right now is to give you some ideas to make this reference current source and then we are going to expand on the idea and we are going to make a certain kind of reference current source ok. So, this is just general discussion. These are not real circuits. Suppose I make a current mirror that looks like this; w by l ratio is 1 w by l ratio is 1 and w by l ratio is 1 n 1. What do you think is going to happen? You have got a current mirror alright. By the way I need you to now start remembering things ok.

When you see this, what is this? This is a current mirror current coming n over here, current being created on the other side alright. I need you to remember these patterns in the circuits because when you when you use these, this is a block this is a current mirror block alright. This is also a current mirror block and you have to identified these blocks. You cannot start treating every device on its own and looking at its characteristics and so on.

That is no longer I means you are no longer in class 10 right. You are not in class 10, class 11, class 12 right. You are studying engineering. You have to move ahead. So, when you start moving ahead, you start recognizing patterns. So, this is a pattern this is this circuit is a block right. This has a patterned. This is a current mirror right. You have to identify the current mirror and then use it accordingly in your analysis.

So, if I have a circuit like this, I have got a current mirror on the bottom, a current mirror on the top. What is it doing? So, if I have a current on this branch; let us say this is I, then this current mirror the bottom NMOS current mirror is going to reflect it and create I and what is the PMOS current mirror going to do.

It is going to reflect the I and create it on the other side, enforce it on the other side. Is this ok? It is a funny circuit right. It is not really doing anything much. What can be a possible value of a I? I could be anything. We do not know. Looking at the circuit, we do not know what is the value of I over here. All that I know is if I have a value of I over here that is going to be mirrored and that is going to be mirrored back, what is that value I cannot tell ok.

Let us modify this. Let us say I make this four times. So, 1 is to 1 and 1 is to 4. So, if I start with the current I, the NMOS mirrors it and makes it I and then the PMOS mirrors it and makes it 4 I. What is happening? Then 4; I gets mirrored right and then the PMOS mirrors it and makes it 16 I ok. So, it is not really converging right. The answer is not even converting alright. So, if 16 I has to be equal to I, then I must be equal to 0 ok. So, I in this case is going to be equal to 0 all right. So, I am just trying to play around over here to get you comfortable with using these current mirrors alright. How about this?

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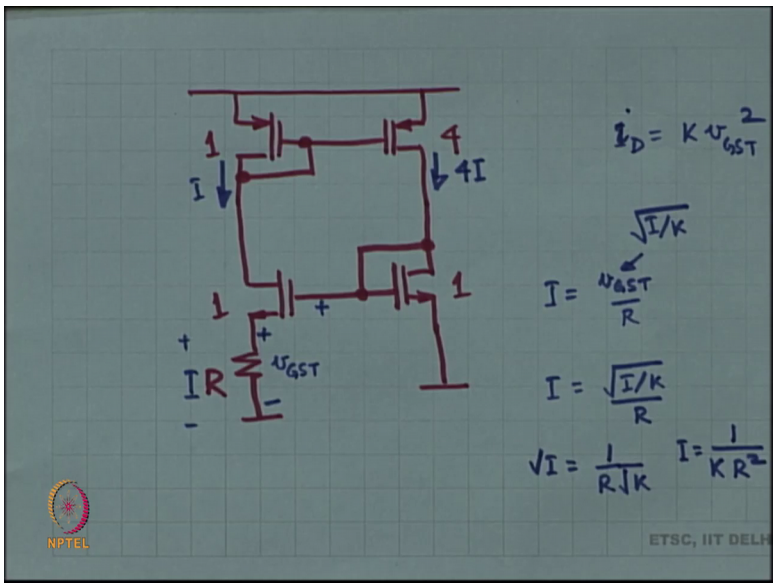

So, I have change the circuit slightly. In fact, I have drawn it the other way. So, I have mirror the circuit around itself, around the vertical axis I have mirrored it ok. So, these

are similar this has been mirrored like this right. So, you have got the current mirror is now on the other way right. The PMOS current mirror is the other way that is ok. It is nothing very significant, just topological representation, but what is more important is that have added a resistor R over here. How is this going to work?

So, let us start with the PMOS. If I have some current over here I, then the current on the PMOS side is going to on the other side is going to be 4 I. This 4 I current that is the reference current; it is going to create some voltage drop, VGS right. Now this is going to appear across the MOSFET as well as the resistor. So, I current is coming. The drop across the resistor is I times R ok. The drop across the MOSFET is going to be the requisite VGS minus I times R the requisite VGS for 4 I minus I times R. So, the requisite v GA for 4 I VGST of 4 I is going to be 2 times the VGST of I right because square law k times VGST squared is I ok. So, if I is 4 times, then VGST is 2 times.

So, the requisite VGS is 2 times the VGST plus VT and here I have got only VGST plus VT which means that the remaining VGST is over here. So, this is just a VGST for I which means what is I? I is VGST by R where what is VGST? VGST is I by K square root alright and that gives you some current, square root square root cancel out.

So, square root I cancels out and what you get is that root I is equal to 1 by R root k or in other words I is equal to 1 by K R squared ok. This is something interesting. You are actually getting a value for a correct over here as opposed to earlier. So, earlier in this case first when everything was 1 1 1 1, you got any value; then I made this into 4, now you got a 0 value. Here you are actually getting some value now rights. Things are getting better ok. So, we will proceed from here in the next class.

In this class we discussed better current mirrors, current references, how you organize the bias voltages everywhere. We discuss the Wilson current mirror and then I showed you the circuit for the modified Wilson current mirror, how in the Wilson current mirror you are getting graceful degradation. Then we even developed the circuit for optimal voltages the best possible current mirror, but this does not create an exact replica ok. So, let us stop here. We will continue in the next class.

Thank you.