Analog Electronic Circuits
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Lecture - 10
Swing limits

Hello welcome back to Analog Electronic Circuits lecture 10. So, in today's lecture, we are going to continue from where we left of in the last class and we are going to discuss Swing Limits. So, in the last class what we were at the end looking a, so we had in detail discussed the three different topologies; common source, common gate, common drain circuits. We had discussed input impedance output impedance. We worked on two important formulae that I hope you have memorized right; one is the impedance looking into the drain when the source is terminated by a resistor and the other is the impedance looking into the source when the drain is terminated by a register, in both cases the gate is grounded.

So, in the first case where you looking from the drain impedance multiplies; whereas when you looking from the source impedance gets divided ok. So, these area few things that we had looked at; then we looked at the source degenerated amplifier where you start observing what happens, when at the source you have a resistor and do not have a short to ground which is usually the case in the common source amplifier. So, these are the different topologies of single transistor amplifiers right. And we are now going to proceed with a discussion where the signal is no longer small.

So, in general all the discussions before this where we worked out the gain and so on and so forth, these where all small signal right; all this analysis was done in the incremental picture. So, if I incrementally increased if I incrementally change the voltage at the input what is the incremental change at the output? So, that is what we had looked at so far. What happens when this when the change at the output is no longer incremental? So, let us try to understand what are the limitations of our circuit and these limitations are called the swing limits.

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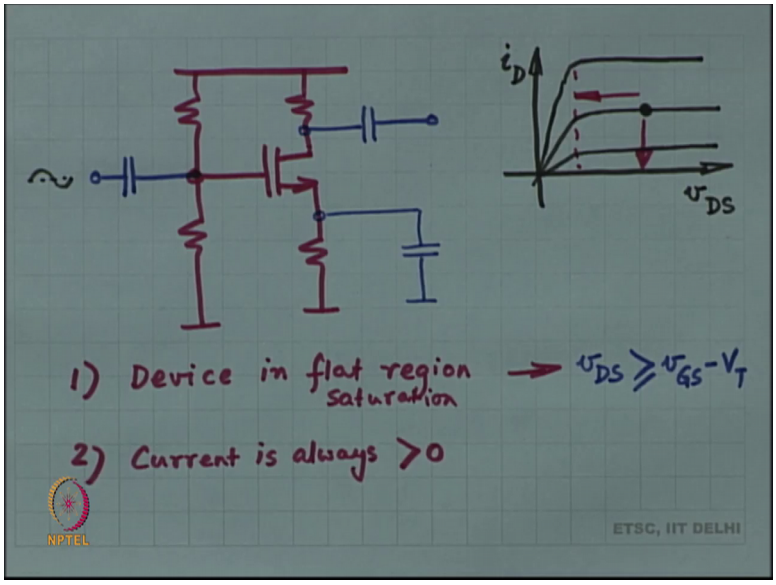

So, let us look at the circuits one by one. So, first of all are biasing circuit is common. It does not matter what you are doing; common source; common drain, common gate. We use the same core structure to establish the dc operating point and we had long discussion on why this structure looks like this right. So, this side you establish the operating the voltage at the gate and this resistor is important because otherwise the current is too sensitive to this voltage right to, this to this operating point; to this precise voltage, the current becomes overly sensitive. To reduce the sensitivity, we placed this resistor and now you know you have got a much more stable dc operating point.

Then on top of this, we had all the capacitors right. This is your input capacitor. This is your output capacitor. So, I am drawing the common source amplifier and this is the capacitor which clamps the voltage at the source to a fixed value ok. This is our set up.

Now the question is I am going to be changing the voltage over here that is going to change the voltage over here; that is going to change the current right the dc current is going to still flow through the resistor, the small signal current or rather the incremental current is going to come through the capacitor right. All of this is going to hold true no matter what.

Now, this MOSFET has to be kept in its flat region of operation, otherwise what? Otherwise the understanding the basic understanding of the MOSFET the g m for example, of the MOSFET no longer is what it should have been ok. The MOSFET is no longer going to reside at the nice operating point that you had set. So, remember you had

set the MOSFET at an operating point right, but you need to remain in the flat region of operation, otherwise the slope of this line is going to become low and therefore, the gain is going to not become enough and so on and so forth.

So, the largest change in the drain voltage, in the drain to source voltage that you can have the largest change is so much right. Beyond this you are not allowed to change the drain voltage ok. So, that is one point one extreme. The other extreme cases remember, when you are changing v GS i D itself is changing right. So, you are picking different curves from this family of curves and so on right. You should not pick an i D that has dropped all the way down to 0 or lesser it cant i D cannot go below 0 all right. So, you have to make sure that number one, your device is in its flat region of operation and number 2, the current through the device is more than 0 under all circumstances. So, these are the two extreme conditions.

So, remember these are these are two and only two extreme conditions. Everything is going to be depending on these two. Flat region is called saturation. So, what is the condition for saturation? V DS has to be more than v GS minus VT. This is the condition for saturation mathematically and number two what else do you need to make sure? You need to make sure that current is always more than 0 and this has to happen throughout the cycle right.

These are the two extreme limits right; one on the top. If I increase the current too much, then what is going to happen? If I increase the current through the MOSFET, then this voltage is going to drop this voltage is going to increase maybe if this resistor is there. If this resistor is not there, then it is fine; this voltage is clamped. But the drain voltage is dropping right.

You have to make sure that v DS even though the drain voltage has dropped v DS should be sufficient that it is more than v GS minus VT ok. This is when the current is too much. And then the current is too little right, the lowest current that you can have is 0, you cannot have a current less than 0 all right. So, these are generally the two conditions which you have to maintain right.

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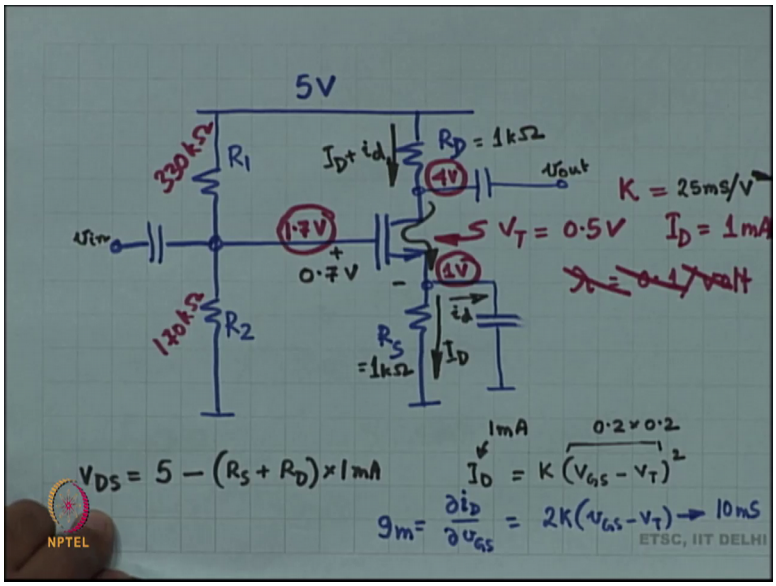

Now for example, let us take an example. Let us say that ok. So, this is your circuit all right. Now, suppose the power supply is 5 volts and then you are given that this MOSFET has VT of 0.5 volt and this MOSFET requires I C sorry I D equal to 1 milliampere this is the dc operating point, current is 1 milliampere and these are the requirements fine and then you have to make sure that you getlet us increase some conditions. So, let us say that what is lambda? Do you know what lambda is? Did we discussed lambda? No ok, we will we will discuss just now ok.

So, lambda will give us, you see the MOSFET has two basic parameters one is g m and the other is G DS or R DS right; g m effectively if you know I D if you know I D and if you know V T and if you know something a little more about the MOSFET like K times v GS minus VT the whole square that is I D. So, if you probably if you know K, then all of this is sufficient to tell you to give you information about g m ok, but what is which is the piece of information that gives you R D S or G D S. It is going to be lambda ok. Lambda will tell you a little bit about the value of R D S. So, with the help of lambda you can find out R D S ok.

Let us forget lambda, for now let us forget lambda. Let us say R D S is infinite of this particular MOSFET, forget it. So, I have this MOSFET I need a K. So, I need a K over here I cannot I mean I am trying to construct this problem for you from the top of my head I am trying to construct it. So, therefore, let me tell you what my thought process is.

So, K times v GS minus V T the whole squared is I D in the flat region. If I want to keep I D to be 1 milliampere and a very reasonable value of v GS minus VT is 0.2 volts and there is a square so, that is 0.2 into 0.2 that automatically means that my K should be 1 milliampere divided by 0.04.

So, K should be 25 millisiemens per volt squared millisiemens per volt, I am sorry fine. So, suppose this is the MOSFET for you now since we back calculated. I already know what is v GS minus V T v GS minus V T is going to be 0.2 volts which means that I need 0.7 volts over here ok. And I know I D is 1 milliampere. So, this 1 milliampere current is going this way as well as coming through this right. So, this is1 milliampere times R S. This is 1 milliamperes times R D and therefore, v DS is 5 volts minus 1 milliampere times R S plus R D in this case fine. Do you understand what we are doing? 5 volts right R D times1 milliampere R S times1 milliampere, the remaining part is v DS. So, v DS is 5 minus R S plus R D times1 milliampere. Any question so far?

So, next what we are going to do is we are going to say that the input is going to oscillate. When the input oscillates the output is going to so, if I have a sine wave at the input, I will have an inverted sine wave at the output because the gain of this amplifier is minus minus g m times g m. So, this there is a g m current which is caused by v G S. So, if I incrementally change this voltage over here at the gate I incrementally change, at the source the voltage is constant. So, this v GS is incremental change across the MOSFET.

This creates an incremental change in the current right. How much? g m times v GS current is going to be produced right and let us say R D S is infinite. So, in that case all of this incremental current is going to come from R D which means that the voltage here is going to be minus g m times R D. If I incrementally change this voltage by V, then the voltage here is going to be incrementally it is going to be change by minus g m times R D times V is this ok. And what is g m by the way? I D is K times v GS minus V T the whole squared.

So, g m is how much 2 K times v GS minus V T which was 0.2 right; v GS minus V T was 0.2, 0.2 times 2 times K. So, 0.2 times 2 is 0.4 times K was 25 millisiemens per volt right, 0.4 times 25 is 10 millisiemens ok.

So, let us say you want a gain of 10 minus 10 in that case, what should be the value of R D if you wanted again of minus 10? g m times R D is the voltage gain g m is 10 millisiemens. So, therefore, R D should be1 kilo ohm fine ok.

What about R student? Let us pick R S also equal to1 kilo ohm. Let us just pick I I really do not care what R S s R S was just for stabilizing that value over there. So, let us put R S also equal to1 kilo ohm ok. Now what happens at dc? By the way what are R1 and R 2, this is1 kilo ohm1 milliampere. So, the drop across this is 1 volt. So, the absolute voltage over here the dc operating point voltage at the source is 1 volt. The dc operating voltage at the gate so, this v GS is 0.7. This is one so, this is 1.7 volt and what is the voltage at the drain? 1 milliampere current is coming from the top right this is 5 volt. So, automatically this means that this is going to be 4 volts ok.

Now, just check that v DS is more than v GS minus V T. v GS minus V T is 0.2 volts right is v DS more than 0.2. Yes v DS is 3 volts over here which is much more than 0.2. So, you are safely in the flat region of the MOSFET. In fact, your power supply could have been much lower ok. This also tells you how to choose values of R1 and R 2 right. For example, R1 and R 2 could have been 330 kilo ohms and 170 kilo ohms. R1 and R 2 could have been 3.3 mega ohms and 1.7 mega ohms for example, that will still give you 1 0.7 volts ok. You do not need too much current in this in this path unlike in B J T circuits which you might have studied elsewhere in case of the MOSFET. You do not need too much current in this path because the gate is not going to take any current what so ever ok. So, this is the plan.

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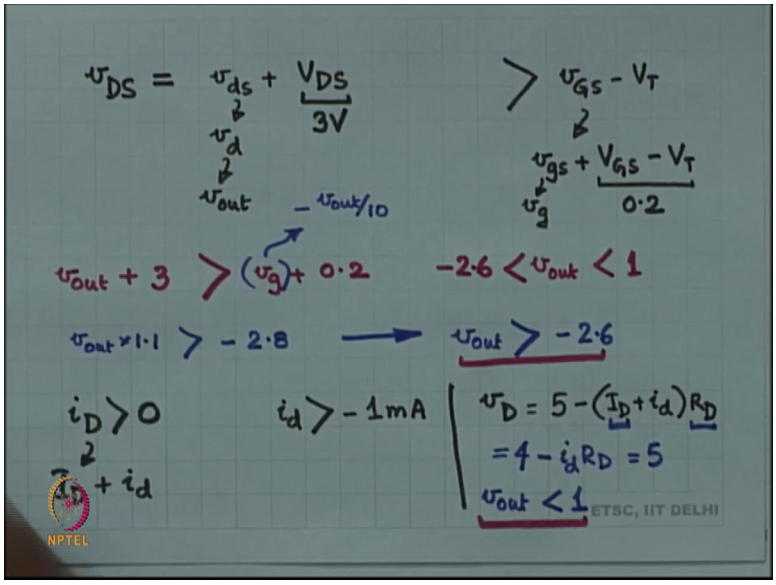

Now, what are the limits of the incremental voltage and the incremental current? So, number 1 v DS or rather the drain voltage is at 4 volts, source voltage is at1 volt. Now when I say V DS this is really small v ds plus capital V DS agreed and capital V DS I know is 4 volts minus 1 volt capital V DS is 3 volts ok. So, when I am changing incrementally when v DS is changing. By the way what is small v s? Small v s is 0 because this capacitor takes all the incremental current ok. This capacitor is a short circuit for incremental current. So, small v s v sub small s is equal to 0.

So, this is nothing, but small v s minus 0. They are the same in this case because there is a capacitor between source and ground all right and this is the same as the output fine. Now I need to make sure that this drain to source voltage is more than v GS minus V T ok. Now in this case the gate voltage is also going to be changing. When the gate voltage increases by 1 milli volt, the drain voltage decreases by 10 milli volts that is what it means by having a gain of minus 10 all right. So, be careful over there. If so once again small v gs minus V T small v gs comprises of small v g s plus capital V GS and this capital V GS is how much? 0.7 V T was 0.5. So, this portion is 0.2 we know this.

Once again source is not changing. So, therefore, this is nothing, but small v g ok. So, what do I have? I have the following v out plus 3 volts that is my small v ds has to be greater than small v g plus 0.2 ok. So, one shortcut is to say that small v g is very small and you forget it right in which case the v out has a limit right v out has to be greater than minus 2.8. If you say that small v g is very small right and that is a limit when you know the gain is that that can be said when the gain of the amplifier is very large. So, if

you were thinking of a gain of 100 or so, then you know v g can be very small. In our particular case the gain is only minus 10 in which case, if v out changes by 10 volt 10 millivolts plus 10 millivolts v g will be minus 1 millivolt. If v out is minus 2.8 volts then v g is plus 0.2 volts and so on and so forth.

So, you can call this approximately minus v out by 10 approximately in which case now you move the v outs together. So, v out into 1.1 is greater than minus 2.8 ok. So, it is not just v out is greater than minus 2.8 v out into1.1 is greater than minus 2.8 and this will give you v out has a limit. It has to be more than minus 2.8 by 1.1 whatever that is right. So, minus 2.8 by 1.1 would be approximately 2.6 minus 2.6 or so, something like that. Any questions so far?

So, just by observing that the drain to source voltage has to be always greater than gate to source voltage minus V T, I found a limit as to how much can possibly be the amplitude of v out; v out cannot dip by more than minus 2.6 volts because, then if it does so, then the MOSFET will move out of saturation. It will fall into the linear region of operation and that is not very good.

Our next critical condition is that the current has always got to be more than 0. So, this is the second critical condition. So, the first critical condition we have looked at. the second critical condition is that the current has always got to be more than 0. Now what does that mean; that means that this total I D has got to be more than 0; no matter what you do. But what is the I D? I D is capital I D plus small i d ok. So, if capital I D we know it is1 milliampere in this case, then small i d has a limit small i d has to be more than minus1 milliampere has to be more than minus1 milliampere. It cannot be less. If small i d is more than1 milliampere, then what. So, this is capital I D goes this way and small i d goes that way. So, it splits up right.

So, what happens here? This is at 4 volts already because of capital I D. Now access dip is because of small i d. So, the drain voltage is going to dip further because of small i d right effectively I have got 5 volts over here and this current is capital I D plus small i d that is the total current. So, the voltage at the drain is 5 minus capital I D plus small i d times R D right that is the voltage at the drain ok. And now this is 1 milliampere, this is 1 K. So, 1 milliampere and 1 K is 1 volt 5 minus1 volt is 4 volt minus small i d times R D and small i d has a limit that it has to be more than minus 1 milliampere. So, what does

that mean? the minimum value of small i d is minus 1 milliampere. So, the smallest value of small i d is minus 1 milliampere; that means, the largest value of v D is how much? 5 volts R D is 1 one kilo ohm right minus 1 R D right another minus. So, this whole thing is a plus 4 plus 1. So, v D the largest value of v D is 5 volts. Look at it again , the something trivial going on.

The smallest value of I D plus small i d is 0 that is this lowest possible value of the current right and when that is the current what is the drop across R D, 0. So, the largest voltage over here is nothing, but 5 volts is this ok. Right now it is trivial because there is no load, but as soon as a load comes this is not going to be the case anymore. So, you have to do it this way ok. So, this is the correct way of doing it. You cannot just say that its 5 volts all right.

Now, this happens to be 5. So, the largest value of the drain voltage is 5 volts which means that the maximum v out is how much? Is 1 volt because v out is what changes from the drain voltage, steady state right. Operating point of drain voltage is 5 volts 4 volts and then beyond that the drain voltage can go all the way up to 5; that means that the excess is limited to 1 volt. So, this tells you the 2 limits ok.

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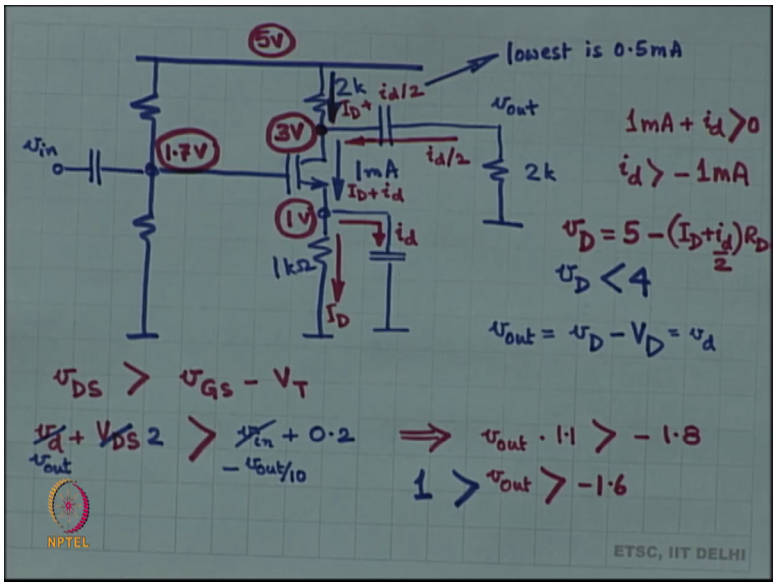

So far so good all right. Let us change the problem slightly, slight change. Let us put a load over here ok. So, first thing we are going to do is we are going to make this 2 K 2 K will target a bias current of 1 milliampere an operating point of 1 milliampere operating

current of 1 milliampere 1 K and this is 1 milliampere1 K. So, 1 volt over here 5 volt power supply and what is going to be the voltage over here? 1 milliampere 2 k; so the voltage over here is going to be 3 volt, and we are going to use the same parameters for the MOSFET.

So, the same K and the same v GS V T ,the same V T right and that will tell me that the v GS is 0.7 volt operating v GS is 0.7 volt which means that the dc operating point over here is still 1.7 volt and then R1 and R 2 you have selected accordingly ok. So, this is the situation ok.

Now, what is going to happen? Let us find out the limits. Limits are how high can v out go and how low v out can go. What is the lowest value of v out? What is the highest value of v out and usually you will get these limits with the help of 2 conditions. Condition number1 is that v DS has to be more than v GS minus V T at all times. Condition number 2 is I D has to be more than 0 at all times. So, these are the 2 conditions that you have fine ok.

So, condition number 1 v DS has to be more than v GS minus V T. By the way what is the gain of the amplifier? Look it is the same as before. It is still minus 10 because I have got 2 K in parallel with another 2 K at the output ok; g m is still equal to1 millisiemens sorry 10 millisiemens right and the output impedance is 2 K in parallel with 2 K. I am assuming output impedance of the MOSFET to be infinite, R D S is infinite. Let us say so, the gain is still minus 10 all right in which case, if I have a if I decrease the output voltage by 10 millivolt, I will have to increase the input voltage by1 millivolt; that is what it means.

Now, once again v DS has to be more than v GS minus V T at all times; v DS is comprised of drain voltage and source voltage source voltage is fixed at 1 volt. There is nothing where v DS is 2 volt in this case and this has to be more than v GS minus V T v D is the same as v out v GS is 1.7 plus the input and V T is 0.5; I am sorry gate voltage is 1 0.7, source voltage is1 volt. So, v GS is 0.7 volts V T is 0.5. So, v GS minus V T dc operating point is 0.2 and then the extra v GS on top of it is v in. And going by the gain that we have computed v in is nothing, but minus v out by 10 and this gives you you put all the v outs together. This has to be greater than minus1.8. So, v out is more than minus

1.8 by 1.1 whatever that is right 1.6 fine. So, this is condition number 1 that drain to source voltage has always got to be more than v GS minus V T.

Condition number 2 is that the current through the MOSFET has always got to be more than 0. So, the current through the MOSFET is 1 milliampere that is capital I D plus small i d that is the current through the MOSFET. This has to be more than 0 at all times which means small i d has a maximum sorry, small i d has a minimum right small i d always has to be more than minus 1 milliampere. This the requirement fine ok.

So, now, what is small i d? Small i d is the current through this capacitor. This is capital I D this is small i d and small i d creates a voltage drop over here, by how much? So, a portion of small i d comes this way. The portion of small i d comes that way. So, this is capital I D plus the small i d split is equal small i d by 2 right and this way the current is small i d by 2 because 2 K and 2 K right I am just trying to understand the situation. The net current is capital I D plus small i d which again splits up into the capacitor and the resistor at the source all right.

Now small i d by 2 is the current, the signal current coming from the drain resistor. Small i d by 2 is the signal current coming from the load fine. It is an equal split because these 2 resistors are equal happened to be equal.

What is going to be the change in the output what is the relationship between v out and small i d yes. So, the drain voltage is you know, the change in the drain voltage is v out. The the smallest value of small i d is minus 1 milliampere ok. So, therefore, therefore, the smallest value of the current of this of this particular current through this resistor is 1 milliampere plus minus 0.5 milliampere ok.

So, the lowest value of this particular current is half a milliampere. So, this particular current lowest is 0.5 milliampere. It cannot be lower than 0.5. Do you agree? Do you see what is going on over here? The entire dc current cannot be the signal current, only portion of it is is coming through this resistor. The other half of it is coming from the other resistor ok.

So, the lowest value of this total current I D plus small i d by 2, the lowest value is only half a milliampere ok. Capital I D is 1 milliampere. The smallest value of small i d by 2 the least value of small i d by 2 the least value of small i d is minus 1. The least value of

small i d by 2 is minus 0.5. So, the least of the total is 1 minus 0.5 which is 0.5 milliampere. It cannot be lower than that which means that the least drop across this resistor, the smallest possible drop is 0.5 times 2 K which is 1 volt; that means, that the largest voltage that the drain will ever go to is 4 volts. The largest voltage, it cannot go higher than that because the smallest drop across this 2 K resistor is 1 volt. So, you want it written down? Ok.

So, the smallest value of I D is minus 1 milliampere. Then the smallest value of the largest value of v D v D is what? v D is 5 volt minus capital I D plus small i d times R D sorry; small i d by 2 and here you are saying that small i d has a smallest value of 1 milliampere. It is always larger than that and therefore, v D has the largest value you plug in capital I D 1 small i d minus 1 right 1 minus1 by two. So, this is half capital R D is 2 kilo ohms half times 2 kilo ohm is 1 volt. So, the largest value of v D is 4 volts ok.

You started from 3 volts. The largest you can reach is 4 volts; that means, v out is 1 volt ok; v out is nothing, but small v D V D all right. Is this kind of understood what what is going on over here? So, all of your circuits all the circuits that we have studied before, you will have this kind of a pattern. The pattern is that the circuit is limited on 2 ends. One is what is the largest value of the output? The other is what is the smallest value of the output? Right you are looking at this in equation inequality. Largest value of the output is 1 volt. Smallest value of the output is minus 1.6. So, these are the limits of the output voltage.

These 2 are always going to be dictated by 2 conditions. One is what is the voltage v DS. This v DS has always got to be more than v GS minus V T; this is condition number 1 and condition number 2 is what is the current through the device. This current has always got to be more than 0 and based on these 2 conditions, you will get these 2 limits. Now when you have more than 1 transistor in the circuit, so far we have not seen more than one transistor.

Even when you have got more than one transistor, the same rules apply right; but then you have to take the conditions 2 conditions for each transistor. So, 2 , 2; 4 conditions some of those 2 conditions will not be relevant because they will overlap and you will be have you will have only 2 extreme limits and those 2 extreme limits will give you the

largest and smallest possible values at the output. So, these are the swing limits of the circuit.

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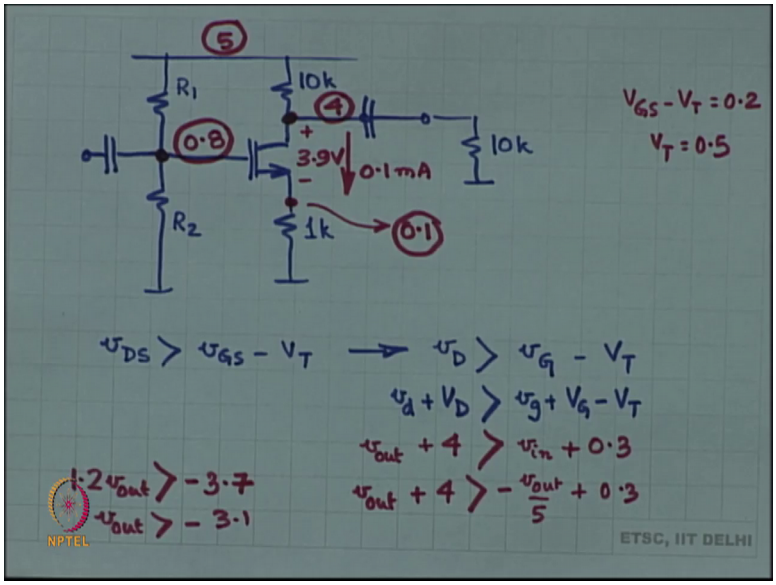

Quick thing; what happens if this capacitor was not there? If there there was source degeneration, shall we quickly think of one?

So, let us do a complicated one right. So, let us say this is 10 K, this is 10 K and this is 1 K and let us say that this voltage over here is 5 volts v D D is 5 volts and let us budget for the dc operating point. Let us budget you know what would be a nice number 3.9 volts would be nice of v DS at dc ok. So, dc operating point I am going to budget. This is just I am doing a budget ok; so 3.9 volts over here. So, 1.1 volt between these two resistors which means I can afford a current of 0.1 milliampere. So, this current is 0.1 milliampere at dc all right. So, this is where we start from.

Now, just by the way, what is the gain of this circuit? What is the voltage gain of the circuit? Do you know? This is the source degenerated amplifier. Yesterday in the last class, we had looked at the expression for this source degenerated amplifier. The expression was quite complicated, but when you say that g m is very large and g D S is very small, some strange things happened lot of things disappear and finally, you end up with the gain as minus R D by R S ok. So, how do you figure that out? You say that you say that the voltage at the source over here is going to be pretty much equal to the voltage at the gate.

So, if I apply v in at the gate, then the voltage at the source is also almost equal to v in. So, that current through the source resistor is v in by 1 K v in by the source resistance. This current has to come from the top. Now from the top means you lump these 2 resistors together right; obviously, it is going to split up between those 2 resistors. So, that signal current is v in by 1 K that signal current has to come from the top through the drain resistor right.

So, the voltage at the output is minus R D times v in by R S or in other words the voltage gain is minus R D by R S where R D in this case 10 K parallel 10 K 5 k. So, this particular circuit will have a gain of approximately 5. It is actually going to be less than 5 right; somewhat less than 5, but approximately equal to 5 ok.

Now, we need to find out the swing limits. Oh! I forgot to do the v GS. Let us say that I have organized V T and I have I have I make sure that the K of this device is such that you need v GS minus V T equal to 0.2 volt ok. Suppose and let us say V Tis 0.5 or so, so then what is the voltage over here? The voltage over here is 0.1. What is the voltage over here? 0.1 10 K is 1 volt 1 volt drop across 10 K. You start from 5 volts. So, you end up at 4 volts that is the 4 volts is the voltage at the drain 0.1 volt is the voltage at the source and if I have v GS minus V T as 0.2 and let say, V T is 0.5; then the voltage here is 0.8 and you have organized R1 and R 2 in that fashion ok. Am I being clear over here yeah? Ok.

So, this is the dc operating point analysis and once you are trough with the dc operating point, then we need to figure out what are the limits the maximum and minimum at the output ok. So, the input is going up and down around 0.8 right, accordingly the output is going to go down and up around 4. The drain voltage is going to go down and up around 4 volts. When the gate voltage is going up and down around 0.8 volts, but whatever happens you want the device to be in its flat region which means that v DS must be greater than v GS minus V T at all times ok.

So, earlier we had the source as a static voltage. Now the source is no longer static all right, but the cool thing over here is that the source voltage is going to cancel out; v DS is equal to v D minus v S v GS is v G minus v S. So, the source voltage really does not matter, cancels out ok. But v sub small D v sub capital D is nothing, but v d plus capital v D capital v D is 4. v sub capital G is fine so far so good. How much is v D? This is 4.

Small v d is nothing, but v out. This has to be more than small v g is nothing, but v in ok. Capital V G is 0.8 and V T is 0.5. So, capital V G minus V T is 0.3 not 0.2, it is 0.3 and then v in is 5 times smaller minus 5 times smaller than v out which means that if I increase v in by 1 millivolt, v out is going to decrease by 5 millivolts all right. Or in other words, this is minus v out by 5.

So, now, you put all the v outs together right, what do you get? You get v out and then 0.2 times v out. So, 1.2 times v out is more than minus 3.7 or in other words v out has to be more than something like minus 3 minus 3.1 all right. So, let us stop here. We will do the other condition in the next class. The other condition being the lower limit right what is the least value? This this is the least value of v out. What is the maximum value of v out that you can tolerate right; what is the least value of current right? The least value of current is going to be 0. So, we will do that limit in the next class ok.

Thank you very much.