**Introduction to Electronic Circuit**
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**Lecture 31**
**BJT Power Amplifiers**

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Yes 31st lecture on BJT power amplifiers, before we do power amplifiers we would like to work out at least one example on BCD biasing. While you design power amplifier you shall do further examples of BJT biases but one only BJT bias.

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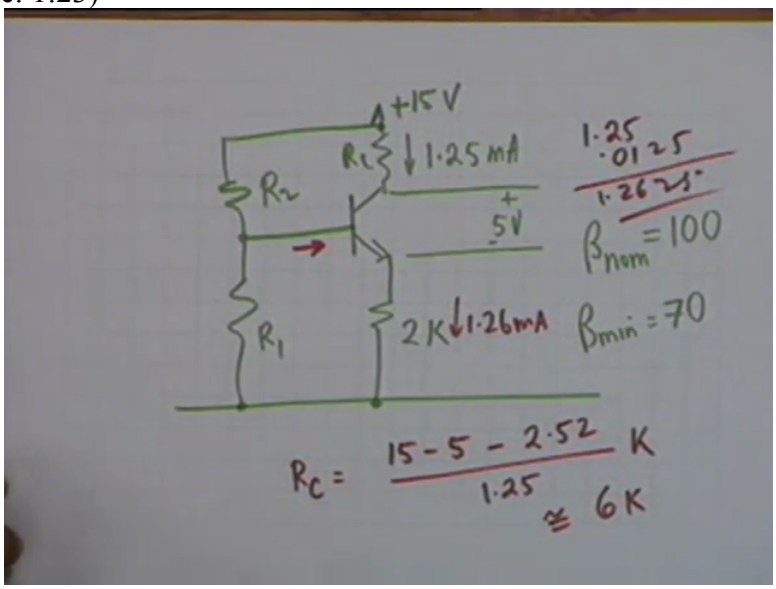


Let us take a BJT in which this is specified as 2K NRE is specified as 2K, so we do not have to we do not have to assume a VE and the collector current is specified as 1.25milli ampere R sub c is not known the VCC is specified as 15 volts and you now have to find out the other resistances namely R1 and R2. VCE is specified as 5 volt, VC is specified as 5 volts, beta nominal is specified as 100 and beta minimum is specified as 70.We have to design the bias(()) (2:26) that is the question.

So the Q point has been specified, the Q point is 5 volt 1.25 milliampere and you know where (()) (2:36) shall be, all you have to do is 1.25 milliampere divided by the nominal beta that means 100, alright. So you know what the Q point is, how do you establish this Q point? What value of Rc do you choose and what values of R1 and R2 that is the question? This is the total exercise.

Now obviously R sub c, you see this is 1.25 milliampere then what is this current? 1.25 plus . 0125, so approximately 1.26 milliampere and therefore R sub C shall be equal to 15 minus 5 then 15 minus 5 minus  2 times 1.26 to 2.52 divided by 1.25, so they need Kilo.

“Professor -Student conversation starts”

Student: So is it necessary?

Professor: Yes.

Student: (()) (3:46)

Professor: Oh! This current is 1.25 plus the base current and the base current is I sub C divided by 100 that is not added here 1.25 and .0125, is it clear? This is 1.2625 I took it among 526 and you can see that this is approximately 6K, alright.

“Professor-Student conversation ends”

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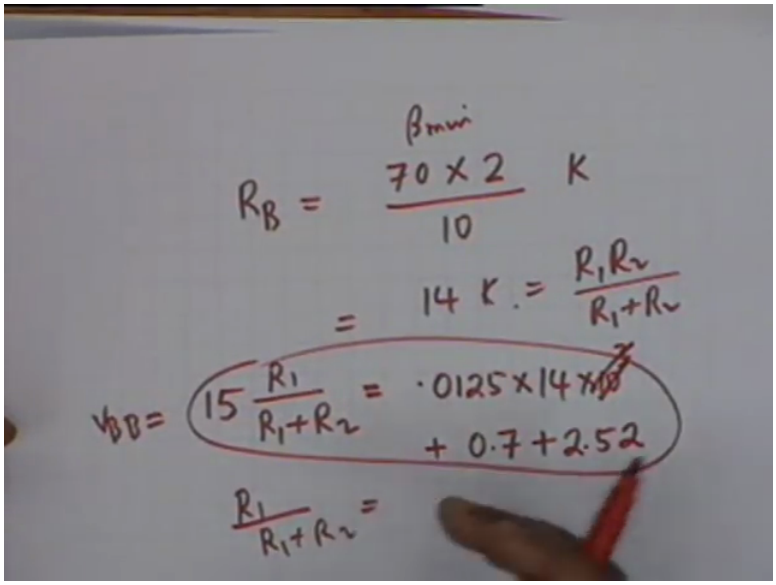


R sub C is known, what you do next? You choose an R sub B, R sub B, R sub B should be beta min which is 70. Beta min multiplied by RE if it is 2k divided by 7 which is equal to 14 K, no I made a mistake.

“Professor -Student conversation starts”

Student: Sir, it is correct.

Professor: It is correct, alright.

“Professor-Student conversation ends”

Then you have to find out VBB, VBB would be 15 R1 divided by R1plus R2 while this is R1, R2 divided by R1 plus R2, alright. R sub B then this should be equal to, this is VBB would be equal to IB RB which is 0.0125 multiplied by RB is already taken 14 times 10 to the 3.

“Professor -Student conversation starts”

Professor: No, I beg your pardon. Do not allow me to make mistake, will this 10 to the power 3 be there?

Student: No.

Professor: No because 0.0125 is in milliamperes, okay plus VBE you take that as 0.7 plus VE, what is VE?

Student: 2.5.

Professor: 2.52 volt or millivolt?

Student: Volt.

Professor: So you know what is R1 divided by R1 plus R2? Alright, from this equation you know what is R1 divided by R1 plus R2? And you know R1, R2 divide by R1 plus R2 as 14k, so all you have to do is divide 1 by the other then you get the value of R2 and if you know R2 then you know R1 and the values are, well, you find out the values. This is a typical design example. Designed for BJT biasing, we shall do further examples while you make actual amplifier designs either power amplifier or voltage amplifier.

“Professor-Student conversation ends”

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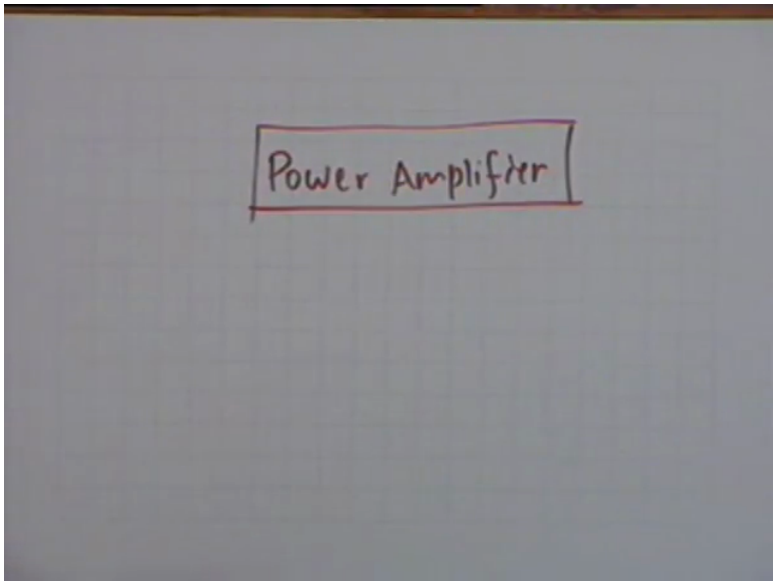


And this is a point where we plan to start our discussion on power amplifier. Well, one the difference between power amplifier and other amplifier is, that in a power amplifier your aim is to get as much power as possible into the load as much power as possible into the load and the ideal situation would be that whatever power is joined from the battery VCC multiplied by I sub C that is the power drawn from the battery.

Not quite, a little bit of power is also drawn the base, is not that right? VBB multiplied by I sub B, now the total power drawn from the battery is there for VCC IC plus VBB IB but you know IB is beta times less than I sub C, V is derived from VCC therefore VBB is less than VCC, am I making sense? Therefore, no, okay.

The total power drawn from the battery is VCC I sub C and VBB I sub B, we recall that the equivalent certainties in a VBB RB and the current that is drawn is I sub D, alright. This goes to the transistor the transistor is R sub C plus VCC they are baby VB and RE, this goes to ground and this current is I sub C, there are 2 sources of our one is VBB, what is VBB? It is derived from VCC.

VBB is VCC R1 divided by R1 plus R2, alright. So the total power that is drawn DC power that is drawn from the sources is VCC times I sub C plus VBB times I sub B nit you know I sub B is IC divided by beta approximately and VBB is less than VCC this is what I was saying and therefore this quantity is less than VCC IC over beta and we get beta of approximately 100, even ignore the second term.

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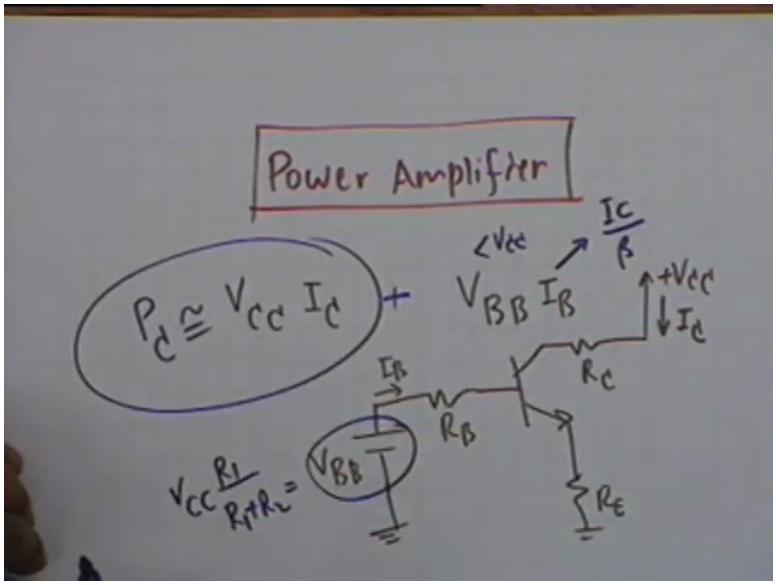


You can ignore the power that is dissipated in the base, power that is taken in the base circuit. So the total power taken from the battery is approximately call this P sub C approximately equal to VCC IC, is it clear? That the power taken the base circuit is much smaller than the power taken in the collector circuit therefore the power taken is VCC IC, now this power, yes.

“Professor -Student conversation starts”

Student: We have few equivalent…

Professor: Yes.

Student: So in (()) (9:53) equivalent the power is not the same. If we have that (()) (9:57) equivalent...

Professor: The current is the same I sub B.

Student: When we take the surveillance equivalent, the voltage and the current across the terminals is the same.

Professor: Correct, so the current in the load, current in the load is the same, where is this current going from? It is going from the source VBB.

Student: In the original circuit.

Pressure: Yes, we have not using the proposition, we had not using the proposition, we are using the same source but converted to the (()) (10:29), this shall be valid. If you calculate from the exact circuit it will be the same result this is a simpler way of doing things because let me tell you, that is a good question that he has asked.

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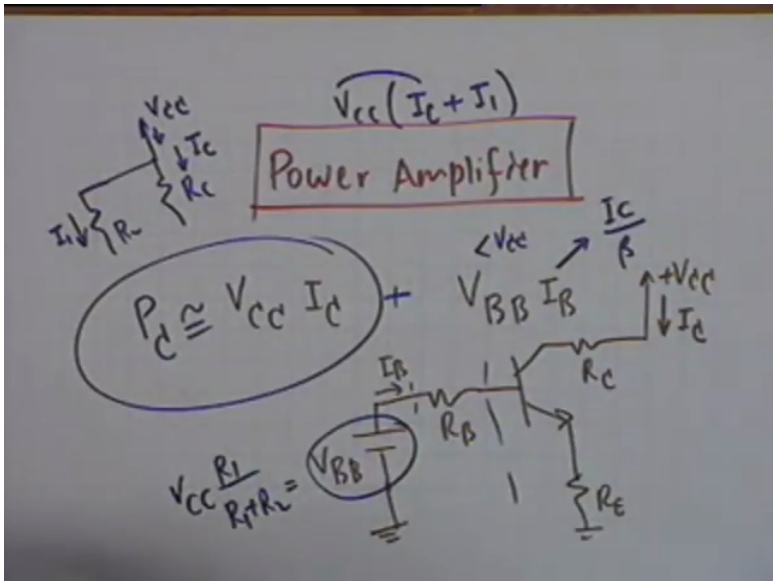


What we are doing is, some current is coming through this and some current is going through this, okay. So it is VCC multiplied by I sub C and the total power drawn from this source is VCC I sub C plus I1, is not that right? That is the only thing that is drawn from the source, there is only one source and it delivers current in 2 branches, this is R2 of course, alright. So the total power drawn from this source is VCC multiplied by current drawn from this source which is IC plus I1.

Now you can show that VCC I1 is the same as VBB IB, it is a simple matter of analysis, a few minutes and you will be able to solve this. So my calculation of power taken from the battery is approximately VCC IC because this I1 is very small compared to I sub C, alright. At least beta times smaller, therefore the total power drawn from the battery is VCC I sub C. Now what is our purpose the power amplifier is that this power if possible I would like the total power to appear as single power.

If it is stereo amplifier and I am taking power from the battery I would like the total power to be converted to single power which is of course not possible, why not possible? because you require a voltage, DC voltage to establish the Q point between the collector and the parameter

VCE is a necessary evil if it is an evil and if there exists a VCE through which the current I sub C passes, VCE times I sub C must be the power dissipated in the transistor.

Okay, so what I was saying is the power that is taken from the battery you would like, like so many wishes that you make you would like this power total power we converted to single power into the load but that does not happen, why it does not happen? Because of necessity there must be a voltage drop between the collector and the emitter to establish the Q point and therefore the transistor must dissipate PVCE multiplied by I sub C, call this PD power dissipated in the transistor.

Then you want that at least the rest of it that is from VCC IC, VC IC is the power necessarily to be dropped to be dissipated in the transistor, you want the rest of the power to be converted to single power, alright. So this is the purpose of the power amplifier, to transfer as much of the DC power as possible to single power and in the process one makes compromises in the process one makes compromises.

Compromising is that you would allow a little bit of distortion, you will allow a little bit of distortion because the larger the swing of this VCC is, the larger the swing of VC the larger would be the power transfer to the load and to be able to get large power you require large voltage swings and large current swings and whenever there are large voltage swings and large current swings you will enter into the non-linear region of the characteristics and therefore in tolerate a certain amount of distortion.

On the other hand if it is a voltage amplifier all that you want to do is to have a large voltage gain and you will see later that voltage gain simply depends on the resistances it does not depend on, it does not allow the currents and voltages to a very large swings, it does not, it is not required for large voltage gain. Similarly for large current again large swings of current or large swings of voltage are not required.

What is current again? Output current developed by input current. On the other hand power gain of transistor is not output power divided by input signal power, do you understand this? The power of the efficient (()) (15:06) transistor is an input power from signal would be very small, sometimes you can fit a voltage without power and input even open for example, open does not take any power, right?

But you require power at the output, so the power amplifier shall be characterized by single power output divided by the tower that is taken from the battery and when you multiply the 100 this will give you the power efficiency of the amplifier. So the main point that I was impressing upon you is that in a power amplifier the purpose of the objective is to transfer as much battery power into AC power or single power as possible.

On the other hand if this is not the requirement in a voltage amplifier or a current amplifier. And therefore our design of a power amplifier shall be governed by the different rules or very different considerations as compared to voltage amplifier and current amplifier.

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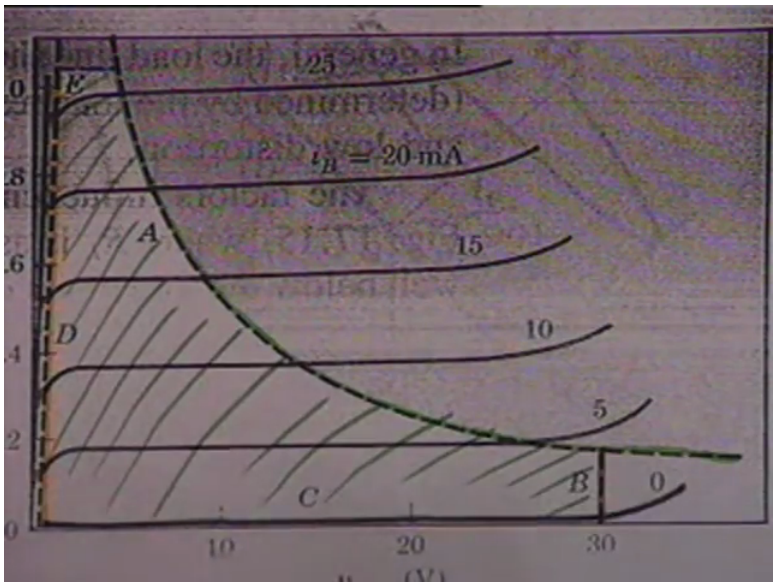


And one of the basic figures that one should understand is this that in the design of power amplifier is this figure quite visible, yes, okay. I will go very slow on this, if the design of a power amplifier the considerations are quite different from the design of voltage amplifier or current amplifier. And since most of you are familiar with power amplifiers we will talk about, we do power amplifiers first.

Before I do in what way? Interning your stereo into the full volume and that is power, okay. the considerations of the following, one is that the power dissipation every every transistor the manufacturer says you cannot dissipate more than 5 watts, alright. So from a single transistor you cannot discipline more than 5 watts and therefore the maximum power dissipation is fixed.

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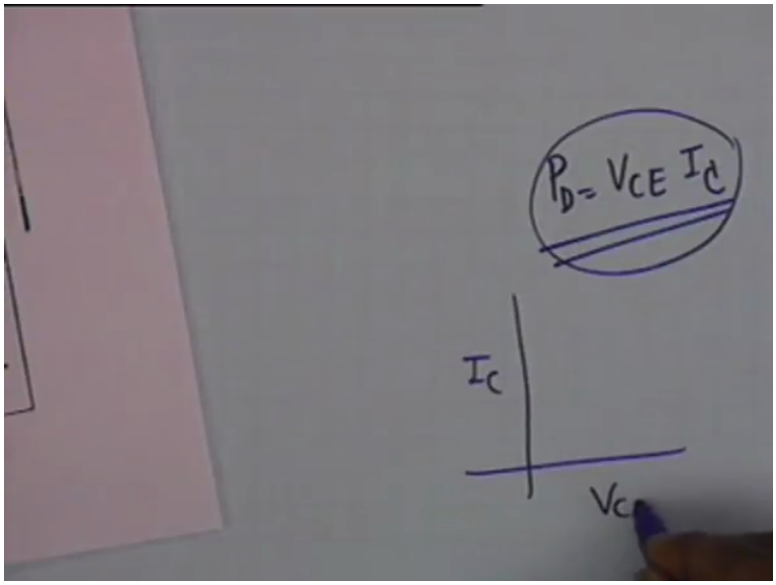


Which means that what is fixed is PD equal to VCE multiplied by I sub C, alright. This is fixed you cannot exceed this, if you exceed this then you will wonder transistor, alright. Now obviously in the VCE in the I sub C versus VCE characteristic, what does this represent? The product is a constant, so this represents a hyperbola, is not that right? The product xy is constant this represent a hyperbola.

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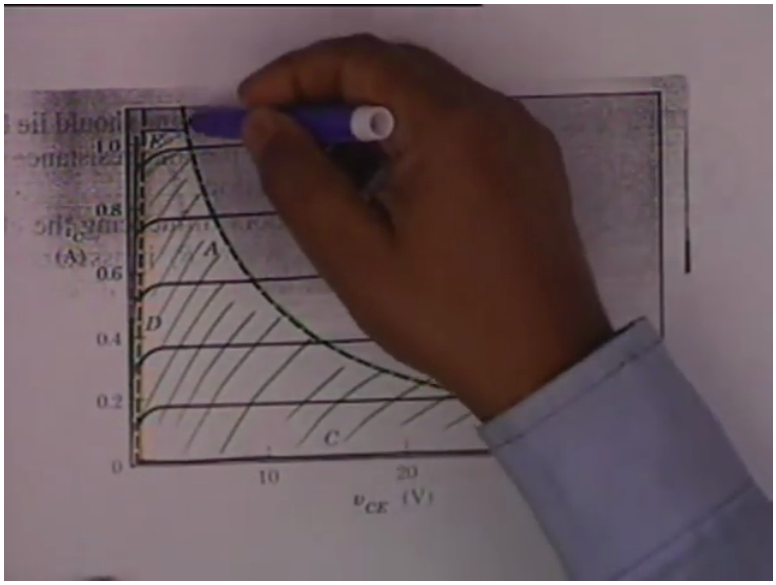


And this green line that I show here is this hyperbola the curve A this represents VCE multiplied by I sub C equal to a constant, how to draw it? You take any VCE, let us say 20 volts and find out the corresponding IC which is PD divided by 20 go to that point and this is a point on the hyperbola and similarly you draw several points then you draw this line, alright?

I have shown this as green hatchet area, this is the cool area and that has vie the colour green, the. Beyond it I should I should have painted it red burning hot area, you cannot go beyond this, alright. So this is the ultimate constraint, this is the fence beyond which you cannot go. Now there are other fences in this consideration, in one of them is the maximum voltage between the collector and the emitter you know that if the collector, parameter, collector base junction is reverse biased and therefore if you go on increasing VCB which also increases VCE, am I making sense?

What is VCB? VCB is VCE minus VBE and therefore if you increase VCE, VCB also increases and you know that at certain point avalanche multiplication or zener affect shall takeover this is why there is a slight tendency of these curves to go up, if you go beyond this while it will go like this and therefore there is maximum VCE it is possible and in this particular case the manufacturers specify the 30 volt is the maximum and therefore there is a red fence here.

You cannot go beyond this, alright. So the maximum VCE sets the line B, a vertical line must not exceed VCE 30 volts, alright. So this part is fixed in you cannot go to a negative base

current the  minimum base current is 0, you cannot go to a negative base current, why not? Because then the transistor does not conduct, alright. Base current can only be positive this is an NPN transistor.

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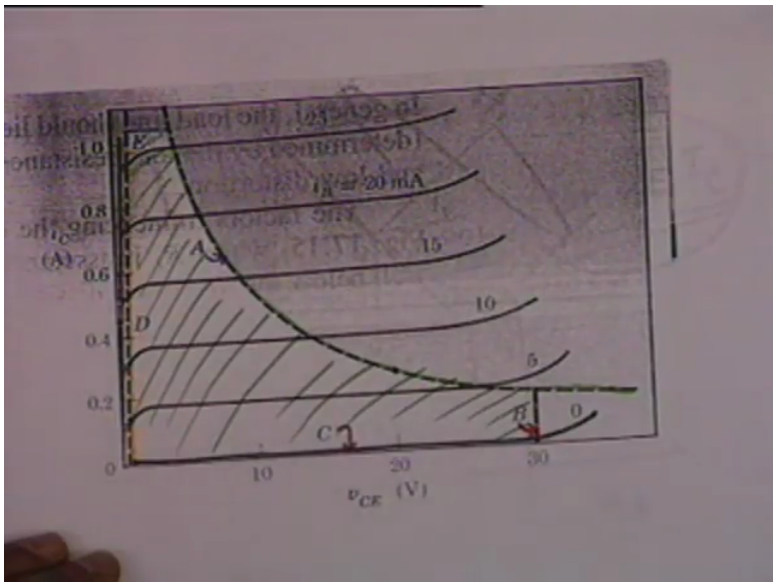


Base current can only be positive and therefore the curve for IB equal to 0 this is the curve C, alright. This determines another fence, you cannot make your base to conduct less than this current and what is this current, how much is this current? Beta plus 1 ICBO you cannot conduct less than this current market. So this is one of the...

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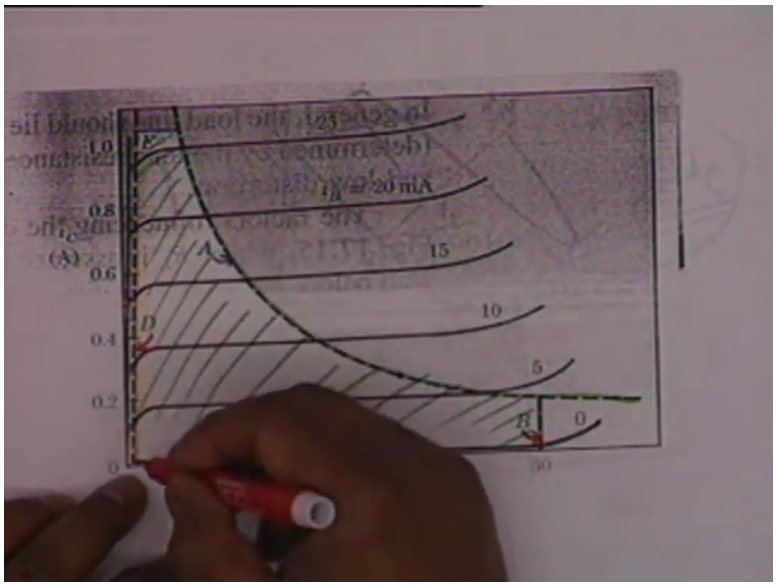

And the fourth line, the line D is this line, this is a saturation line you cannot make a VC less than this because then it is a highly nonlinear region, alright. You cannot go beyond this and another reason is that if VC is so small than the collector base junction refuses to remain in the reverse biased condition it becomes forward biased and this is why this is called a saturation region, alright.

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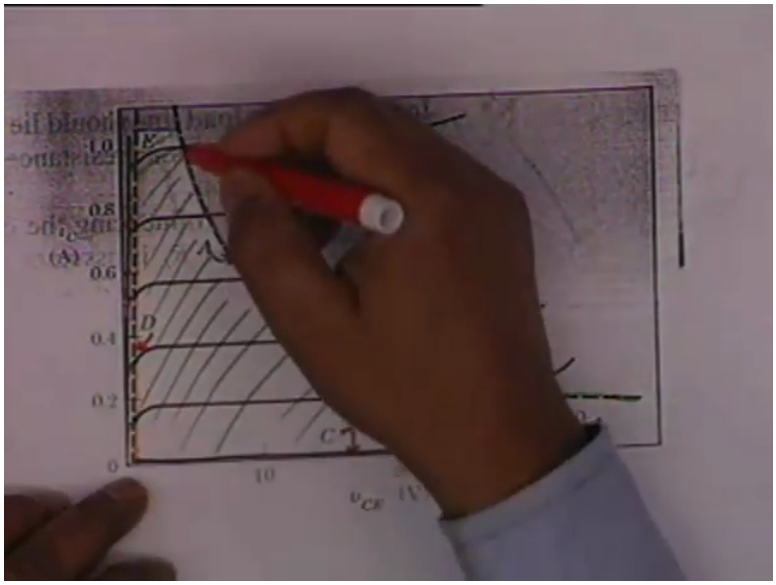


The fifth line, the fifth fence is determined by maximum I sub C maximum collector current, alright. Maximum Collector current, obviously you cannot exceed a certain maximum but usually the maximum collector current you must understand this it is not set by dissipation, it is not set by you see you cannot increase voltage beyond 30 because avalanche multiplication takes place.

You can increase the current beyond this, however but the manufacturers very clever people they say we will specify your transistor that you are going to buy from us only within a certain maximum collector current and this sets the maximum, this sets the line E is indicated here and therefore you have a completely bounded region within which you must operate the transistor.

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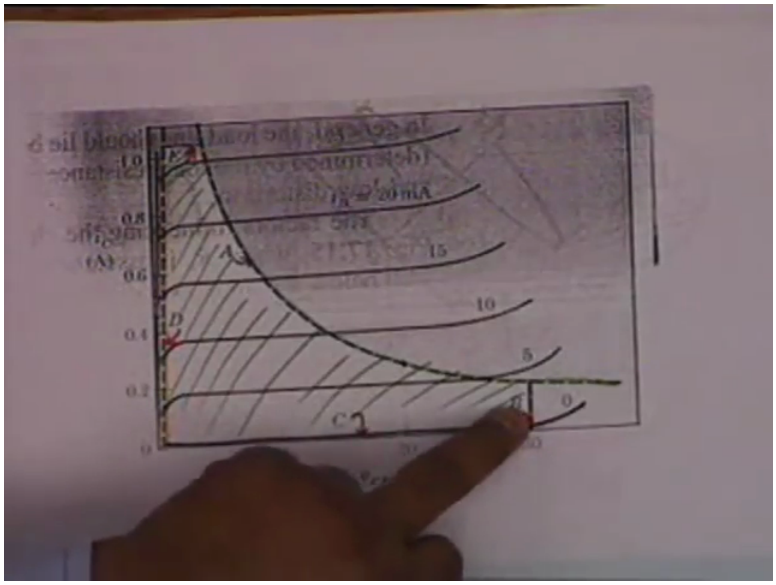


The question now is, is this point clear that it is a completely bounded region? Okay, it is bounded by 1, 2, 3, 4 straight lines and hyperbola, the hyperbola is the so-called power dissipation hyperbola that is VCE times I sub C is a constant, the question now is within this region where a suit your Q point B, where should be operating point B?

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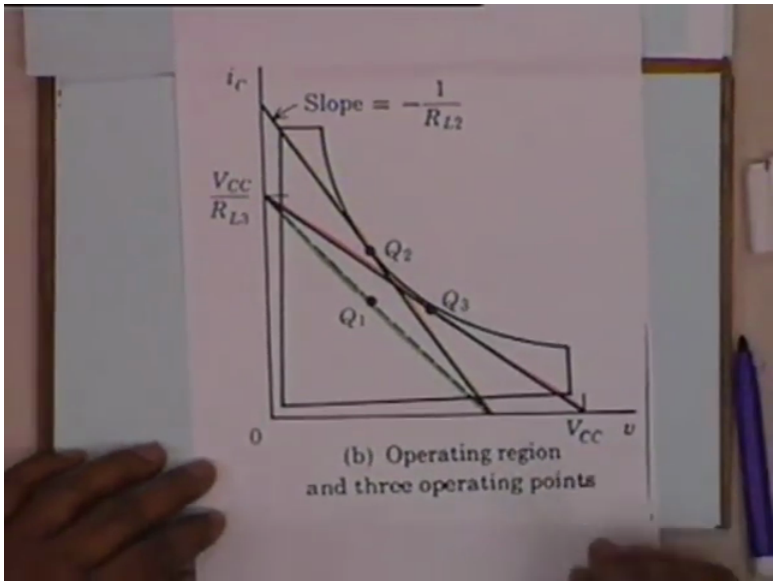


And for that I should project another diagram. Is this, okay? You see the our boundary is this, this one, who sets this IB equal to 0, who sets this maximum? VCE, who sets this hyperbola? Power dissipation, who set this vertical? Maximum current and who sets this? Saturation region. You notice that this is slightly tilted, why?

“Professor -Student conversation starts”

Student: Sir it changes.

Professor: Because it changes, the collector current changes with VCE slightly, this is also slightly tilted that is because the saturation region is also slightly tilted.

“Professor-Student conversation ends”

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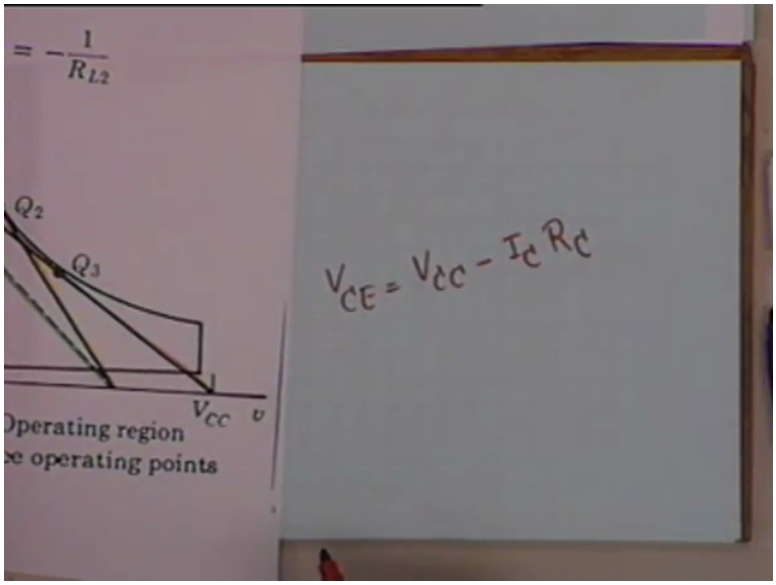


Now the point is where should I choose the Q point? 3 possible Q points are shown here Q1, Q2, Q3 and the corresponding load lines, what is a load line? Load line is a straight line satisfying the relation VCE equal to VCC minus I sub C times R sub C, if there is no resistance in the emitter lead, if there is resistance in the emitter lead then it should be I sub C RC minus I sub C plus I sub B times RE, is it clear?

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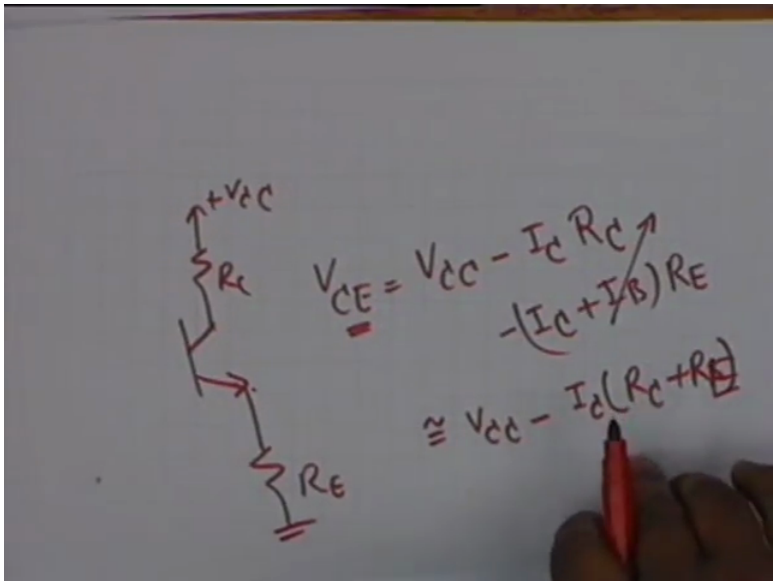


No, this is VCC you have RC the transistor then you have RE, so this he is equal to ICRC plus VCE plus IC plus IB times RE. Usually IB is very not small compared to I sub C it a times less and therefore this is approximately VCC minus I sub C RC plus RB, alright. And therefore the load line shall be a straight line which is slope of minus...

“Professor -Student conversation starts”

Student: RE.

Professor: RFC plus RE, thank you so much, yes.

“Professor-Student conversation ends”

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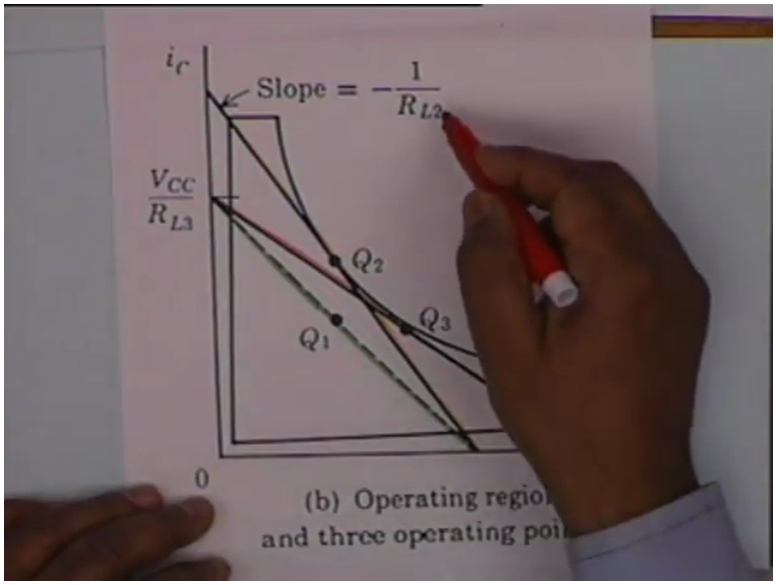


RC plus RE, therefore the load line is a straight line on the VCE IC characteristic with a slope of minus 1 by RC plus RE this is what we have called layer Rl2 or whatever it is, Rl, this is the DC load on the transistor, the total load is RC plus RE. Actually and exactly it is not RC plus RE but it is RC plus RE plus RE divided by beta, is not that clear? Because it is IC plus IB, okay.

Now, so this line for example has a slope, this line the green line, the green line you see is well within this boundary it is a safe operation, you can put your Q point here and then you can swing current and voltage right from this point at this point but that does not take account of to beats of a power amplifier. In a power amplifier you require maximum possible swing in voltage as well as current, alright.

And you want the transistor to be driven to its limit, what does that mean? You see the larger the swing the larger will be the power dissipation in the transistor but if power dissipation cannot exceed PD and therefore any Q point on this hyperbola will make sure that the transistor is being driven to its limit, alright. So Q1 is not a good Q point as far as power amplifier is concerned.

Power amplifier, for a power amplifier the Q point should preferably B on the power dissipation hyperbola that means either Q2 or Q3 should be a proper choice. Let us look at Q2; Q2 makes the voltage swing from here to here, alright. Q2 makes the voltage swing from here to here. So the voltage swing is restricted but the current swing it goes it from here to the maximum possible current that it can go, alright.

Is the point clear qualitatively? Q2 restricts the voltage swing but makes the current swing as large as possible. On the other hand if you look at Q3, if Q3 does not make use of the maximum possible current swing but it makes use of the maximum possible voltage swing, alright and therefore one is to make a compromise. Obviously you see that it is not possible to choose that point which makes use of largest current swing as well as voltage swing but it can be shown analytically at any Q point which in Q2 and Q3.

Any Q point between Q2 and Q3 approximately makes PD a constant, does it happily proved? Any Q point on this hyper Bola shall make PD a constant, alright? Any point on this hyperbola has PD equal to constant but any Q point on this produces approximately the same output signal power, this is what used to be analytically proved, we shall not prove it we will request you to accept this without question, alright.

But a Q point between Q2 and Q3, what is Q2? Q2 allows maximum possible current swing restricts the voltage swing. Q3 allows maximum possible voltage swing; this is VCC but restricts the current swing to VCC by Rl, alright. Now any point between Q2 and Q3 is almost the same power the output the question now is which point is better between Q2 and Q3.

To get an answer to that we require the characteristics signal. Is there any question on this figure? That between Q1, Q2 and Q3 first thing is Q2 and Q3 should be better choices. The next question that we have to decide is should we allow a larger voltage swing? Or should we allow a larger current swing?

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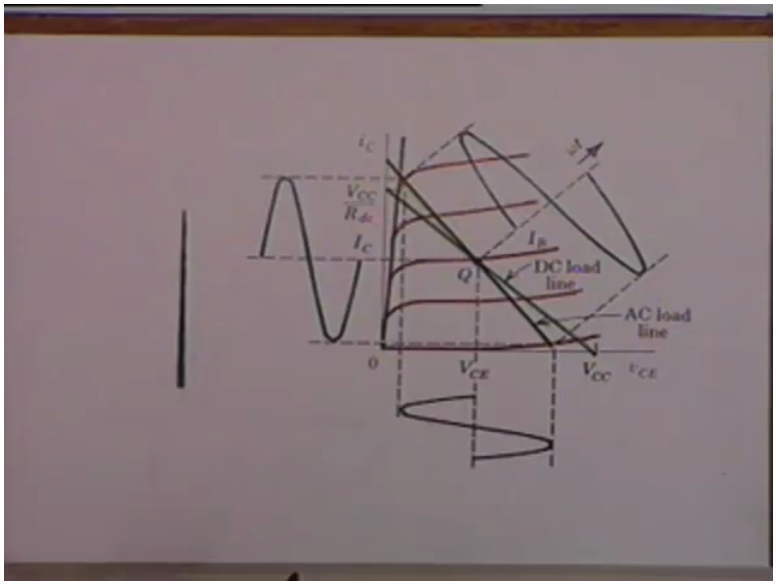


And to get an answer to this question, please look at these characteristics. If we allow a large current swing, if we allow a large current swing then we are coming near the saturation region where the curves are bent, alright. We are entering into the non-linear region. So are we when you come to maximum possible VCC, you see the curves, the curves are again bent but they are approximately parallel to each other even if they rise in an avalanche fashion there approximately parallel to each other. And therefore purely from qualitative inspection of the diagram one prefers to have larger voltage swing rather than a larger current swing, alright.

Let us look at an example, let us look at this example, okay.

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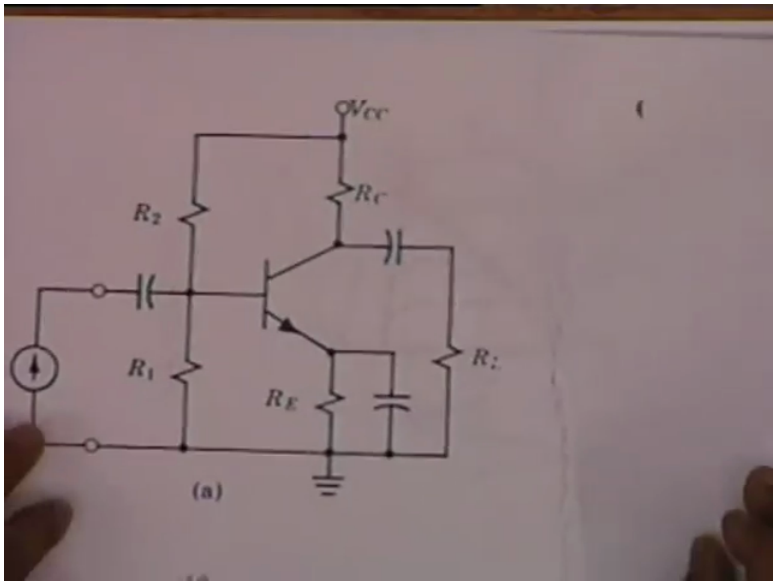


Before you come to this example let us look at this circuit once again. This is the same circuit that I have drawn, this is the usual circuit for BJT you have R sub C, you have an RE, you have R1 and R2 except that in this figure, what is new in this figure? There are 3 capacitors, well, what is the reason for these capacitors? This is the input current source, input source is shown as a current source it could be a voltage source also.

But you know because of source transformation all that you have to do is to include a resistance here, alright which can be combined with R1 if this capacitor was not there but let us first thing first let us look at these capacitors, why are the capacitors used? Okay, the first thing is this capacitor if it is not there then VCC, VCC this source shall see R2, R1, R1 will be parallel by the transistor and also by the source if this capacitor was not there.

And therefore unnecessarily some amount of power shall be wasted; we do not want the DC power to go into the AC source. For example it is good be a microphone or this could be from a transformer, this is a large DC, let us say hundred volts then it might saturate the core of the transformer and the whole signal capability is lost. It could be an LVDT linear variable transducer, okay. Whose core maybe saturated because of passing of DC.

So DC must be blocked from the signal source this could be a microphone as I said, alright. So there is a capacitor here, the purpose of this capacitor is to block DC and therefore this capacitor must act as open at DC but at the same time signal current should be able to pass to the transistor and therefore the capacitor must be large enough to allow signal currents to pass, what does that mean?

It means that its reactants 1 by omega C at the frequencies of Interest should be small compared to the impedance that it faces, what is the impedance that it faces? R2 parallel R1 parallel the impedance that is presented at the input of the transistor this is the purpose of this capacitor and it is aptly called a coupling capacitor, it couples the AC source to the amplifier, alright the transistor.

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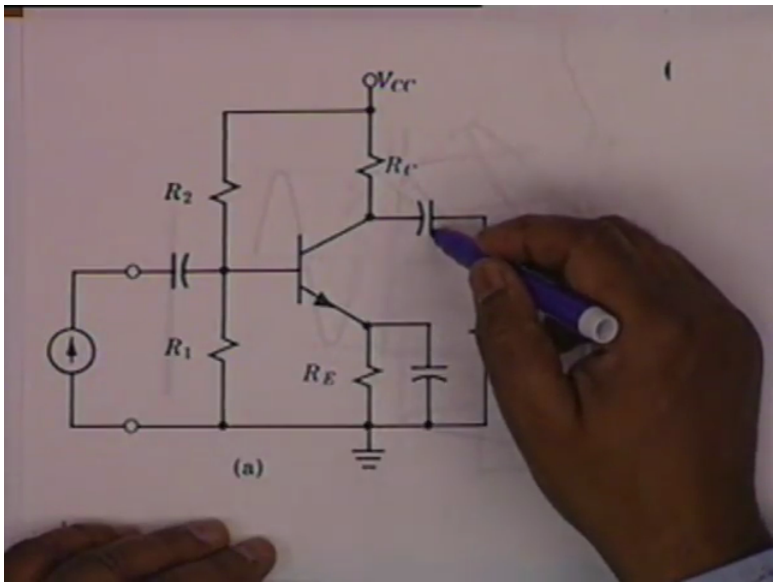


In a similar manner this capacitor, this capacitor is also called a coupling capacitor the reason is that this couples the amplifier the transistor to the load, the load could be a speaker, you know a speaker is an A term load, alright. A terms and your transistor BJT biasing may require 1K RC, alright. How do you get this? Therefore what you do is for biasing use an RC but followed you collect the load through a capacitor, alright.

This capacitor, if the capacitor was not there then the biasing would have been effected because VCC would not only pass the current through the transistor but also through Rl and therefore this is also called blocking capacitor it blocks DC. Third capacitor, the capacitor across RE. Well, obviously this capacitor also is to be AC shot signal shot and DC open, alright.

Now the third capacitor, okay. The third capacitor is inserted here for one reason, the reason is the following the signal power, the signal voltage should appear from the collector the base to ground; a signal voltage appears from the base to the ground. Part of the signal voltage is from base to emitter and part of it is across RE, is that clear? Oh! We do not want this.

We want the total signal voltage appears from the base to the emitter because it is the signal that is amplified. The signal voltage that appears across RE provides what is called a negative feedback at is it effectively reduces the input signal to the transistor, alright. And therefore we do not want that, what you want is that RE should be AC shot that means as far as signal is concerned this point should be of the same potential as this point.

On the other end we know RE, why could not we do it without RE? For biasing, for stabilising I sub C we do require an RE therefore we have to put an RE and we have to bypass RE for AC by a capacitor and therefore this capacitor is called a bypass capacitor, it provides a shot for AC. AC does not pass through RE it passes through this capacitor and since it is connected to the emitter terminal it is called an emitter bypass capacitor, is that okay?

"Professor -Student conversation starts"

Professor: The 3 capacitor is, do you understand this?

Student: Blocking (()) (38:12)

Professor: Pardon me.

Student: Blocking capacitor is this one and this one, okay they blocked these but this is called a bypass capacitor, alright?

"Professor-Student conversation ends"

Okay, now you should understand it also its complications now. It creates complications it is not simple as we have presented here because you see for DC, the effective load is RC plus RE, for DC VCE as you said is equal to VCC minus collector current multiplied by RC plus RE. On the other hand for AC RE is shorted, so RE does not present alone but RC what is the AC potential of this point?

A battery internal resistance 0, so the AC potential should be 0 and AC potential of this point is also 0 therefore RC and Rl connected in parallel because this is an AC shot therefore 2AC the effective load is not RC. The effective load is not RC plus RE, the effective load is RC parallel Rl. Obviously the AC load is smaller than the DC load and it is the AC load which

determines the amplification not the DC load, you understand this? And therefore there are 2 load lines now, one is the AC load line and other is the DC load line.

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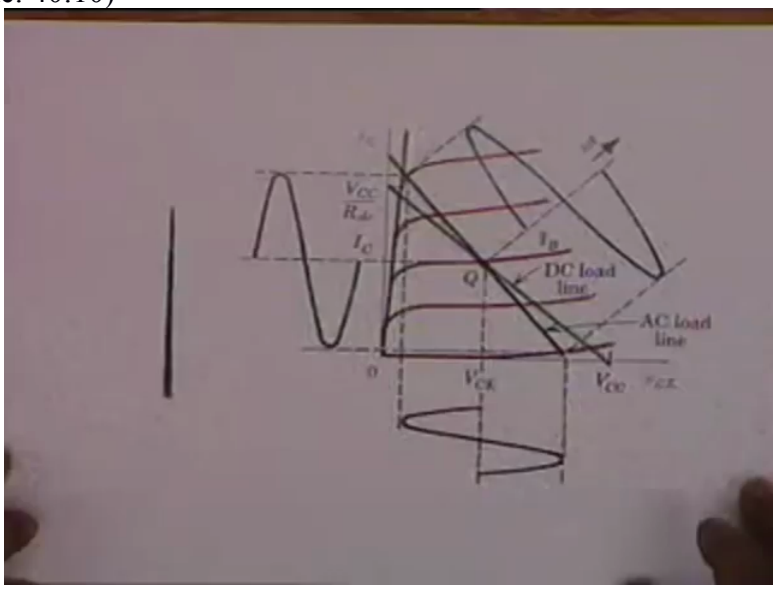

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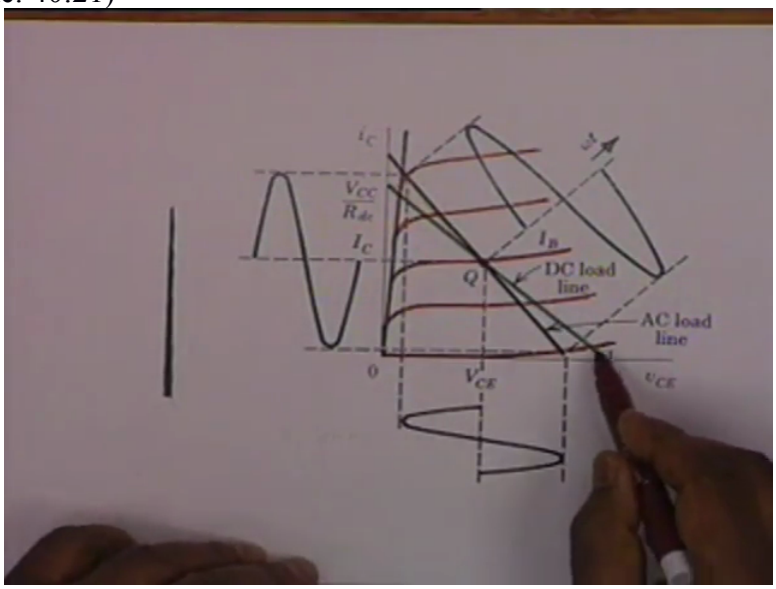


And let us look at this. Let us look at this now carefully look at this, these transistor characteristics and please be with me when I explain this. This green line which starts from VCC and goes to VCC by Rdc, what is Rdc in our case? Rc plus Re, this green line is the DC load line and normally if the DC load was equal to the DC load then you would like to choose your operating point or the Q point approximately at the middle point of this, is not it right?

So that there are equal voltage swings on both sides and equal current swings at both sides, okay. The AC load is not RC plus R E but it is RC parallel Rl and AC load is smaller than the DC load. The slope of this line is minus 1 over the load resistance and therefore the AC load line is tilted in the clockwise direction.

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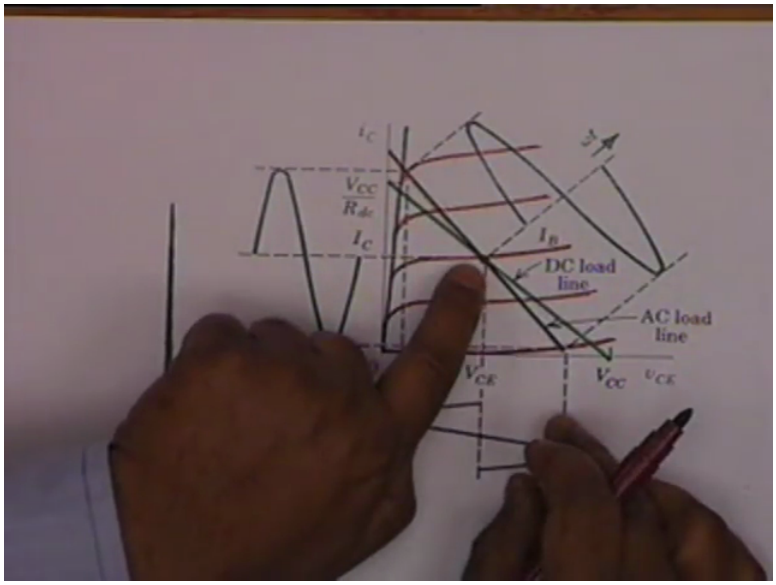


Therefore this orange line is the AC load line and we have shown that the AC load line also hinges at the same operating point Q point, why is it so? The AC load line must also satisfy…

“Professor -Student conversation starts”

Student: Sir therefore and input current is 0.

Professor: At this point the input signal current is 0, this is the DC croissant point, DC croissant point is also the AC, alright. Therefore once you settle on the DC Q point the AC led line hinges of this point and goes slightly above that is it goes slightly in the clockwise direction, alright.

“Professor-Student conversation ends”

Now when it does so then obviously for power amplifier operation you must restrict it between this points you see it does not go right up to the VC axis right, why not? Why not? Because you cannot go below I equal to 0 it must end here. Similarly it cannot exceed this point because then it will go into the non-linear region of the characteristics and therefore your operation is restricted between this point and this point.

This is the Q point and your operation is restricted between this point and this point, there are slight distortions because you are driving the transistor to its limit, whenever you drive anybody to once limit well, one cannot give the maximum but it gives as much power as is

needed you pay a price, the price is slight distortion, alright. It also shows what happens when the base current is allowed to fluctuate through the complete range, okay.

This is the base current, base current sinusoid the zero current is here, zero signal current, maximum signal current is here minimum signal current is here, alright. So the base goes through a complete fluctuation complete cycle. The collector current similarly goes through one complete cycle; the collector current as I had indicated on an earlier occasion is in phase with the base current.

On the base current is maximum the collector current is also maximum. The corresponding variations in the collector to emitter voltage is this and this is out of phase, is not it right? When the collector current increases VC decreases and therefore there is a phase change between the base voltage power base current with the collector to emitter voltage, alright. We will, alright.

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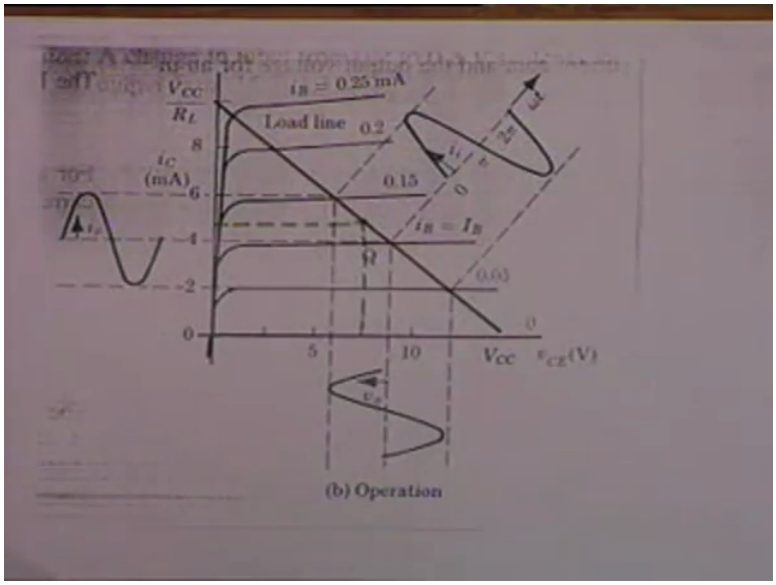


Let us see, is there any question? Then we will conclude with a simple example which can be answered by looking at the graph. The DC load line and the AC load line for this example are the same and it is this orange part, the Q point is here at 7.5volts DC and 5 milliampere, can you tell me what is the maximum possible voltage swing?

If this is 7.5 the DC load line and the A/C load line are the same, you know that there is no capacitor taking to a load it is RC while 7.5 volts is the Q point and therefore approximately swing is how much? 7.5 volts that means it can go 15 here and out approximately 0 on the other side. So 0 to 15, what about the current string? 0 to 10 approximately,it would not be quite then it would be about 9.5 or so up to this, alright.

“Professor -Student conversation starts”

Professor: So can you tell me what the load line is? What the load resistance is? No, just a second. What is a load resistance from this graph? This is approximately 10, this is approximately 10 and this is 15.

Student: Minus 1.

Student: Minus 1

Student: Yes.

Professor: Resistance is 125, no. How much?

Student: 10 to 300 then.

Professor: This is 10 milliampere and this is 15 volt, so 15 divided by 10.

Student: 1.5K.

Student: 1.5K.

Student: 1.5K.

Professor: 1.5K, alright. We know this slope but what is the peak value? Okay, what is the power dissipation? 5 times 7.5 which is 37.5 that is the maximum dissipation allowed in the transistor, is that okay? We cannot exceed there, alright.

And if I sub C if you collect that current is to swing from let us say 0 to 9.5 milliampere which is approximately here, what is the corresponding base current swing? You see these are things which have to be red from here. How much? This is obvious, it is given.

Student: 25 milliampere.

Professor: 02.25 milliampere base current swing, what is the corresponding collector current, collector voltage variation, collector swing? It is slightly asymmetric we can go right up to see the 0 base current is here, 0 base current is here that means ICB is approximately 0, Sweden go right up to 15 here, the (()) (48:31) right up to 0 here, no. Because the current is here this is about 1 volt, this is 2.5 this is about 1 volt.

So this symmetry is to be maintained but the swing will be asymmetrical 7.5 to 15 and 1 to 7.5 and therefore your collector voltage swing is restricted to...

Student: 6.5.

Professor: 6.5, that is right peak value because practical terms are since 1 obtains by looking at the graph, alright. Whereas in the design one has to look at these carefully because these are realities of life and cannot be ignored. With this happy note we conclude the class.

“Professor-Student conversation ends”