Introduction To Electronic Circuits Professor S.C. Dutta Roy Department of Electrical Engineering Indian Institute of Technology Delhi Module No 01 Lecture 30: BJT Biasing and Introduction to Power Amplifiers

This is the 30th lecture and the topic for today is BJT biasing and introduction to Power amplifiers.

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We had discussed last time a BJT biasing circuit in which the emitter was connected directly to ground, the collector was connected through R sub C to + VCC, a supply and a base current was supplied by means of a resistance connected directly to V sub CC and this resistance we had decided to call R sub B and we had seen that if due to any reason the current in the collector, I sub C, if due to any reason, I sub C increases, then the process is such that after several intermediate steps, I sub C further increases and this is a, this goes on in a circle till what you get is a thermal runaway.

That is as if the transistor cannot tolerate or accept any more heat and therefore it runs away from its responsibility which means that it gets damaged, it gets burnt out. Thermal runaway. And the remedies for this that we had suggested last time and had terminated the class at that point was that you introduce to this circuit, a couple of other resistances, namely you introduce a resistance from here to ground and another resistance at the emitter lead. This is the most common circuit that is used for biasing a transistor. This resistance which is connected to the emitter lead is called RE.

The resistance that is connected from the base to ground is R1 and this resistance is redesignated as R2 and this is the standard terminology. I sub C is the collector current, I sub B is the base current and total circuit is called aself bias circuit.



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Let me draw this again and explain how this helps in getting the bias stabilised. You have a emitter resistance RE, a collector resistance R sub C, this goes to + VCC.+ VCC because it is an npn transistor. If it is pnp, then it would be the negative supply. Then you have a resistance R1 here, no R2 and the resistance from here to ground is R1. This is the circuit and this current this correct is I sub C, this current is I sub B, this current obviously by KCL is I sub C + I sub B all right.

And total circuit is known as the self bias circuit. I would will not understand why and how the collector current stabilises, you assume that due to some reason, I sub C increases. If I sub C increases, then so does I sub C + I sub B and therefore the voltage drop across RE if I call this V sub E, V sub E increases. If V sub E increases, then naturally VBE shall decrease. VBE shall

decrease and if the diode voltage decreases, then you know the current shall also decrease and therefore I sub C increase means VE increase which meansVBE decrease and VBE decrease means I sub B decreases.

And I sub B decreases shall mean that the collector current which is beta times approximately beta times I sub B shall decrease and therefore the increasing tendency of I sub C shall be rested and therefore I sub C shall be stabilised. Qualitatively this is the explanation of the bias stabilisation due to the self bias circuit. Quantitatively, in order to calculate the values of the resistances and what values of resistances should be put to get a proper operating point, the Q point as we call it with stabilisation of the operating point irrespective of changes of temperature, irrespective of replacement of transistor.

This was the main cause, one of the main causes why the previous circuit could not be could not be used because that had kept IB constant and therefore if we replace the transistor, the beta of the transistor as you know can have a spread of about 1 is to 6 irrespective of whether the transistor is replaced, whether temperature increases or decreases Isub C should remain constant. Let us see analytically how this happens.

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In the process, you should remember, I will keep this circuit in the in the background.+ VCC RE, R1, R2, RC, this is IC and this is IB and this is IB + IC. As many times you draw it the better.

Now toanalyse this quantitatively, the transistormust be replaced by an equivalent circuit. And the transistor simply the base to emitter, simply means that you require, the base to emitter is a junction, is a diode and we assume that it is an ideal diode in series with a battery of VBE which is approximately 0.7 volts for silicon and 0.3 volts for germanium.

And therefore the transistor is equivalent to the following. It is equivalent to an ideal diode in series with VBE all right? This is the base and this is the emitter. Base, emitter, this is the collector and under this condition, you know that if the base current is IB, then I sub C the collector current is simply beta IB + beta + 1 I CBO. The collector current obviously is independent of VCE all right and therefore the collector, simply there are 2 current sources.

One of them is beta IBand the other is beta + 1 I CBO okay. This is the circuit, this is the equivalent circuit that we shall use for quantitative analysis. For quantitative analysis, we shall also use a simplification. You see, this branch consisting of R2 and R1 and VCC can be separated, that is you can include another VCC here. Itdoes not matter as far as analysis is concerned. So and this R2 disconnected to VCC, then connected base and R1 and if we look to the left of this line, we can replace this by a thevenin equivalent.

And a thevenin equivalent would be a battery VCC multiplied by the venin equivalent voltage source is the open circuit voltage multiplied by R1 divided by R1 + R2. Is that clear? Now.



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Let me draw it again. You have a VCC, then an R2 and an R1 and this is, this goes to the base. We are looking to the left of these 2 lines, from base to whatever the point is. Let us call it G. We are looking to the left of this line. So what we have is, we have a battery VCC, then we have an R1 and we have an R2. And it is these 2 points that we are looking into for thevenin equivalence and therefore this is simply equivalent to a thevenin voltage, let us call this VBB in series with a resistance which is parallel combination of R1 and R2, we call this resistance as capital R subscript capital B, this is R1 parallel R2. And VBB obviously is VCC multiplied by R1 divided by R1 + R2. Now this as you will see greatly simplifies the analysis.

If we substitute this in the original circuit, then my equivalent circuit becomes. Let me draw it on a separate sheet.



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The equivalent circuit becomes, I have a VBB, then I have R sub B, then the transistor, RE, then R sub C + VCC and this current is I sub C and this current is I sub B. Therefore, also this current is I sub C + I sub B. Now if I writeKVL equation around this loop, KVL equation, then I get VBB I sub B RB, the drop in RB + the drop from base to emitter + VBE + the drop across RE which is I sub C + I sub B RE, this is one equation in which the 2 currents, I sub C and I sub B are unknown but we know that I sub C and I sub B are connected by the relation, I sub C equal to beta I sub B + beta + 1 I sub CBO and thereforeI can eliminate I sub B from here.

Our purpose is to obtain I sub C and to see how stable the collector current is. So what I do is, I replace in this equation, the 1st equation, I replace I sub B by I sub B equal to I sub C - beta + 1 I CBO divided by beta all right. I replace this here and also here. Then I can simplify the algebra and obtain an expression for the collector current I sub C. The result after this algebra which I shall skip is as follows. Let me write down the complete expression.

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 $T_{1} \leq T_{2} \frac{1}{5276} \sqrt{BE} \frac{densur 2.5 \text{ mv}}{2.5 \text{ mv}}^{\circ} C$ $I_{CBN2} \frac{1}{1} \frac{1}{CBN2} \frac{\beta \propto T}{1} \frac{1}{CBN2} \frac{1}{1} \frac{\beta \propto T}{1} \frac{1}{CBN2} \frac{1}{1} \frac{1}{1} \frac{1}{CBN2} \frac{1}{1} \frac{1}{1} \frac{1}{CBN2} \frac{1}{1} \frac{1$

The expression is I sub C equals to VBB - VBE. And you can see that this comes from, VBB - VBE, that means I take it to the left-hand side and then I shall have a term containing I CBO. I CBO comes from here and also from here. The term is beta + 1 divided by beta I CBO, then RB + RE. Write down the expression because it is a very significant expression. Although a bit long but we shall investigate, we shall go very deep into this expression to be able to understand how and why I sub C is stabilised, why is it called a stabilised by a circuit. The denominator is RE + RB + RE divided by beta.

This is the expression for I sub C which contains its dependence on temperature through 3 things. What are these? In the denominator it is RE, oh it is there is no RC at all. This is correct. RE + RB + RE by beta. This is correct. Okay. Now I want you to notice I want you to qualitatively 1^{st} understandhow I sub C depends on 3 temperature dependent quantity. One is VBE. As you know VBE decreases at the rate of 2.5 millivolts per degree C. This is VBE

decreases at the rate of 2.5 millivolts per degree C and therefore VBE is a temperature dependent quantity.

Beta also increases with temperature almost linearly. Beta is proportional to temperature all right almost linearly and I sub CBO increases, it doubles, it exponentially, it doubles for every 10 degrees centigrade rise of temperature. I sub CBO doubles for every 10 degree C rise which remains that if I have let us say 2 temperatures, T1 and T2, look at this modelling, very simple modelling. If I have 2 temperatures, T1 and T2 where T2 is greater than T1, then I sub CBO2, that is at the increased temperature shall be I sub CBO1, that is the decreased temperature multiplied by 2 to the power T2 - T1 divided by 10. Is that okay?

This is a very interesting way of writing the expression. This is approximate but we can work with this. Is this clear? That if T2 - T1 is 10, then I sub CB 1 is multiplied by a factor of 2 which is in keeping with this relationship that is I sub CBO doubles for every 10 degrees centigrade rise in temperature all right. It also can be affected besides temperature even if you keep it within a temperature stabilised and closure, it can be affected by a replacement of transistor. A transistor goes bad in an amplifier, so you pull it out and put in another transistor of the same type but you know beta, beta has a large spread, it can vary by as large a ratio as 1 is to 6.

If the original transistor was a beta 30, the new one may have a beta of 180 but even then you do not want I sub C to change. You want I sub C to be stabilised. And therefore we must examine this expression as to how the stabilisation occurs. Before I take up the question of stabilisation, let me illustrate with an example as to how the things change withtemperature, utilising this expression. (Refer Slide Time: 19:18)

1CB0 $I_{c} = \frac{V_{BB} - V_{RE} + \frac{\beta+1}{\beta} I_{CB}(R_{\beta} + R_{\epsilon})}{R_{E} + \frac{R_{\beta} + R_{\epsilon}}{\beta}}$ Si $30 \le \beta \le 180$ $0.5 \text{ M} \le V_{BE} \le 0.9 \text{ mV}$ $1 \text{ nA} \le 100 \text{ nA}$

Suppose we have a transistor circuit, I will keep this expression in view. Is itvisible? Okay. Suppose have a transistor circuit in which the beta, well it is a silicon transistor and beta varies between 30 and 180. As I said, 1 is to 6 all right. A silicon transistor. VBE, the temperature is such that VBE varies between 0.5 millivolts and let us say 0.9 millivolts. It is a silicon transistor but with temperature, VBE can vary between 0.5 and 0.9. And I sub CBO can vary between let us say 1 nanoampere. Nano is 10 to the - 9 to let us say 10 nanoamperes, as much as 1 is to 10. That means the temperature may rise, no it will double for every 10 degrees centigrade.

And therefore this is a large range of temperature. It is 2 to the power, what is the temperature difference for which the ratio can be 10. 10 is 2 to the 3 is 8. So it is slightlyslightly less than 4, 2 to the 4. Yes, between 8 and 16. Okay. What we want to know is, what is the worst-case variation in I sub C all right. Obviouslythen you would want to know what the circuit is. Let us look at the circuit now.

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The circuit is the usual circuit, the self bias circuit and let us say the values are given as 10 K, 90 K, these are typical values, 90 K and then this is 2K, RE is 2K, RC is 15 K and VCC is + 28 volts. That is a typical circuit, typical biased or stabilisedcircuit . Toevaluate the worst-case currents obviously you require the values of R sub B. R sub B is the parallel combination of 90 and 10 K if you recall, it is a parallel combination of R1 and R2. So it is 9K and V sub BB, VBB is 28 multiplied by 10 divided by 100. So it is 2.8 volts. Is that okay?

Now let us consider the worst-case. We recall that I sub C is given by VBB - VBE + beta + 1 divided by beta I CBO RB + RE divided by RE + RB + RE divided by beta. The 2 worst cases are the following. One is that you put VBE, you want the minimum IC, you want the worst-cases, the minimum and the maximum. Obviously minimum shall occur when VBE is 0.9 all right because it subtracts. VBE is 0.9 millivolts, beta the smallest value which is 30. Now you might ask me why do you take the smallest value?

Because this is 1 beta + 1 divided by beta and there is a division by beta here. Now smallest is 30, 31 divided by 30 and 181 divided by 180, they do not differ much. 1 + 1 over beta and therefore beta basically controls this quantity. So you putbeta equal to 30 and I CBO put the lowest value. That will give you the lowest IC. Is that okay? Lowest value is 1 nanoamperes. You put down these values, then I sub C comes as 0.8 milliamperes. Now the other extreme, the other extreme is when VBE is 0.5 millivolts, let me indicate this in another colour.

The other extreme is 0.5 millivolt, beta is 180 and I CBOis 10 nanoamperes, beta is 180 and under these conditions, if we put down the values, then IC calculates as 1.1 milliampere. Can you see the range? 0.8 to 1.1, approximately 30 percent. Is that okay? 30 percent. But this is not a very good design. It can be reduced to much to a much less much lower value by an appropriate design. But even a roughly designed circuit causes a change of only 30 percent. All right?

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Now after this demonstration of the example, let us look at this expression again carefully and see what should be our design steps. Obviously obviously if you look at thedependent on beta, the numerator there is a term containing beta. In the denominator also, there is a term containing beta. And as I said, 1 + 1 over beta, when beta changes from 30 to 180, does not make much of a difference because 1 by 30 is 0.03 and 1 by 100 is 1.01 all right? So it does not make much of a difference.

The dependence on beta, there are 2 reasons why it does not make much of a difference, what beta is. That is because I CBO is also typically a very small quantity and therefore the total quantity here compares negligibly with VBB - VBE and therefore beta dependence is mostly through the denominator all right. And to make this insensitive to beta, what does that mean? It means that insensitive to transistor replacement all right? It is transistor replacement which causes the maximum change in beta.

So if I wish to make I sub C dependent on beta, what I should do is, I should make RE much greater than RB + RE divided by beta, which means that RE should be well beta - 1 RE. See if I multiplied beta RE and I bring RE from right to left, this should be much better than RB all right? This is the condition for independence to beta and you know beta is much greater than 1. Therefore this condition approximates to RB much less than beta times RE because beta is much greater than 1.



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Therefore one of the conditions in a stabilised biasing is that this design condition should always be fulfilled, RB must be much less than beta RE. And in electrical engineering, much less than or much greater than always is can safely be taken as 1 is to 10. And therefore if you know beta, you know RE, what you choose RB as? Minimum beta RE divided by 10. Which beta should you take? The nominal or the worst-case or the worstminimum case or worst maximum taste?

Student: Sir, minimum.

Professor: Minimum all right because you are taking much less than and therefore RB much less than beta min RE which means that the lowest value of RB that you can take is beta min RE is the lowest value or the highest value?

Student: Highest value.

Professor: Highest value.

The highest value of RB that you can take well let me put it here, I would be highest is equal to beta min RE divided by 10. This is a golden rule of thumb and must always be kept near the thumb all right. It must always be remembered. This is one of the basic design conditions of a BJT biasing circuit.

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BB-VBE + ICBO

Let us look at the expression again to find out other parameters. Now suppose s suppose I satisfy this condition all right, then my expression will simplify the following. It will simplify to VBB - VBE +, beta + 1 divided by beta we take as 1. So I sub CBO times RB + RE, is that okay? If we compare the previous expression, beta + 1 divided by beta, we take as 1 and therefore I CBO RB + RE and in the denominator, we shall have simply RE because that beta, term is negligible.

Now how do I reduce my dependence on I CBO? I CBO is inaudible is for every 10 degrees centigrade rise intemperature. So what I have to do is that this term, I CBO RB + RE must be made very small compared to VBB - VBE. Now who determines VBB? Obviously VCC and therefore the higher the value of VCC, the better will be the stability. There is also a choice in I CBO. You see, for silicon transistors, I CBO is much smaller as compared to germanium transistors.

For example, a typical silicon transistor as I said I CBO could be 10 nanoamperes whereas for germanium transistors, I CBO could be as large as 5 microamperes. So microamperes in relative terms is a small quantity but relative to 10 nanoamperes, obviously 5 microamperes is a large quantity. 5 times 10 to the - 6 and 10 times 10 to the - 9 and this is why silicon transistors are much more preferred than germanium transistors. This is one of the reasons that I CBO is much smaller okay.

Now normally in a silicon transistor, if you choose your VBB properly, then this will be satisfied all right? In any case, you must see that this inequality is satisfied. This is one of the inequalities. Finally, the devil is VBE which decreases at the rate of 2.5 millivolt per degree C. How do you reduce the dependence onVBE? Obviously what you should do is, VBE should be much less compared to VBB and how do you obtain this? VBB is VCC R1 by R1 + R2. You must choose your R1, R 2 and VCC such that this relation is satisfied okay. So these are the basic design parameters of a BJT.

As you can see as far as temperature is concerned, in this expression, we have eliminated beta all right. In this expression, the temperature dependent quantities are 2, one is VBE and the other is I CBO. And therefore, if temperature changes from capital T to capital T + Delta T all right, then with a corresponding change in I sub C, that is what would be Delta I sub C?

AIC = - AVBE + AICBO RB RE VDE = 0.7V , ICRO IONA Ge: 0.3V $\Delta T = 50^{\circ}C$

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Obviously, Delta I sub C shall be, VBB is independent of temperature, so - Delta VBE + Delta I CBO times RB. I am intentionally ignoring RE because usually RB is one order higher than RE, that is approximately 10 times RE and therefore I am ignoring that. This divided by RE. This is a simplified expression for calculating the temperature dependence of I sub C. For example, if you take a silicon transistor, then VBE is 0.7 volt and I CBO typically is 10 nanoamperes.

For a germanium transistor, the corresponding figures are 0.3 volts and let us say 5 microamperes and suppose there is a 50 degrees centigrade rise of temperature. Suppose delta T is 50 degrees C, then the question is, how much does I sub C change? Delta I sub C contains 2 quantities, one is Delta VBE and one is Delta I CBO. Due to 50 degrees centigrade rise in temperature, what will be the factor by which I CBO changes? 2 to the 5, that means 32 all right. And therefore, the new I CBO shall be 32 times 10 nanoamperes, 32 times 5 and Delta I CBO should be 31 multiplied by these 2 quantities. Is that clear? Is that clear, why 31? Okay.

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2.5 mV × 50 - D. 125 V ATc =

Soif I take silicon Delta I sub C shall be equal to let us take some specific values of RE, let us take for the same design, the design that we had just, let us take 2 kilo okay? 2k and what we, what did we take RB? 9Kall right. Then Delta I CBO for silicon would be 300, 32 times 10 - 10, so 310 multiplied by 10 to the - 9. Then +. Now you see what happens? Delta VBE, VBE actually decreases with rise of temperature. So what would be delta VBE? It would be, Delta VBE isnegative but because of - Delta VBE, it will be an addition.

And Delta VBE therefore shall be - 2.5 millivolts multiplied by 50 which is equal to -0.125 volts. Is that correct? 125 millivolt which is 0.125. This will be 0.125. I must multiply by 10 to the 3. And this figurecalculates out to 0.05 milliamperes approximately. Do you understand this calculation? Okay. On the other hand, one can now say if it is germanium and you proceed with the same calculation, Delta VBE is the same, is not it right? Delta VBE is the same. It is only Delta I CBO which now becomes how much?

31 times 5 microamperes which is 155 microamperes. If you put that, Delta I sub C calculates out to 0.75 milliamperes. And you see the range of variation. Whereas this is only 0.05, germanium, same rise of temperature can cause a large change in I sub C. And this is the reason why silicon is always preferred, particularly where the device has to work under extreme temperature conditions all right.

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We can now summarise the methods, the procedure for BJT biasing. What are the steps? The steps are that the 1st thing is to do is to choose a Q point. How to choose a Q point, we shall illustrate later but 1st choose a Q point. What does this mean? It means choosing an I sub C, the collector current. It means choosing a V sub CE all right? And if you know the nominal beta, then obviously you know I sub B also. You know I sub B if you know beta all right. These 2 quantities are enough to specify a Q point.

This is an additional information, that is on the characteristics, which characteristic does the Q point lie on? You know that the characteristics are regularly spaced, parallel lines depending on the value of beta, depending on the values of I sub B. I sub B is the parameter and therefore which I sub B line it lies on, this is an additional point. Nexthave to go to the emitter. You recall that the emitter has a resistance RE and the current through this is I sub C + I sub B all right?

If RE is given, then of course you know what the drop across this is. If RE is not given as is usually the case, you arbitrarily assume a value for VE, you assume a value for VE. Suppose your power supply that is given is let us say 12 volts, then obviously RE cannot drop how much? It cannot drop 12 volts because there would be a VCE, there will be a drop in RC and you do not want this drop to be large because you want a large swing in the output voltage.

Typically this is chosen about 20 to 25 percent, rule of thumb again. There is nothing sacred about it all right. 20 to 25 percent. And one of the things that textbooks or manufacturers specify is arbitrarily choose VE equal to 3 volts. Now suppose this transistoris to go into a space instrumentation, into a space vehicle where voltages are available are very small, maybe 1 volt is the total voltage available. Then obviously, this will not do. You will have to change the design appropriately. Maybe 0.3 volts but for normal operating conditions, a 12 volts supply or 15 volts supply, we assume VE approximately as 3 volts.

This must be done with care. If RE is given, youneed not do this. But if RE is not given, you assume this to be 20 to 25 percent of the given power supply and then you can calculate RE because you know IC+ IB all right? So the 2nd step would be to determine an RE or V sub E. If RE is given, then you determine VE. If RE is not given, then you assume a VE and determine RE all right.



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The next thing is select VCC, 3rd step VCC and R sub C, select VCC and R sub C. Now if VCC is given, if this is given, if the power supply is given, then what is R sub C? This will be VCC - I sub C well, I am sorry.R sub C would be VCC - VE - VCE all right because if you recall, the transistor is like this. This is VCC, VCC - VCE -VE divided byI sub C. So you can determine RC. On the other hand, if RC is known, it might be specified bythe load.

The load may be specified, then if RC is known then you calculate VCC. VCC would be sub C RC + VCE + VE right? This is the 3rd step. Either you find RC or you find VCC.

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The next step is choose an RB, that is R capital B which is the parallel combination of R1 and R2.Parallel combination of R1 and R2 which means R1R2 divided by R1 + R2. And I have already told you that this should be chosen as beta minimum times RE divided by 10 all right? Far less than or far greater than 1 is to 10. So you choose an RB all right? And once you have chosen an RB, this...

Student: Why divided by 10?

Professor: Why divided by 10? What I want is RB should be much less than beta RE. This is the rule of design all right? Much less than, therefore it must satisfy the expression even when beta is beta minimum. And much less than or much greater than in electrical engineering is1 is to 10 ratio, that is enough. This is why, I divided by 10. You can divide by 20. There is nothing sacred about it all right? This is aarbitrary figure but divided by 10 is taken to be specifying much less than or much greater than.

And the 5th step isafter you choose this, you know R1, R2, you also know that VBB is equal to VCC R1 divided by R1 + R2 and this would be equal to if you recall the thevenin equivalent

circuit at the base emitter junction, this is equal to I sub B RB. This was the circuit. VBB is equal to IB RB + VBE + VE all right. You know VE, you know VBE, you know IB, you know RB, you have chosen it all right and therefore you know 2 things. One is R1R2 divided by R1 + R2 and the other thing that you know is R1 divided by R1 + R2.



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From these 2 then you find out R1 and R2 and these complete the design. We shall now have a break for 5 minutes and then continue with the design.