Introduction To Electronic Circuits
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Module No 01
Lecture 29: Transistor Characteristics and Biasing

This is the 29th lecture and the topic for today is transistor characteristics and biasing. We have already seen the transistor characteristics under the common base connection.

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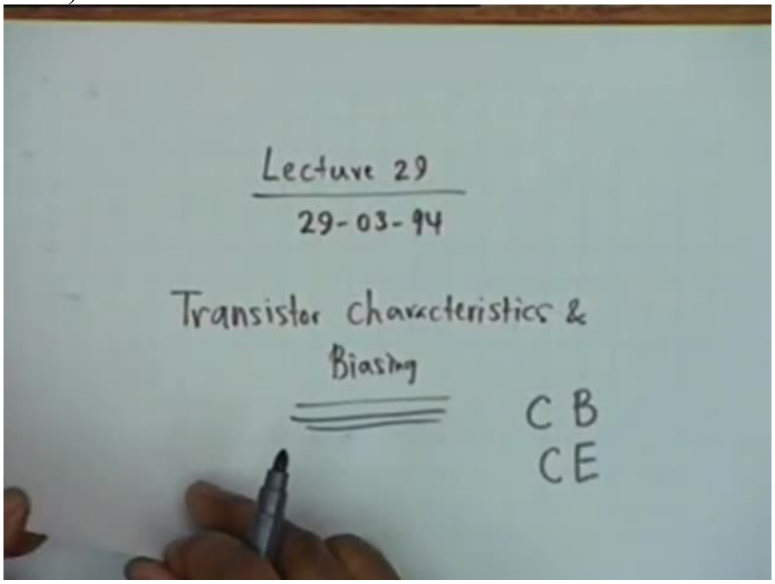

Lecture 29
29-03-94

Transistor characteristics &
Biasing

CB
CE

We had also briefly discussed the common emitter connection which we would like to expand on today.

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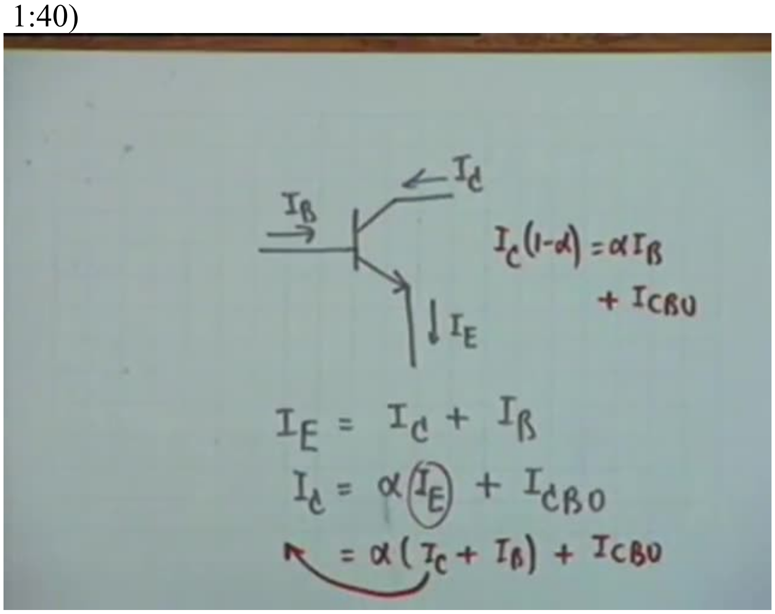

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_E = I_C + I_B$$

$$I_C = \alpha(\boxed{I_E}) + I_{CBO}$$

$$= \alpha(I_C + I_B) + I_{CBO}$$

In the common emitter connection, it is the emitter terminal which is common between the input and the output. Obviously we are considering an npn transistor npn transistor and the currents are I sub E, I sub C and I sub B. Settled down quickly and quietly. These are the actual directions of currents, the base, collector and the emitter all right? The base emitter junction is forward biased and the collector base junction is reverse biased. And therefore the basic relation, one of the basic relations is that emitter current is the sum of the collector current and the base current.

And we also know that the collector current is a small is a fraction of the emitter current alpha IE where alpha is less than 1 and in addition, because the collector junction is reverse biased, there is a reverse saturation current I CBO flowing in the circuit. Now if I combine these 2 relations, these relations hold good under any connection of the transistor. What we are interested in is in showing how I sub C, the output current varies as a function of the input current I sub B because this is a common emitter connection.

So what we do is we substitute for I sub E here from the 1st election and therefore I get alpha I sub C + I sub B + I CBO and then take this term to the left-hand side, this term, the term containing I sub C. And then I get I sub C 1 - Alpha and the left-hand side should be equal to alpha + I CBO all right? I am interested in finding I sub C as a function of I sub B.

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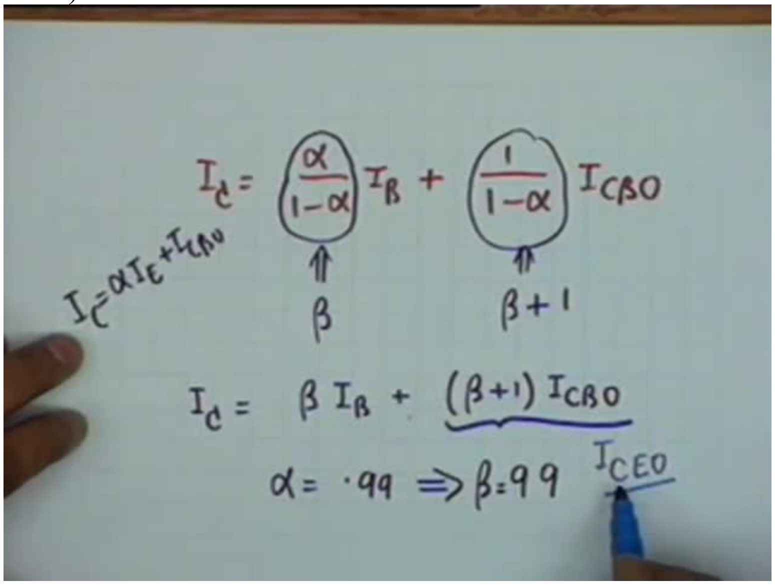

$$I_C = \underset{\Uparrow \atop \beta}{\boxed{\frac{\alpha}{1-\alpha}}} I_B + \underset{\Uparrow \atop \beta+1}{\boxed{\frac{1}{1-\alpha}}} I_{CBO}$$

$I_C = \alpha I_E + I_{CBO}$

$$I_C = \beta I_B + \underbrace{(\beta+1) I_{CBO}}_{I_{CEO}}$$

$$\alpha = .99 \Rightarrow \beta = 99$$

And if I divide both sides by 1 - Alpha, then the relationship that I get is I sub C equals to alpha by 1 - Alpha I sub B + 1 by 1 - Alpha I sub CBO, the reverse saturation current. Now Jack Jack we defined last time this quantity alpha by 1 - alpha as beta, then 1 by 1 - Alpha can be easily shown to be equal to beta + 1 and therefore I sub C is equal to beta I sub B + beta + 1 I sub CBO all right? If you ignore this term, if you ignore the I CBO term, that is the reverse saturation current term, then you see that the collector current is exactly proportional to the base current and the proportionality constant is beta.

This is why beta is called the current amplification factor under the common emitter connection. Beta can be much larger than unity. For example, if alpha is equal to 0.99 then beta is how much? 99. Beta is 99. Beta can be much larger than unity. The other thing is that in the reverse saturation condition, in the common base connection in the common base connection, the relationship was simply IC equal to alpha IE + I CBO. In the common base connection, the relation between input and output was simply IC equal to alpha IE + I CBO and I CBO formed a small fraction of the total current. Here you see, I CBO is multiplied by a large quantity, beta + 1.

And if beta is 99, then this is 100 times I CBO. And therefore, the reverse saturation current contributes to a much larger fraction of the total collector current under the common emitter connection. And this current is sometimes denoted by I CEO, that is it is the equivalent reverse saturation current under the common emitter connection all right? Under the common emitter connection.

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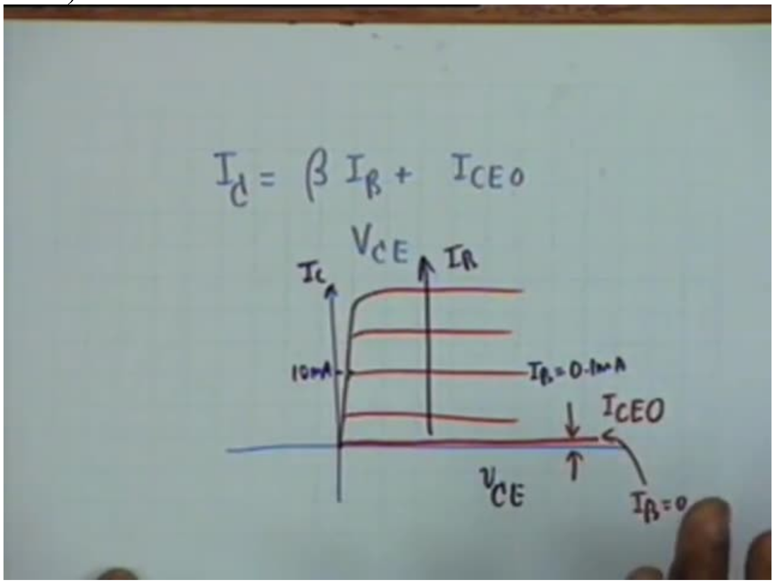

$I_C = \beta I_B + I_{CEO}$

And therefore my characteristics now become I sub C, the output current is beta I sub B + I sub CEO which is about which is beta 1 beta + 1 times I CBO. Now let us look at this relationship. You notice that the input current is 0, that is base is open. Base does not contribute anything. Then I sub C will consist of a small component, I CEO and this is independent of VCE, that is the collector to emitter voltage. It it does not contain amazing concerned with VCE and therefore it is independent of VCE. In other words, if I plot the characteristics and then beta equal to 0 will give rise to a characteristic like this where this current is I sub CEO, that is this corresponds to IB equal to 0.

Now when IB increases to a nonzero value, naturally the collector current increases by the amount beta IB. So equal increments of IB shall cause equal increments of I sub C. Is that clear? Equal in because I CEO is a constant all right? And therefore, as we go ahead, we shall have curves like this. Each of them representing a certain value of IB and IB is increasing in this direction. Suppose IB is equal to let us say 0.1 milliampere, for a particular curve, there is a certain value of IB all right?

And suppose this curve when extended on the left, meets this at let us say 10 milliampere, suppose. Can you say approximately what beta is? Approximately? If you ignore I CEO, then obviously the collector current, this is I sub C and this is V sub CE. It would be 10 milliampere divided by 0.1 milliampere. So it would be approximately 100. Now let us see some actual characteristics.

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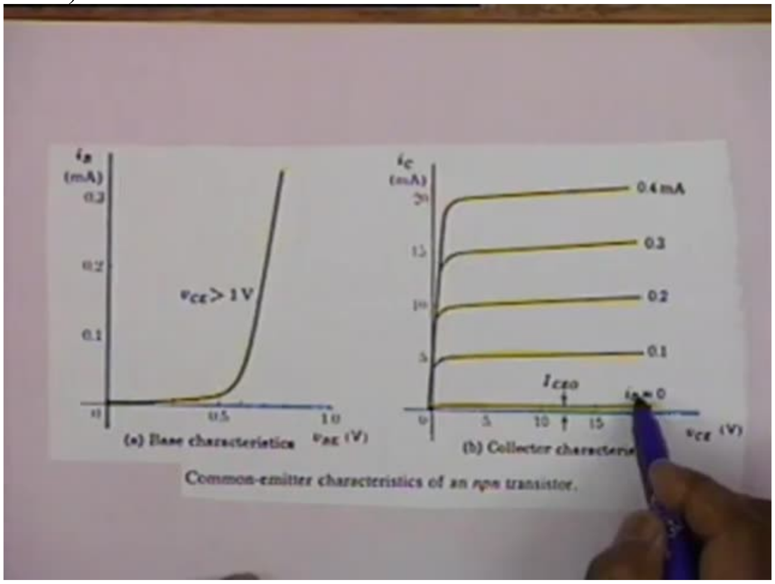

Do not try to read the read what is written here because I am going to spell it out. These are the common emitter characteristics of an npn transistor and this curve shows the input characteristics, that is IB as a function of VBE. As you know, in the common emitter connection, the base to emitter junction is forward biased. It is a diode and therefore no wonder, this characteristic is that of a diode characteristic, the base emitter junction and you can see that it is approximately a straight line which when extended to the x-axis, to the VBE axis, it will cut at ats a (vo) voltage of about 0.7. This is 0.5, 0.6, 0.7 and this is why we take the input junction, the base emitter junction as equivalent to an ideal diode in series with 0.7 volt if it is silicon all right?

Now the output characteristic, that is the collector current I sub C vs VCE as I said when IB is 0, no base current, all you have is I CEO all right? When IB increases to let us say 0.1 milliampere, well the curve goes like this and you see, it cuts, if you extend this it cuts at about 5 milliampere and therefore this is a transistor with a beta of 50, 5 by 0.1. Similarly when the when the base current goes to 0.2 milliampere, well it cuts the axis at about 10 which which corroborates the fact that beta is approximately equal to 50. An equal increments of base current should cause equal increments of collector current and this is approximately true in practice also. This is what the collector characteristics look like and this is the input characteristic.

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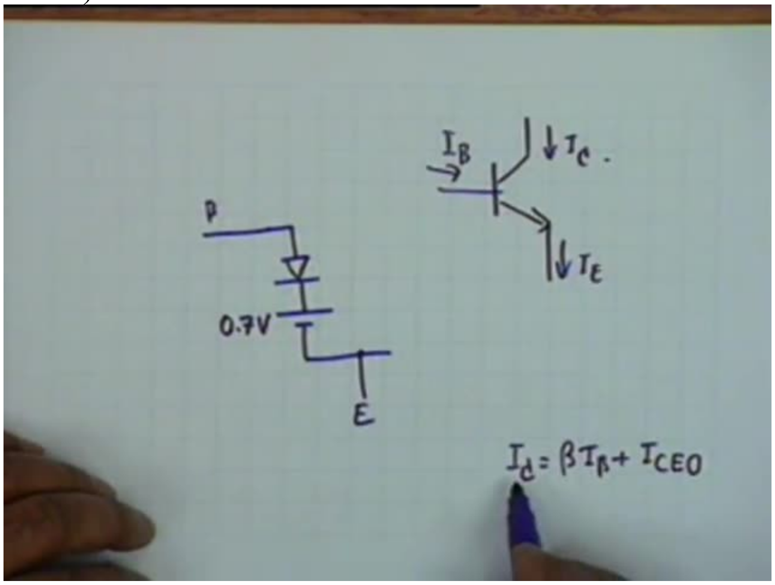

And as I said as I said, we approximate the DC operation of the common emitter transistor. DC operation in which there is a current IB, there is a current IE and there is a current I sub C. Well, the input junction, base emitter junction is a forward biased diode and if this is silicon, then we approximate this by means of an ideal diode in series with 0.7 volt DC voltage and this leads us to the emitter. If you are fussy, if you wish to incorporate the slope of this line, then you should add a small resistance.

You should add a small resistance here which for the present, we ignore and as far as the output is concerned, well the output is simply beta IB + I CEO which is beta + 1 IBO and this is independent of VCE.

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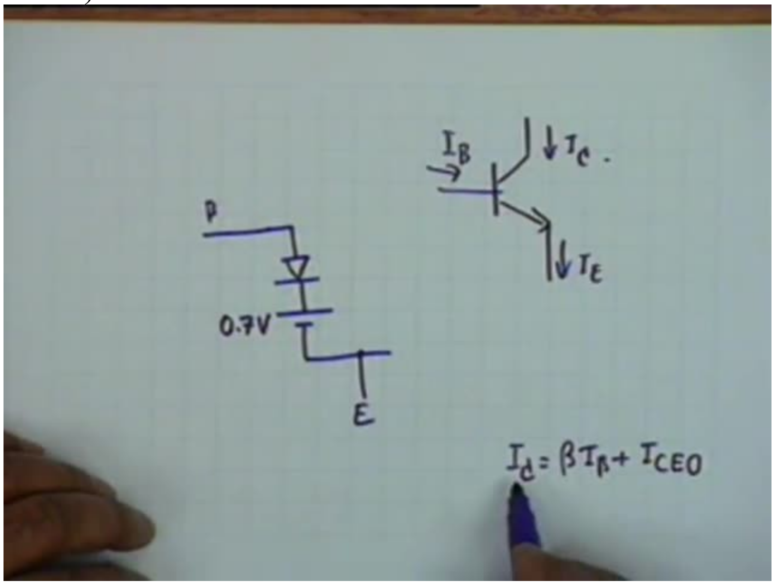

As you can see here also. It is independent of each, it is almost parallel to the VCE axis except for this region except for this region where VCE is so small that the collector base junction can no longer be reverse biased. It becomes forward biased and this region where the current increases with VCE is a very small region very small region and is called the saturation region. We shall come back to this later. As far as amplification is concerned, we are concerned with the part of the characteristic where equal increments of IB lead to equal increments of I sub C. This is the region which we are interested in for amplification.

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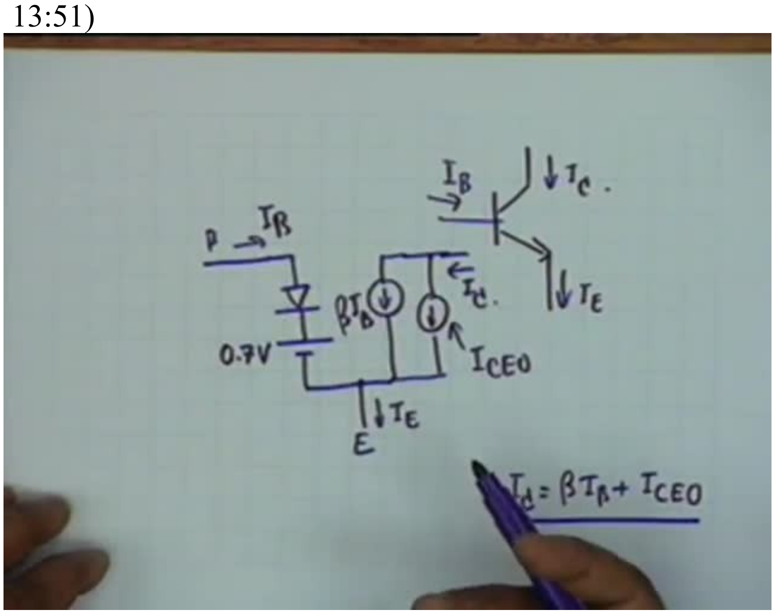

Now this characteristic I sub C equal to beta IB + I CEO can be represented by simply 2 current generators. One of them, well this current is IB, the input current is IB and this current is I sub C, this current is I sub E and the 2 current generators, one would be beta IB and the other would be I CEO. This is the simple DC model of the (tra) common emitter transistor. And in any circuit analysis, well you can utilise this equivalent model. Then life becomes very simple. Utilising this model, one can now analyse to see why a transistor behaves like it does. Why does it amplify?

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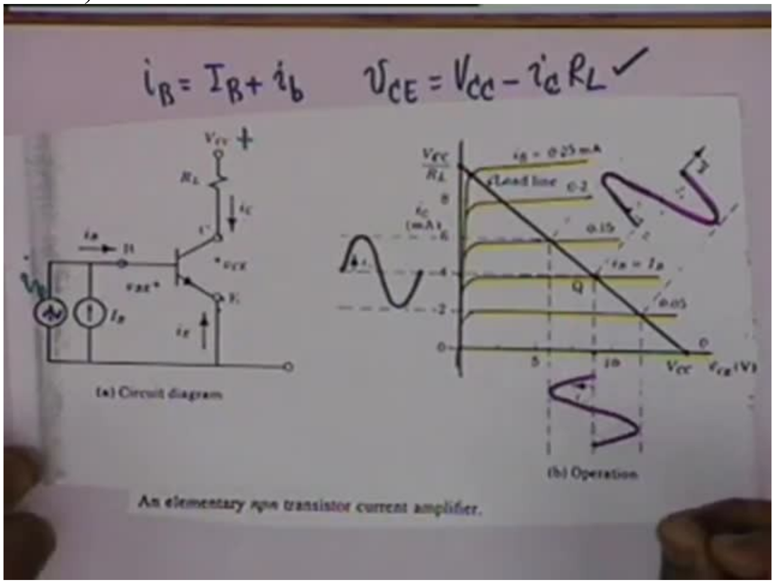

$i_B = I_B + i_b \quad v_{CE} = V_{CC} - i_C R_L$ ✓

(a) Circuit diagram

(b) Operation

An elementary npn transistor current amplifier.

Well, you see here is a transistor, a common emitter transistor which is connected to a positive supply here, VCC. It has to be connected to a positive supply because the collector base junction has to be reverse biased. This is an npn transistor, this is n, this is p and this is n. So n must be connected to positive supply to make it reverse biased. Then, it is connected to the collector through a resistance which is called the load resistance RL. This is the transistor. For simplicity, E is shown connected directly to the output to the common terminal Jack and to the base are connected sources, 2 current sources.

One is a DC current source, Is capital I sub capital B, a DC current source and this is an AC current source or a signal source small ib and therefore the total current, total current I sub capital B total current shall be the sum of the 2. That is I sub capital B + small i sub small b. small i sub small b, this is a varying current, this is the signal current whereas this is a steady current, I sub B established by some battery and some resistances as we will see later. Now if you look at the characteristics, we have plotted the same characteristics against. In addition, this red line here simply specifies the fact that VCE, the collector to emitter voltage must be the supply - the drop in RL.

That means VCE is equal to VCC - I sub C times RL which is the question to a straight line. All right? This is These characteristics are non-linear characteristics and therefore what we do this, we have to satisfy VCE and I sub C should satisfy this relation and also the characteristic curves. And therefore, we draw this straight line on the characteristic curve. How do you draw it? You put I sub C equal to 0 I sub C equal to 0, then VCE is equal to VCC. That means the the straight line starts from this point where this point is VCC and then we put VCE equal to 0.

Under that condition, I sub C should be VCC by RL. So it must pass through this point which is VCC by RL and you know a straight line can be specified by 2 points. So you join them and that becomes your load line. It is a straight line dictated by the load. It is a straight line dictated by the load. Also of course, the supply voltage VCC all right? Now to find out where the transistor operates, that is what would be the value of VCC and I sub C. It must satisfy two equations, one is a non-linear equation specified by the characteristic curve, the other is a linear equation specified by this line and therefore the intersection of these 2 shall determine, the operating point of the transistor or the so-called Q point of the transistor.

And if I specify if I figure out from here, from the characteristic curve, which one is the curve for the specified value of IB? Now ignore small iB. Small iB is a small variation or perturbation over the study value of IB. I identified that this is the curve on which which corresponds to the given value of IB. Then I find out where does it intersect. This is the point and this is my Q point or left to itself, if there is no signal current, the transistor will set at this point. Set at this point means its VCE will be would be equal to this and the collector current would be (ek) equal to this.

This is about oh I do not know, 7.5. This is about 8 and this is about 4 milliamperes. So 8 volt and 4 milliampere. That is where it the transistor will set. Now suppose on this base current, on this steady base current is superimposed a small AC base current, small i small b which for simplicity, let us assume that it is sinusoidal with a peak value of 0.05 milliampere, that is this point Q corresponds to point 0.1 milliampere and when the base is current is maximum, it becomes 0.15 milliampere. So the Q point shifts to this point because this curve is for 0.15 milliampere and this curve is for 0.05 milliampere.

Equal changes in IB leads to equal changes in IC. This is the part that we are interested in. So when the base current fluctuates like this, when it goes to one complete cycle, what happens the collector current? At the peak of the base current, the collector current reaches the value 6 milliampere. At the trough or the or the minimum of the base current which corresponds to 0.05, the collector current is 2 milliampere and therefore therefore as the base current varies varies from 0.1 to 0.15, comes back to 0.1, goes back to 0.05 and then again comes back to 0.1, 1 cycle of the base current is completed, the collector current goes through a very similar variation.

When the base current increases, collector current increases. And if these lines are equi-spaced, that is equal base current increments lead to equal collector current increments, then obviously this curve shall also be sinusoidal all right? So a small base current here is able to control a large collector current here. If the peak to peak current here this 0.05 milliampere, and the peak. I am sorry, not peak to peak. Peak to peak is how much? 0.1. And peak to peak here is from 2 to 6, 4 okay.

So when the when the base current goes through a peak to peak variation of 0.1 milliampere, the collector current goes through a peak to peak variation of 4 milliampere and therefore the collect the current amplification factor is 40 all right? A small current at the base can produce large current variation in the collector. So there is current amplification by the transistor. In addition if you look at the phases, when the base current increases, the collector current also increases. So they are in phase. All right?

On the other hand, if you look at this voltage from collector to emitter, VCE, when the collector current increases, VCE decreases. And therefore, the VCE variation shall be out of phase with the input current variation. Is that clear? It is also shown here that when the base current increases, the collector to emitter voltage decreases. All right? When the base current decreases, the collector to emitter voltage increases. So there is a variation, corresponding variation in VCE but in opposite phase. And you see, the voltage now goes from 5 to 15, that is there is a 10 volt peak to peak variation. All right?

And this 10 volt peak to peak variation is a large amplitude variation caused by a very small current variation at the base. And therefore, there shall be a voltage amplification also. We would be able to say how much voltage variation if we knew the equivalent resistance between base and emitter. Well, we shall calculate this later but qualitatively, is the picture clear to you that the common emitter transistor can amplify current as well as voltage?

This amplification, the faithfulness of this amplification depends on where your Q point is. That is in absence of the signal, where does the transistor reside? For example, if your Q point is here if your Q point is here, that is the quiescent collector current is 0, then the transistor will conduct only when I sub B small i sub b is positive. Is not it right? In other words, the transition will now behave like a like a rectifier. That is, it will only produce the positive halfs. All right? The transistor is sometimes operated under this condition and this condition is known as class B operation, class B all right?

If the transistor is biased here, let the if the Q point is here then obviously, the positive halfs there shall be problems in amplification. The negative halfs shall have less problem in amplification. In other words, the output waveform that you shall get shall no longer remain sinusoidal. It shall be distorted all right? And therefore, for faithful amplification where the base current variation shall lead to an exact replica but an amplified or magnified replica in the collector current, you require that part of the characteristics where the lines are equi-spaced, that is equal increments of base current lead to equal increments of collector current. Jack. This is the basic idea of amplification, how a transistor can be used as an amplifier.

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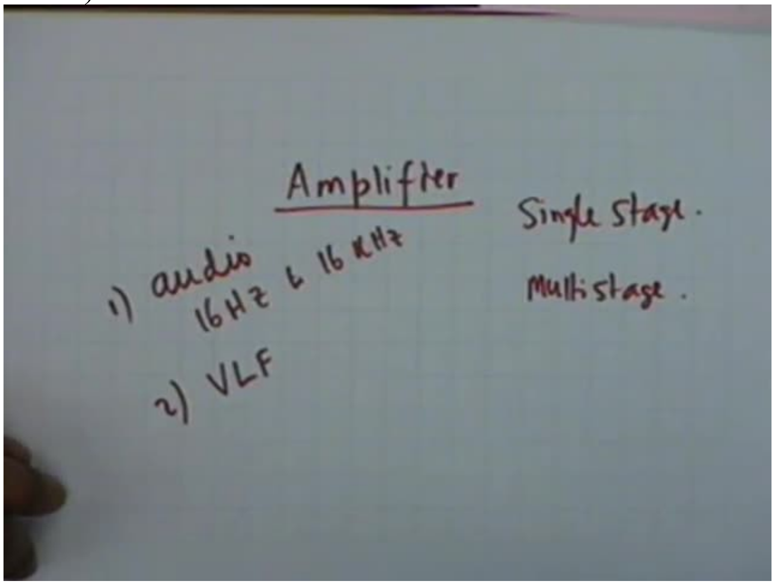

Before we take up this topic again in an actual circuit and see how the Q point is determined, let us clarify a couple of concepts, couple of terminologies that are used in connection with an amplifier. Amplifiers can be single stage or multistage. That is, if we use one transistor and around it, you introduce resistors, power supply to get some amplification, one stage, that is one device, is called a single stage amplifier. Now single stage amplifier obviously shall have limitation on the gain. How much amplification? How much amplification?

So if you want more amplification or more gain, you might use 2 such stages. Such amplifiers are called multistage amplifiers and it should be clear in the context, whether an amplifier, a given amplifier is a single stage or a multistage. For example, a stereo amplifier is is a usually a 3 stage amplifier, is a multistage amplifier. The 1st stage is a voltage amplifier matching microphone to the amplifier system, 2nd stage is another voltage amplifier and the last stage is a power amplifier because you have to feed power to a loud speaker.

Amplifiers can be single stage or multistage. Depending on the frequency range of operation, amplifiers can be classified as audio amplifiers, that is amplifiers which are useful in the audio range of frequencies which is 16 hertz to 16 kilo hertz Jack. 16 hertz to 16 kilo hertz you can have for example, VLF amplifiers, very low frequency amplifiers like those used in biomedical applications Jack where frequencies encountered are of the order of a fraction of a hertz or in process control, a sulphuric acid plant where the variations are very slow, very low frequency amplifiers.

Or you can have let us say video amplifiers where the frequency range may vary from 30 hertz to about 4 megahertz or higher okay? Video amplifier and so on. You can so you can classify amplifiers on the basis of number of stages, on the basis of their frequency range, then on the basis of the bandwidth.

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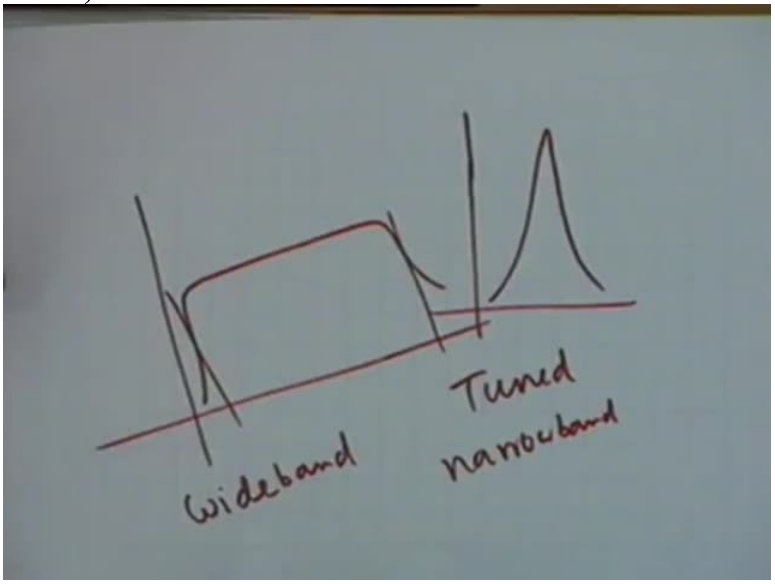

You might require an amplifier Jack as you do in the case of a radio receiver or a TV receiver so that only a narrow band of frequencies are required around a centre frequency. Well, then it is called, such an amplifier is called a tuned amplifier. On the other hand, you can have, tuned amplifier has a narrow band okay, tuned or narrowband. On the other hand if you want an audio amplifier, well obviously what you need is something like this where the 3 dB frequencies are 16 hertz and 16 kilo hertz and therefore, this is a wideband amplifier okay. These are some of the terminologies that we shall be using in future. Single stage, multistage, audio, video, VLF and narrowband or wideband amplifiers. How do you characterise amplifiers?

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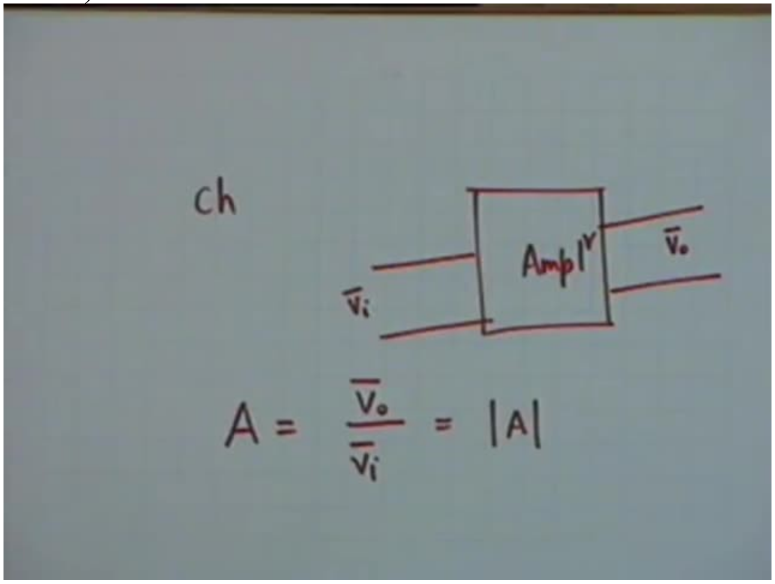

$$A = \frac{\bar{V}_o}{\bar{V}_i} = |A|$$

Now we consider an amplifier as as a black box. There are input terminals, there are output terminals and mostly amplifiers are characterised by sinusoidal inputs and therefore one can work in terms of phasors. Let us say that the input phasor is VI and the output phasor is VO all right? Then the gain or amplification of the amplifier is denoted by V0 the ratio of the output phasor to the input phasor. Obviously, this would be a complex quantity. This would be a complex quantity, there would be a magnitude which is the ratio of the 2 magnitudes of the voltages and there would be a phase, e to the power j theta all right?

If the gain if the (amplitu) if the amplification is dependent on the size of the signal all right, then obviously then obviously equal increments of the input current may not lead to equal increments of the output current. If that happens, then you have good amplification.

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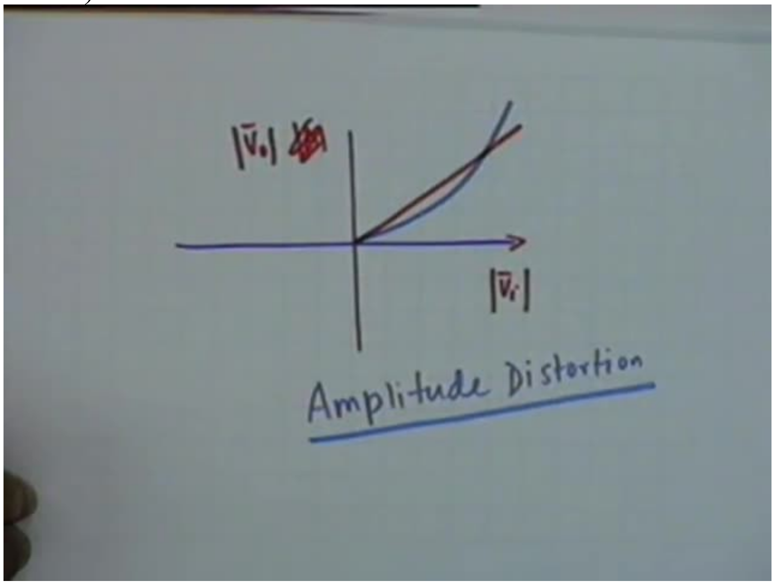

But suppose you have an amplifier suppose you have an amplifier whose characteristic, ideal characteristic would be like this okay. The gain vs signal strength, let us say VI. No, I am sorry. V0 vs VI, it should be a straight line all right with a slope of magnitude of A all right. Now suppose the characteristic is like this. Instead of a straight line, suppose the characteristic is like this. Then obviously obviously a sinusoidal signal shall not give you a sinusoidal output. Is that clear? The output shall be distorted. Agreed? Such distortion is called amplitude distortion amplitude distortion.

Is that clear? The characteristic that I want is that the output voltage should be linearly proportional to the input voltage. If this is not so, then a sinusoidal signal shall not give rise to a sinusoidal. It should give rise to a distorted sinusoid and under this condition, we say the (ampli) amplifier produces amplitude distortion which is very commonly the case with public address system, particularly those used for large rallies and so on. The voice is not detectable. In fact, if we put music on such a public address system, it is massacre.

For musical reproduction, we require a very very good linearity of amplification. On the other hand, the speech, most of it is not paid attention to, so somebody speaks, that is about it. And there is a large crowd okay. We will make TV news, the actual content of the speech is not important and therefore lot of amplitude distortion is tolerated in a public address system. It cannot be tolerated in music.

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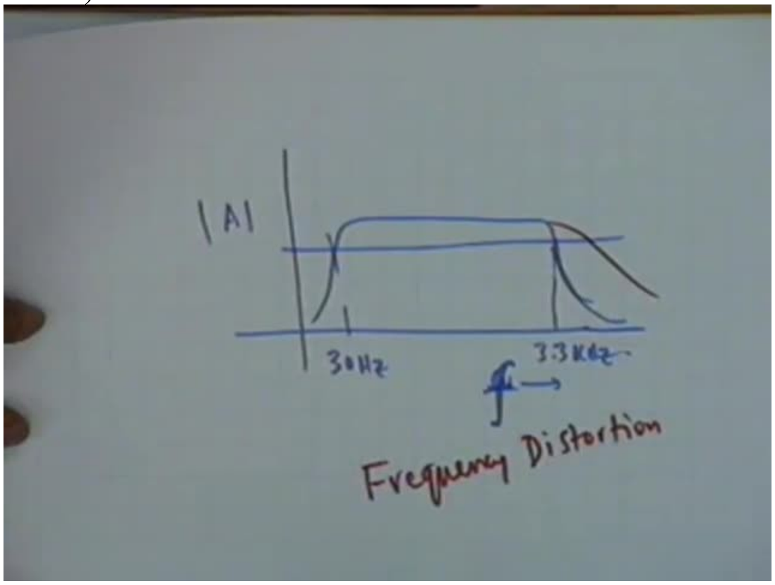

On the other hand, if you have an amplifier whose gain is sensitive to frequency, as I have said, for an audio stage, it is like this okay. Now suppose suppose the 3 dB points are 30 hertz to let us say 3.3 kilo hertz as is used in reproduction of speech signals then obviously if it is the full band audio, then such an amplifier cannot take, this is frequency in hertz. Such an amplifier cannot reproduce the full audio, that is beyond 3.3 up to about 16 kilo hertz, the gain has come down. Obviously this is also going to produce distortion all right.

This is like this is like decreasing the treble. In a stereo set, you have two controls, one is the bass control, the other is a treble control. Bass control means you either increase or decrease the low-frequency 3 dB point. If you increase the bass, the drums will come better, the tabla sound for example. On the other hand, if you increase the treble if you increase the treble, this means that you are increasing the high-frequency 3 dB point. That means, you are admitting more high-frequency and therefore a violin sound sweeter if the treble control is increased all right.

The point that I am making is that if the signal consists of certain band of frequencies and the amplifier cannot accommodate total band, it accommodates only a part of it, obviously there shall be distortion all right. For example, if you cut off the high frequency, Lata mangeshkar will not sound like Lata mangeshkar. She will sound like, I do not know. Give her (())(35:16) baser voice (())(35:17), would that be all right? Okay, so this distortion is called frequency distortion.

We have discussed 2 kinds of distortion. One is amplitude distortion and the other is frequency distortion.

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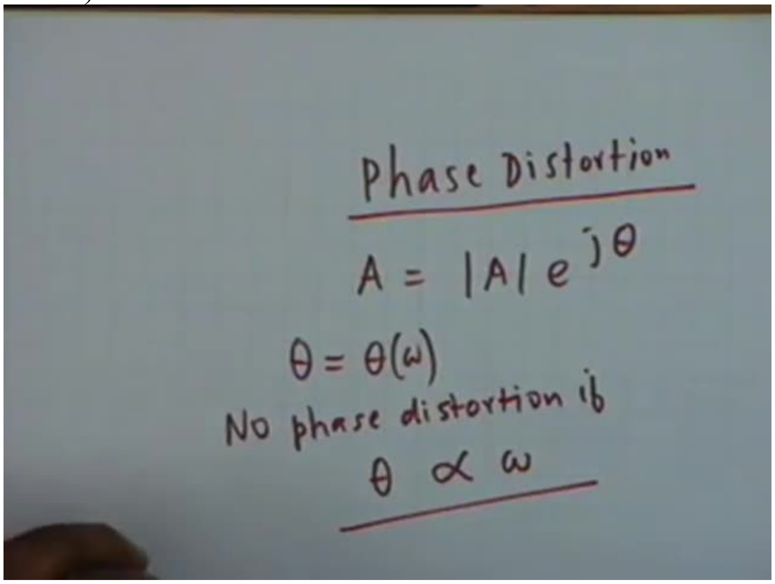

Phase Distortion

$A = |A| e^{j\theta}$

$\theta = \theta(\omega)$

No phase distortion if

$\theta \propto \omega$

There is still a 3rd kind of distortion that one has to bother about and this is the so-called phase distortion. I shall simply state this without proof that phase distortion has to do with the angle theta. Theta usually is a function of omega. If theta is a function of omega then no phase distortion shall occur. No phase distortion shall occur if theta is a linear function of omega, if theta is proportional to omega. All right. If theta is proportional to omega, no phase distortion shall occur.

Now let me mention to you a particular situation where the situations where phase distortion is important. Phase distortion, fortunately or unfortunately cannot be detected by the ear. That is, our hearing capability is insensitive to phase distortion. Even if the phase is non-linear, it does not matter but phase distortion, our vision is very sensitive to phase distortion. So in a TV for example, the picture cannot have the phase distortion. If it does a phase distortion, you will see all kinds of distortion, will not see the correct picture.

On the other hand if it is the audio, the sound, we do not care what the phase distortion is all right. Beside this general rule, you need not know much more about phase distortion at this point of time.

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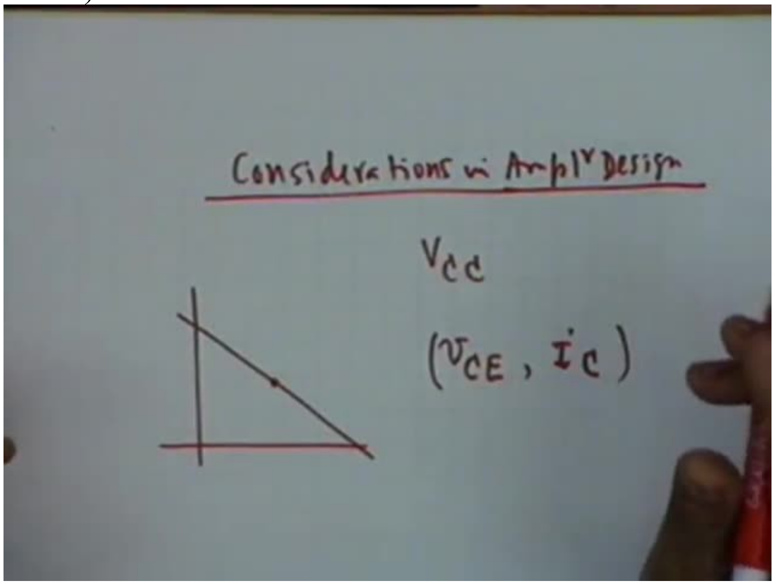

Considerations in Ampl^r Design

V_{CC}

(V_{CE}, I_C)

Then what are the considerations in amplifier design? Considerations in amplifier design Jack. As I have shown you with the help of the common emitter characteristics, obviously the Q point of the transistor is important. If the Q point is at a round point then you might get a lot of distortion in the amplification. And therefore, the transistor must be biased properly. That is, your choice of VCC and the resistors used to bias the transistor to a particular VCE and a particular I sub C, these are the 2 points that determine the Q point of the transistor.

You remember, there was a load line and the Q point was somewhere in the middle. To establish this Q point at an appropriate point in the characteristic is an extremely important task. So the 1st consideration in amplifier design is its biasing. Then there are other considerations like if you want to if you want a multistage amplifier, if you want to couple one stage to the a to the other, well then coupling is important, how do you couple?

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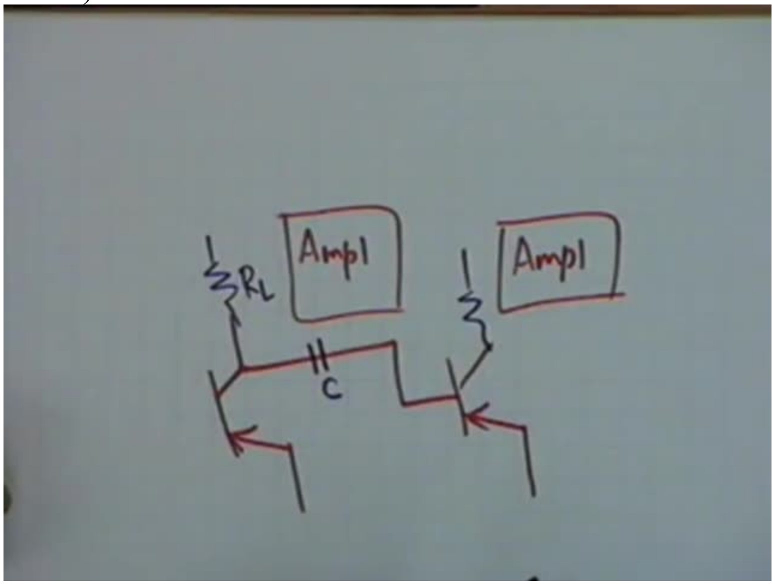

For example, you have one amplifier stage and another amplifier stage here. How do you couple? Suppose you take, you connect the collector of one stage directly to the base of the next stage. Can you connect it directly? Well, the problem is that this would be at a high voltage VCE. If you connect this to the base, then the base, base does not require that high voltage and therefore DC coupling may introduce distortion. And what you have to do is to introduce a C here, a capacitor so that DC is blocked but AC is passed.

And there is a load here, RL. There is a load here. For every transistor, there is a load and therefore this coupling is called RC coupling, resistance capacitance coupling all right. On the other hand there can be other kinds of coupling. For example, if the capacitor is not there, then we call it direct coupling. It is not that direct coupling is not used. It is also used in some places. So direct coupling can be used, RC coupling can be used. One can also use transformer coupling as is done for example at the last stage of a stereo amplifier.

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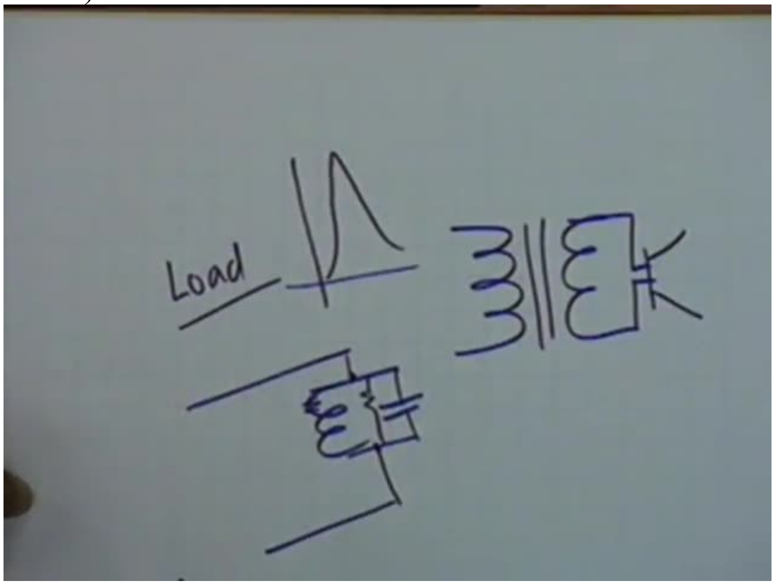

At the last stage of stereo amplifier, the transistor feeds a transformer primary, the secondary of which is connected to the loudspeaker. Okay. This is called transformer coupling. So coupling is an important consideration in amplifier design. Then the load, nature of the load, obviously the load. load can be resistive, can be inductive, can be capacitive, all kinds of loads. For example, a loudspeaker is usually considered a resistive load. On the other hand, a radio-frequency stage may have a load like this.

You may have a load like a parallel tuned circuit, parallel resonant circuit. What is the impedance at resonance? Infinity. What is the impedance at resonance of this circuit? Infinity. And therefore, jack you will see later that the gain of such an amplifier is proportional to the load. And therefore, you expect infinite gain from this. Actually, you do not get infinite gain because the inductance has resistance, the capacitor has a resistance in parallel and therefore, you can get a large gain all right? And that is how you get a characteristic like this. A tuned characteristic. So the nature of the load whether it is resistive, inductive, capacitive or tuned, it is important.

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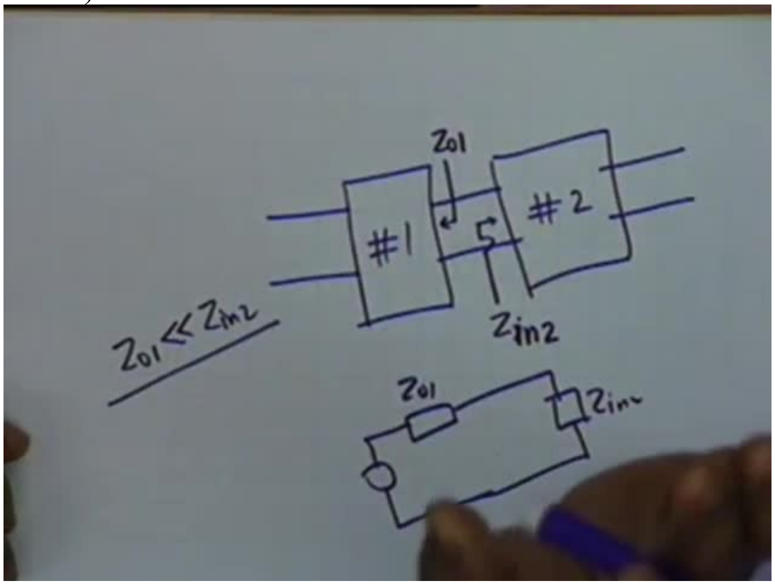

It is also important to consider, when you are connecting one amplifier stage to another, suppose this is stage 1 and this is stage 2, it is important to consider what is the input impedance of this stage Zin and what is the output impedance of this stage Z01 and Zin2. It is important to consider the relative proportion of these 2 all right. Suppose Z01 is very large and Zin2 is very small all right. Then then only a small fraction of the 1st stage output shall be coupled to the 2nd. Is not it right? Because the Thevenin equivalence says that you have Z01, a voltage source, then you are connecting to Zin2.

If Zin2 is very small compared to Z01 then obviously very little voltage shall go to the 2nd stage. So what is the consideration then? Z01 must be very small compared to the input impedance of the stage that it couples to, Zin2 all right. This consideration is extremely important. On the other hand, there are situations where you when you are not interested in transferring voltage. You are interested in transferring power. Well, what do you do there? You make impedance matching. That is, if you are interested in transferring maximum power from this stage to this, then Z01 and Zin2 should be complex conjugates of each other and therefore it is important what your application is.

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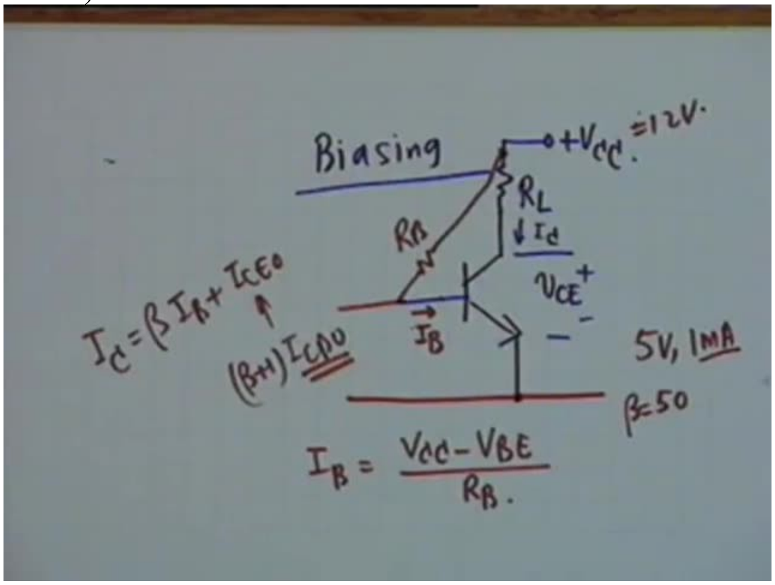

You have a a transistor, you have a load all right and you have a + VCC. You have a load RL, you wish to establish a particular VCE and a particular I sub C. So the condition the condition will be satisfied if you can find out the appropriate base current and establish the corresponding base current. And one of the ways that this can be done with a single battery is that the same battery is connected to the base through a resistance let us say RB all right. Then this will be the base current, the DC base current, I sub B. Okay.

This is the circuit. This is one of the simplest circuits for establishing for biasing the transistor. Obviously, I sub B the base current here shall be equal to the drop in RB. What is the drop in RB? This is VCC - the drop between base and emitter. And if you recall the DC equivalent circuit, this is 0.7 and therefore this will be VCC - VBE which is 0.7 divided by R sub B all right? And the job seems to be seems to have been done. This will be IB. Beta times IB + I CEO shall be I sub C. I sub C will be beta times IB + I CEO which normally which normally is negligible.

And therefore if you know the beta of the transformer, you know what is I sub C all right and if you know I sub C, then you can determine RL to find out a specific value of VCE. For example, if VCE is equal to be 5 volt and I sub C is equal to be 1 milliampere with a beta of 50 beta of 50 then you know what your IB required is. IB will be 50 I am sorry 1 milliampere divided by 50, 0.02 milliampere and if VCE is 12 volt, then 12 - 0.7 divided by the resistance, that will determine IB. So you know RB all right and then since you know collector current, 1 milliampere, you want 5 volts here, so 7 volts should be dropped here.

They are very simple calculations and therefore you know RL. The disadvantage of this is that if this transistor goes bad and you replace it by another transistor of the same type, then the Q point will go haywire. The reason is the following that in mass production of transistors even though they are produced by the same process, about 1000 is perhaps the minimum number that is that is produced or fabricated in one go, these transistors vary very widely. In other words, beta can vary by a ratio of approximately 6 is to 1. You can have a lot of transistors 2N110, one thousand of them and you go on measuring beta, the lower is better maybe as low as 30, the highest maybe as low as 180, 6 is to 1 variation.

And therefore as soon as you replace the transistor, the Q point changes. Similarly, this as you see I CEO is beta + 1 I CBO. And as soon as temperature changes, I CBO as you know doubles for every 10 degrees centigrade rise in temperature. The law of variation of I CBO approximately is that it doubles for every 10 degrees centigrade rise of temperature and therefore if temperature changes, then I CBO rises, this quantity changes and therefore once again the Q point goes bad. Not only that, the most drastic disadvantage of this circuit is funeral to have to follow me carefully.

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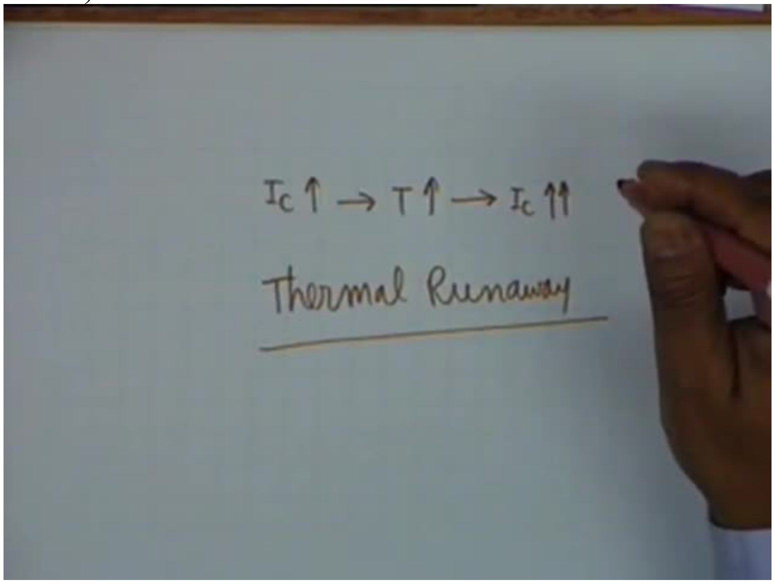

Suppose due to a small change of temperature, in this circuit, I sub C increases. Suppose due to a small change of temperature, I sub C increases, this collector current increases. Now what happens? If collector current increases, naturally the the heat dissipation in the transistor also increases. That is VCE times IC increases all right. Now this heat is generated here and is to be dissipated in the transistor and therefore it causes a further rise of temperature all right. If I sub C increases, temperature increases.

If temperature increases, I sub C further increases all right. And this can now be a merry-go-round situation and ultimately the transistor will be burnt. This process is called a thermal runaway. This process of burning a transistor should never be resorted to but it does happen in practice and the process is known as thermal runaway. It should be avoided. And this is one of the main disadvantages of this particular circuit. A circuit in which this does not happen has to be designed on the basis of a different kind of philosophy. The philosophy in this circuit was to to establish a particular IB, to establish a particular base current.

The base current is a constant. The collector current is not a constant. All right? Because it varies with beta, it varies with I CEO. If I change the philosophy of maintaining a constant I sub C, base current let it adjust to get a particular value of I sub C, then this process of thermal runaway shall be arrested.

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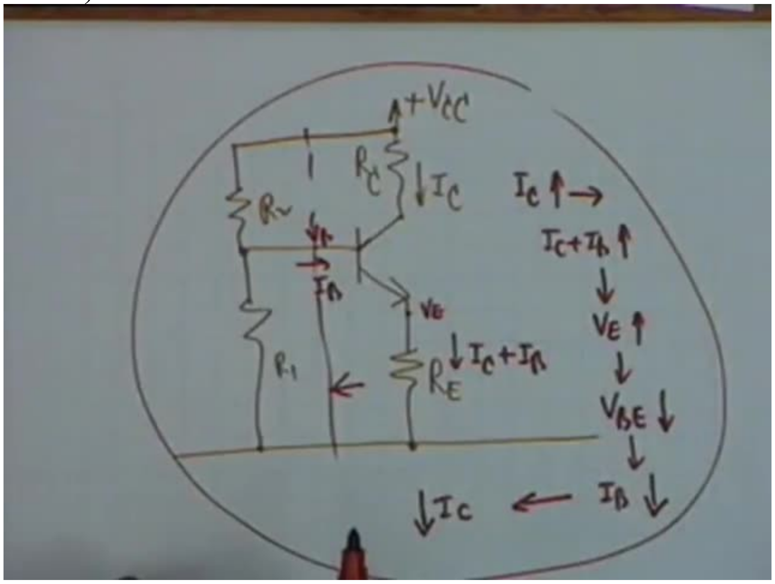

And this is done by a circuit which is known as a self biased circuit. It is a very simple circuit. You have 2 resistors here. This is + VCC, this is I sub C, call this R sub C and call this R sub E. In the emitter also, there is a resistance and the base is biased not through one resistance but through 2 resistances, that is R1 and R2 R1 and R2. If you look at if you look at this circuit from the left of this line, obviously it is a battery VCC supplying a series connection R2 and R1. The drop in R1 then supplies the base. The base voltage VBG ground, you call this simply VB is simply the drop at drop across R1 which is equal to VBE + the drop across RE.

Now let us see what happens. Suppose I sub C due to some reason increases, what is the current through this? What is the current through RE? IC + IB. This is the current IB. Now see what happens qualitatively. We shall analyse this quantitatively later. If I sub C increases, then I sub C + I sub B also increases. If that increases, then what does it have what happens? The drop across RE, you call this VE. VE increases. If VE increases, then what happens to VBE? Decreases. Is not it right?

VBE, this drop shall then decrease. If VBE decreases, what happens? I sub B. If the diode voltage decreases, I sub B decreases and I sub C is nothing but beta times I sub B + I CEO. So if IB decreases, then what happens to IC? IC decreases. You see, the increasing tendency of IC is arrested. In other words, there is a feedback mechanism which tends to keep I sub C stable and in such a connection, the transistor can never burn down. Thermal runaway is arrested and this is one of the most popular biasing circuits. Next time, we shall make a thorough analysis of this and see the stability of the biasing.