Analog Electronic Circuits
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Lecture No 07
FET Biasing,
Current Sources.

FET biasing and current sources.

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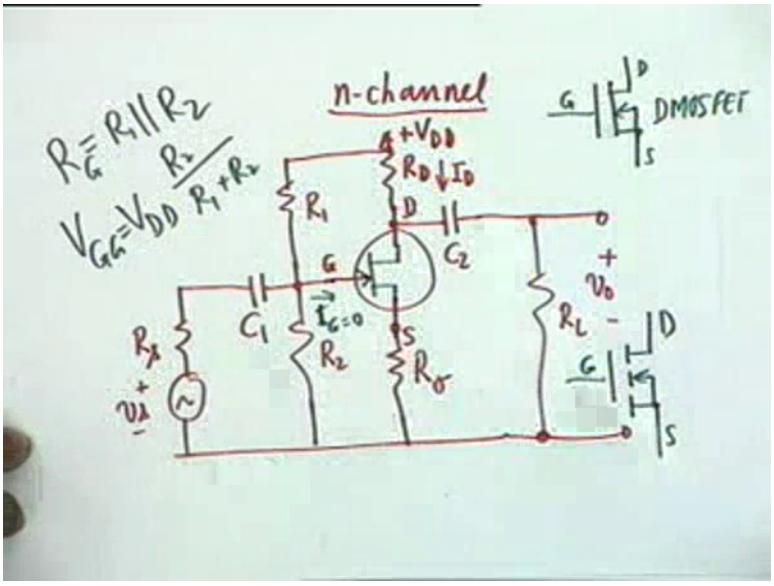

As far as FET biasing is concerned if we consider an n-channel device the circuit is the same. Whether it is a JFET or a MOSFET. Even if it is a MOSFET it could be either depletion type or enhancement type. The circuit is the same, so if we discuss, if we consider and FET is having 3 terminals. Gate, Drain and Source. Symbol is different for different types of FET but we're considering n-channel then we have to have a resistance R D and this goes to a source of voltage V D D. Note the change of symbols. The drain instead of collector, so R D and V D D and the current through R D is I D and then the gate biasing is done in exactly the same manner as we do the base biasing in a BJT. That is we use 2 resistances. R1 and R2 and at the source we use another resistance exactly like emitter resistance and to distinguish this from the source resistance signal source resistance okay. You know the signal source would be here. And this usually we call R S and this is the signal source V S, in order to distinguish between R S the

source internal resistance and the resistance connected to the source terminal of the FET we denote this by R sigma you understand the meaning of this subscript sigma.

This is just to distinguish between this resistance and this resistance. Of course the output is taken from the collector, not collector the drain and there is a resistance R L across which the signal output is taken okay. Now unlike alright, let me recall the symbols. If it is a JFET the symbol would have been simply this, n-channel JFET. If it is an MOSFET of depletion type, now the depletion type, two lines. And you have drain, this is the connection on the other hand this is the depletion type MOSFET DMOSFET. On the other hand if this is an enhancement type then you have 3 lines like this. This is the drain, this is the source and this is the gate okay. In either of these 3, in any of these 3 devices the same circuit shall be shall be effective.

Now you notice that the difference between BJT and FET is that the gate is virtually insulated. If it is MOS it is DC insulated absolutely metal oxide semiconductor so it's a capacitor basically. So the gate does not take any current. Gate does not take any current.

Student: Sir in MOSFET?

Professor: In MOSFET.

In JFET the gate and source is a reverse biased junction, the gate and source is a reverse biased junction and therefore that also takes negligible current. In other words the gate current I G can be taken to be 0. The gate current I G can be taken to be 0. So the FET basically and you know the gate controls the current I D, the gate to source voltage controls the current I D. So FET is basically a voltage controlled device alright.

You've also noticed that as far as DC is concerned the voltage at the gate is simply V G G equal to V D D R 2 divided by R 1 plus R 2 agreed? So this is the equivalent of V B B agreed? Equivalent to V B B in a B J T alright. And the equivalent of the resistance R B would be the parallel combination of R 1 and R 2 alright? But it does not go as in a BJT, it does not go to a diode. It goes to an open circuit alright? And I D is the I D is the drain current. Let us look at the DC equivalent circuit of this.

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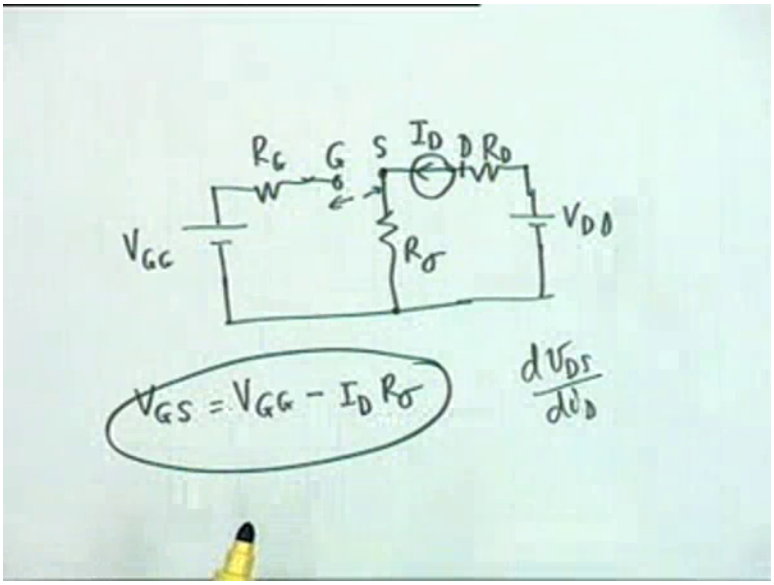

We have a battery V G G, V G G then we have the resistance R G which we have already defined. This is the gate terminal and this remains open alright. At the at the other terminal we have, what do we have a V D D okay in series with a resistance of R D and a what? Where does R D go? Isn't there a current source? There is a current course which is I D we're considering DC equivalent circuit there is a current source I D. Then this goes to, what is this terminal now? No, the drain terminal is here.

Student: Source

This is the source terminal and therefore from here we have the current as the resistance as signal to the ground. Okay, this is equivalent circuit.

Student: Sir we choose the drain terminal also from this?

Professor: Tell me which is the drain terminal?

Student: Just before the current source.

Professor: Just before the current source that is correct, this is the drain terminal.

Student: Won't there be a resistance of n-channel.

Professor: We will come to this later.

This is that R B which we shall consider for dynamic resistance. Small r Subscript small d that is d i d, I am sorry d V D S d i d. What we're talking of is this the dynamic resistance. This we shall consider in the AC equivalent circuit. As far as DC is concerned we don't have to.

Okay now you notice that here the controlling voltage is V G S, V G S that is this voltage. This is the controlling voltage. And you notice that this is, since the gate current is 0, this is equal to V G G minus the source voltage is I D, R sigma, is that clear? This is the golden relationship that we shall have to explore. Now let's review little bit about what we learnt about the different kind of FET. Let's review the relationships the we shall go to this relationship and see how to explore this.

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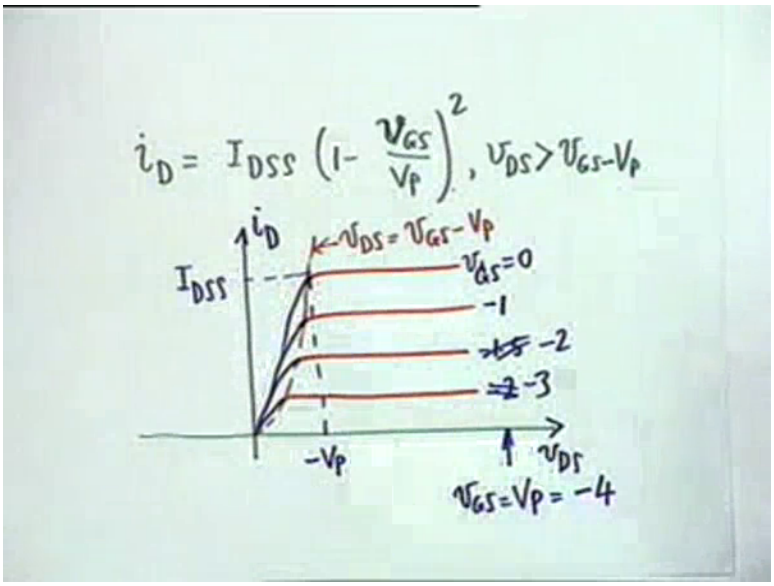

You know that the drain current in an FET is given by, if it is a junction type is given by I D S S, 1 minus V G S divided by V P whole square provided V D S is greater than V G S minus V P where V P is a pinch-off voltage okay. For an n-channel JFET V P is usually a negative quantity. V P typically is let say minus 3 volts and your V G S the gate to source voltage has to be less negative than 3 volts. In order for the transistor to conduct. In other words,

Student: Sir is there any equivalent region like saturated cut-off (())(0:10:43)

Professor: Yes, if you remember the characteristics, characteristics are exactly similar to a BJT characteristic except that there is a slope here, there is a slope here and the characteristics are like

this okay. This line given by V D S is equal to V G S minus V P, this line okay. And before that, before this line the characteristics is like this, this is the ohmic region okay. If this is for V G S equal to 0 alright then this voltage this voltage, this is minus V P alright, because this line is V B S equal to V G S minus V P alright. So the the flat portion of the characteristics which is saturation characteristics. The current reaches saturation there and this current for V G S equal to 0 is obviously I D S S the drain current under saturation condition. And this is I D.

Student: Basically we are talking about saturation region in this?

Professor: That is correct.

The FET must be operated in the saturation region, it is there that you can explore the characteristics for a linear amplification. And as you go down V G S becomes negative. Let’s say minus may be 1 minus 1.5 this may be minus 2, well these are not to scale. And what is this line corresponds to? V G S equal to..

Student: Minus 3

Professor: Not minus V P.

Simply V P, so this is the cut-off line, this is the cut-off line and these are the saturation characteristics okay. Let's make them (())(0:12:57) may be this minus 3, in this case V P is approximately minus 4 volts, you can't go beyond this.

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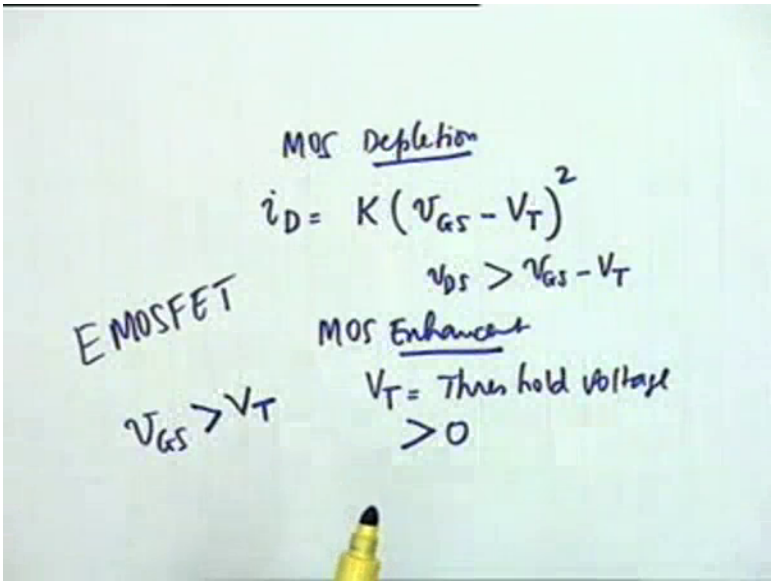

On the other hand if the transistor if the FET is MOS type MOS diffusion type okay if it is MOS depletion then the characteristics are written like some constant K multiplied by V G S mins V T square again V D S must be greater than V G S minus V T otherwise it is 0, otherwise this is ohmic region okay. And V T if it is depletion then V T is indeed a pinch-off voltage and V T is a small negative quantity, it's a small negative quantity. On the other hand if it is MOS enhancement type then the same relationship hold that V T is now a threshold voltage threshold voltage and has a slightly positive value, V T is greater than 0. For conduction V G S now mind this carefully small V G S in an enhancement type E MOSFET, enhancement MOSFET V G S has to be more positive than V T alright. If the 2 characteristics are drawn on the same graph that is the plot of I D versus V G S then for the depletion type.

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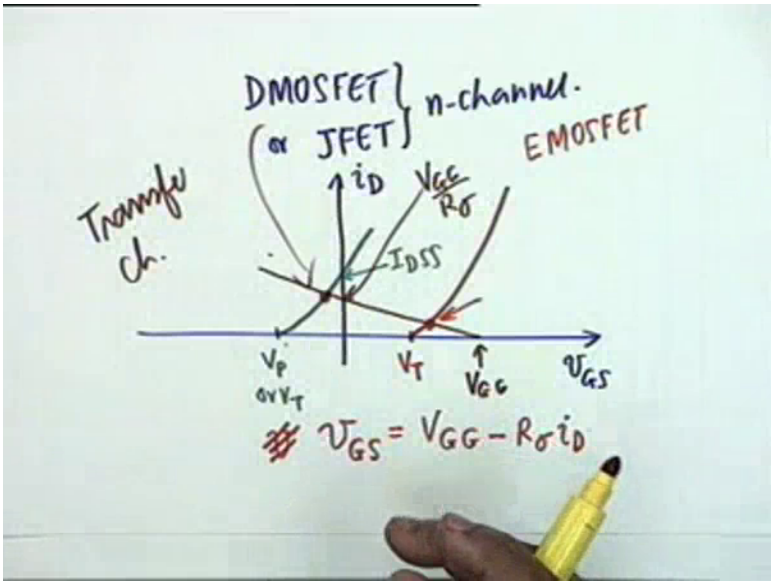

For the depletion type FET, that is DMOSFET or JFET both of n-channel the characteristics would be like this, this is d transfer characteristics, that is a plot of I D versus V G S, if you plot this obviously this would be a parabola a square law characteristics. And the characteristics when did it start? It would start from V P agreed or V T if it is DMOS. So this is a negative voltage so this is somewhere here. V P or V T and as the voltage exceeds V P that is when the voltage becomes less negative then V P the current rises and goes like this, it's a square law characteristics. Now what is this current I D S S because here V G S is equal to 0 okay. On the other hand if it is a enhancement type MOSFET then then V T is a small positive voltage V T and the characteristics goes like this, it's a parabolic characteristics, alright.

You notice also that in the biasing circuit our V we're considering DC alright. We can take the total voltage no problem V G S was equal to V G G minus R sigma I D right, this is the condition, this is the expression giving the gate to source voltage as a function of V G G and I D drain current. And you notice that this line this straight line can be drawn on this characteristic. I D versus V G S it is exactly the same as the load line. And it will start it will start at V G G and this current would be V G G by R sigma is that okay? So take these two points and draw the load line. This is the load line transfer load line, this is not these are not voltage and current at the same terminals okay the voltage is between gate and source and the current is in the drain a third terminal and therefore this is a transfer characteristics.

This picture is worth 1000 words. It takes JFET, DMOSFET, EMOSFET it shows the load line, it shows the operating point. Where is the operating point now? This is the operating point if it is EMOSFET and this is the operating point if it is DMOSFET or JFET alright. And therefore the Q point the Q point can be calculated graphically alright or it could also be done analytically. Let us look at how to do it analytically.

Student: Sir, what is the load line physically mean, what does it indicate?

Professor: Oh, it is the locus of variation of a current and the voltage.

In this case the load line is the locus of variation of drain current and gate source voltage. That is if the gate to source voltage varies then your characteristics your current variation must lie on this line. That's what it is. Okay now if I want to do it analytically.

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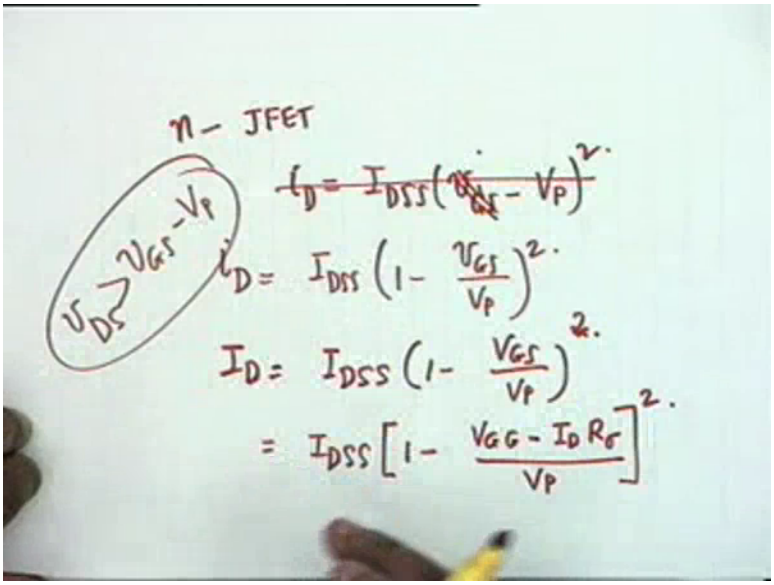

We have seen it how to do it graphically, if I want to do it analytically let's let us for example consider for specific specific case it will be a JFET. If it is a JFET n-channel JFET then I D is equal to I D S S, V G S minus V P whole square. No I beg your pardon, it is written differently. 1 oh let me write it again. I D S S, 1 minus V G S divided by V P whole square. I want to find the DC drain current okay. DC drain current and I know, then ofcourse I D under the DC conditions it is I D S S, 1 minus V G S by V P whole square in this you substitute the value of V G S. So it becomes I D S S, 1 minus what is V G S, V G S is V G G minus I D, R sigma divided by V P whole square and you see that the right hand side contains the unknown. The left hand side of course is the unknown. And therefore it is, what kind of equation?

Student: Quadratic.

Professor: It's a simple quadratic equation which can be solved for I D quadratic equation has two roots by the fundamental theorem of equations.

Student: Then I D should be positive.

Professor: One of them would be acceptable and other would not be acceptable. Now what will be the logic for rejecting one of the solutions. I D should be positive. Suppose both are positive. One of them one of them will violet the condition that V D S is greater than V G S minus V P, the one that satisfies this, the one that satisfies the relationship V D S greater than V G S minus V P

is the solution to be taken. And there will be a large number of examples that will work out in the tutorial class. And also I will work out some in the Thursday class okay. So you can either do graphically or analytically and it turns out that analytically it's not very difficult so why why turn to a graph and draw a graph and be inaccurate and all that okay. Now with this out of the way, let's look at the AC equivalent circuit, because the AC load line requires a knowledge of the AC equivalent circuit, let's take the same circuit as far as AC is concern.

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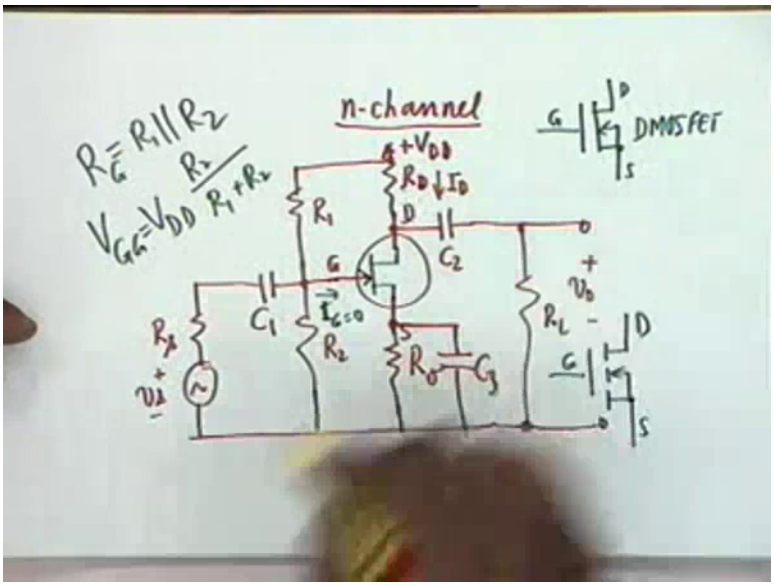

We shall have V S, R S the capacitor will become a short. And R 1 and R 2 they will combine into a single resistance R G which would be from the gate to ground. Is that correct? R 2 will come in parallel with R 1 because V D D is basically AC short. Then in the drain circuit, between the drain and the source we shall have a current generator, current generator which is incremental current generator okay, incremental current generator which we will find out. But that current generator shall feed and R sigma you can wish this away unless R sigma is short circuited alright. This capacitor we did not use earlier, now we bring in this capacitor C 3, R sigma is short circuited and this current generator incremental current generator infeed R D and R L. C 3 will be a short C 2 will be a short. So R D in parallel with R L. Now let's look at the circuit then we will explain further.

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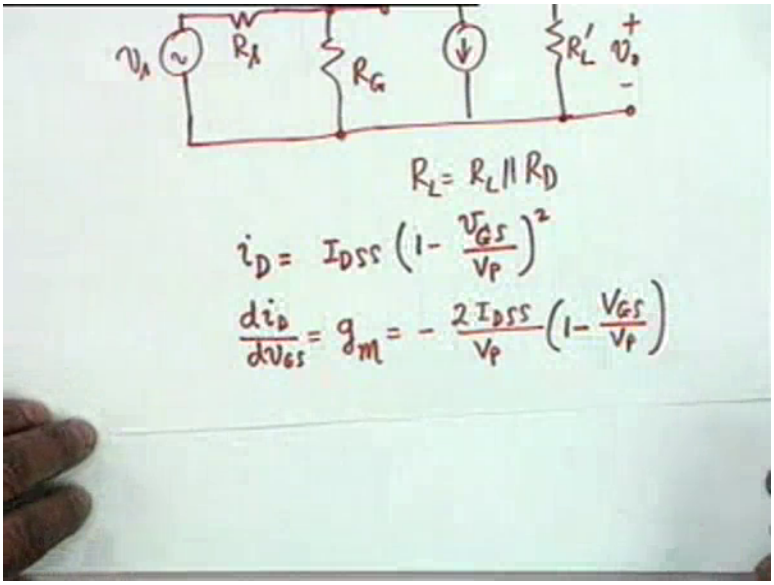

What we have is AC equivalent circuit. AC equivalent circuit V S will come in series with R S, this is the source resistance, then we have R G which is the parallel combination of R 1 and R 2. This is your gate and then you have a current generator. We will see what this current generator is in the BJT case it was beta small i subscript small b okay. Let us see what this is here. We will see it in a minute that what this puts is a parallel combination of this is R L prime where R L prime is R L parallel R D the drain resistance and this is the this is the output voltage V 0. Now to determine what this current generator is, you recall the total drain current is given by I D S S, 1 minus V G S divided by V P whole squared. Now what we have to do we should take the AC part of this, AC part of this obviously what we can do is take d I D, d V G S okay, what would be the dimension of this?

Student: Conductance.

Professor: It's a conductance.

So it's a conductance so it should be denoted by g, it's a dynamic conductance, it should be denoted by small g and because it relates a current in one terminal to the voltage across another 2 terminal it is a transfer conductance or a trans-conductance and if you differentiate this you can easily see that this is given by minus 2 I D S S divided by V P multiplied by 1 minus V G S divided by V P. Note that I have shifted to capital V G S why? Because this is to be evaluated at the Q point at the Q point. At the Q point the voltage V G S.

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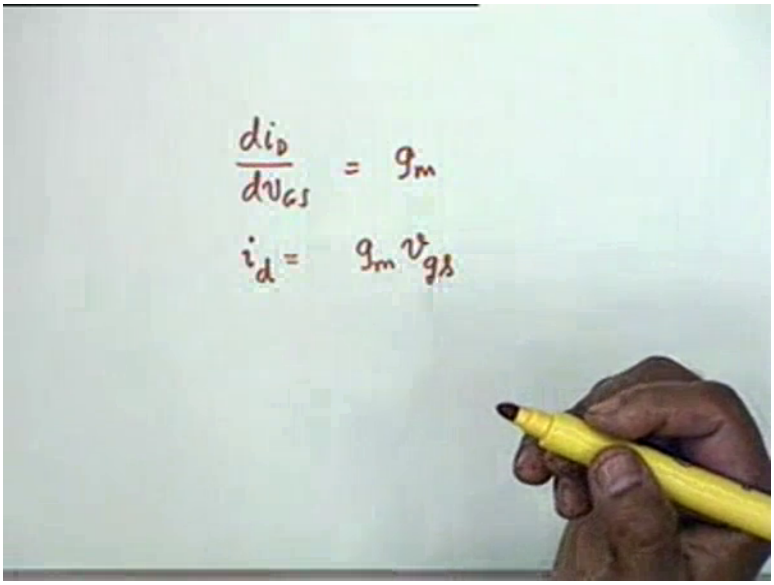

Now therefore what we have is d i D, d V G S, I have found out gm, this can be found for MOSFET the expression will be slightly different but you notice that d i D is increment in the total current, so d i D can be replaced by small i subscript small d and this is equal to gm times d V G S is increment in the gate to source voltage. So small v subscript small g small s.

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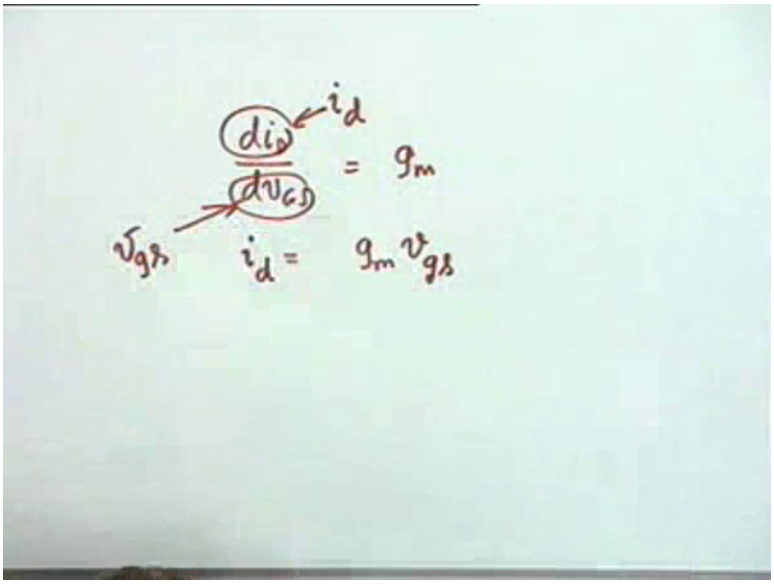

Therefore the current generator that you see here shall be gm times small V g s, this is the AC equivalent circuit okay. And you can make simple calculations of the gain, V 0 by V S very easy right. What is V G S? Where is the source now? This is the drain, where is the source?

Obviously this terminal is the source, why was the source come here? Because R sigma is grounded, R sigma is short circuited for AC.

Student: Sir how is the gm V G S AC?

Professor: How is the source, this is what I explained here. d i D, d V G S, d i D is the increment in gain current so it is i d and d V G S is increment in gate to source voltage. So this is V G S okay, so you can calculate the gain very very easily.

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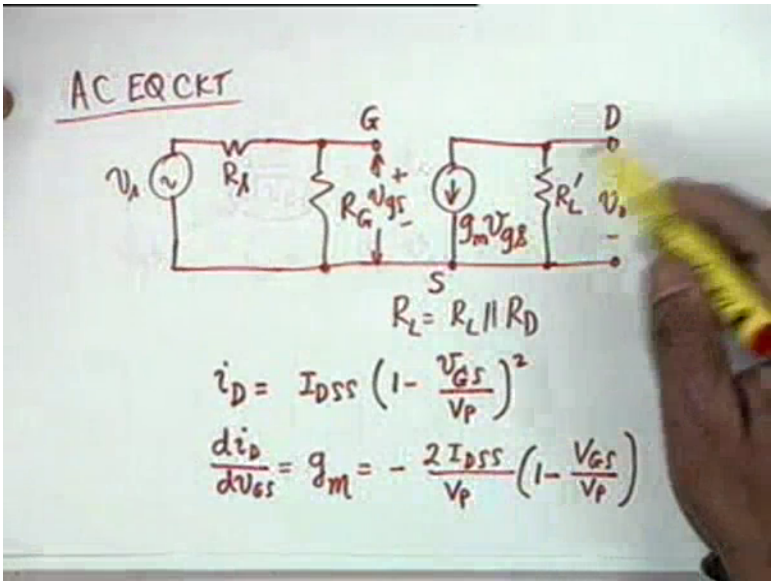

You can see that small v g s which is voltage between these two terminals is simply V S R G by R G plus R S. And V 0 would be minus gm V G S multiplied by R L prime and therefore it's a very simple matter of calculation to find out what the gain is. You remember in the case of BJT we had and alternative circuit in which R E was made equal to 0 alright but there was a feedback from the collector to the base, can we do the same with respect to FET? Let's draw this circuit.

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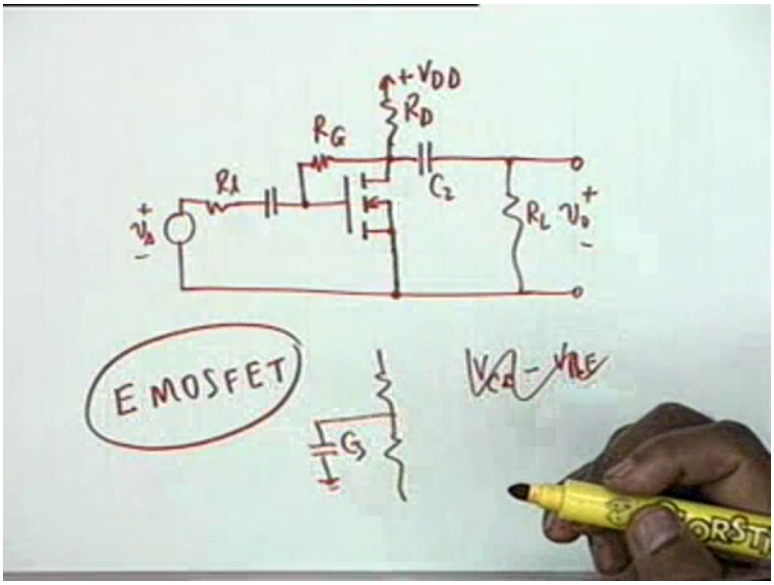

We have a V S, R S capacitance then we have the FET for reasons to be explained in a minute we show an enhancement type FET EMOSFET enhancement type MOSFET okay. I will explain this in a minute, why I am not drawing any other. R S is R sigma is 0, so it goes to ground. The drain terminal goes to plus V D D okay and the biasing, if I take the same type of circuit the biasing would be applied through a resistance what shall we call this resistance? R G in the previous case we had called it R B now this is a perfectly good way of biasing, you're output comes from here C 2 and this is R L, this is V 0. This is a perfectly good biasing provided it is an enhancement MOSFET you cannot replace this FET by a JFET or a DMOSFET and the reason is very simple, what is the reason?

For enhancement MOSFET V G S has to be positive, on the other hand if it is a depletion mode operation either a JFET or MOSFET your V G S is required to be negative this circuit cannot give you V G S equal to negative unless unless there is resistance here. If there is a resistance here then V G could be less than V S, but here V S is 0 identically. Therefore this is one of the differences between FET and BJT that this circuit is specific to EMOSFET and this is a popular circuit. Never make the mistake of having a biasing circuit for depletion mode with a circuit like this.

Student: What are the advantages of this kind of a biasing?

Professor: Oh advantage I have already told you, it uses 1 resistance less, the if you recall instead of V B B, V B B was replaced by V C C and therefore wherever V B E occurs V B E is much less compared to V C C then V B B. Let's say it's a more stable circuit. Than the previous one okay. And however there is a problem of AC feedback that is AC signal, signal current may flow to through R G into the drain directly for which the solution is that you break R G into 2 parts R G 1 and R G 2 and bypass, by means of a third capacitor. So you don't really save a resistor okay, you don't really save a capacitor also, you have to use this there r 2 more 2 more components. We don't really say it but this is a good enough circuit. (())(0:32:15) reason of the source has to be ground, then this is a solution provided the FET is in enhancement mode MOSFET.

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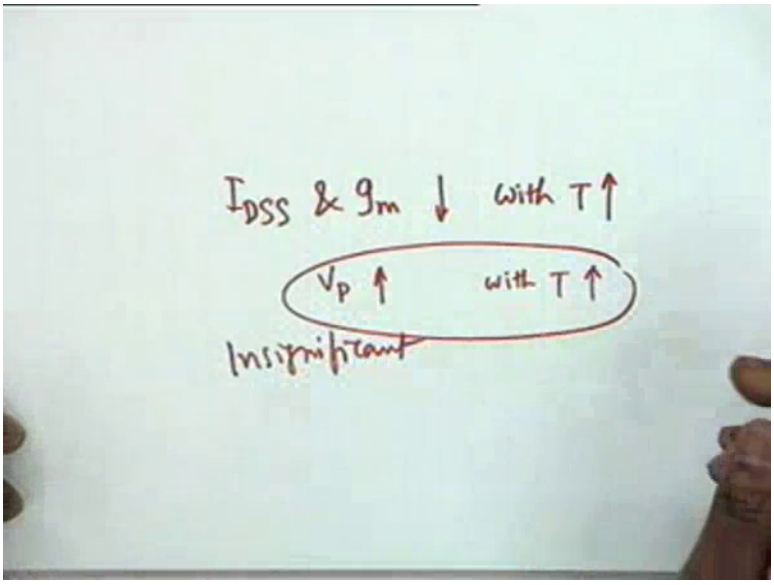

As far as the effect of temperature is concerned I D S S and gm both of them decrease with rise of temperature. Can anyone explain why it is so? With rise of temperature why I D S S and gm decrease?

Student: Because of the resistance.

Professor: Which resistance?

Student: Resistance of the channel.

Professor: It's not the resistance okay, that is a that is a that is a gross explanation but what happens is with temperature increase the mobility decreases because they go on colliding with each other, they acquire more energy they don't know how to dissipate the energy so they fight each other. Okay I heard this term happening with human beings okay.

Student: Sir carriers also increase when temperature increases?

Professor: Carriers you see it's an n-channel and therefore you should drive the device to it's limit as much as you can, as it afford. So that is not, that is marginal.

But the energy of the increased thermal energy it causes carriers to fight each other they can't recombine with anybody. So they fight with each other they are of the same polarity and the mobility is decreased. This is also true that V P the pinch-off voltage increases with temperature increase, pinch-off voltage increases with but this effect is not very significant. It's insignificant, insignificant increase okay.

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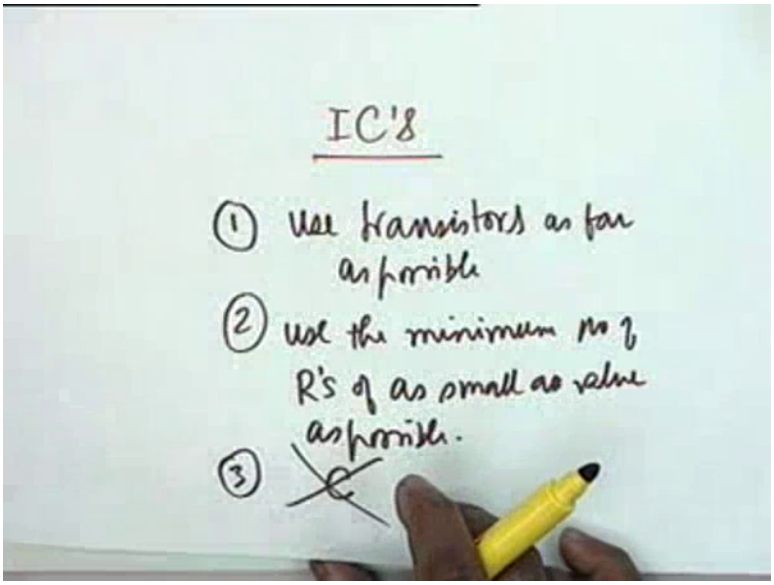

This takes us to have a look at at a completely different type of biasing which is to be used in integrated circuits IC. In integrated circuit, the biasing that we have discussed so far, either BJT or FET cannot be used because in integrated circuits there is a limit on the volume, there is a limit on the area of silicon that can be used. So in integrated circuit, the main guiding principles are in making an integrated circuit or in biasing main guiding principles are that use transistor as

many as possible to replace any other function for example a diode you didn't make a diode separately, you used a transistor connect what?

Student: Base Connector.

Professor: Base collector short that is a the best diode base collector short and the emitter is the other terminal okay, you can make, diode can be make from a transistor in in I think 6 different ways. Of which the best is the one, did you know this or you just guessed?

Student: We know.

Professor: You know it okay.

Alright so whatever the function it is, whether it is diode or a resistance, even a resistance use an FET between the drain and source. Keep the gate open doesn't matter, use this as a resistance doesn't matter you understand what I mean? So use transistors.

Student: Why?

Professor: Because resistors are more costly. Diodes are more costly than transistor.

Student: (())(0:36:15)

Professor: I will tell you I will tell you why.

You see in an integrated circuit, every step of fabrication, diffusion, oxidation, masking every step has to be very precisely controlled. And when you make a transistor let's say 2N222 or whatever the type is, if you want to change it to make a diode it costs a huge lot of money, because the whole process has to be stopped, reconfigured and then carried out, so it costs money in terms of man power in terms of material, in terms of utility of the equipment alright. So one one standardizes one process in a particular setup, let's say Motorola they will only make transistors, they will not make anything else unless they are forced to. And this transistor you can make many end in one chip. In one of the wafers you can make million transistor there is no problem VLSI with appropriate designs.

So use transistor as far as possible. If resistors are to be fabricated then use the minimum number, as few as possible. Minimum number of resistors or as smaller value as possible. Why is this so? The larger the value of resistance the more is area of wafer, area of silicon.

Student: But at the same time the current is also increased and the power dissipation.

Professor: The current we shall current is of our choice. Current is our choice, we will make we will reduce the current. We will reduce the current, you see for amplification the absolute level of current and voltage are not important, as long as you put the Q point in the appropriate operating point. And the dynamism the dynamics of the whole situation is such that the dynamic range is not exceeded, that is we don't go into cut-off half power dissipation or saturation or whatever it is, then you're perfectly safe. So current is in our control and in integrated circuit the one of the guiding principle is use as little current as possible, so that you don't have to provide for heat dissipation.

Heat is a menace, it can cause havoc. So current is of our choice. If the minimum number of R's or as smaller value as possible as far as practicable do not use capacitances because capacitance also are very costly. They use they use a large semi-conductor area, silicon area capacitance is directly proportional to the area. Not only that if you want make a large capacitance the thickness the separation between the two plates has to be made very small. Which means insulation strength of the capacitor will be very small, alright. So do not use capacitance unless you're forced to. If you have to use a capacitance use a MOSFET in a MOSFET there is already a capacitance between the gate and the channel. So use gate to source or gate to drain as a capacitance, instead of a transistor or use a reverse biased junction, a reverse biased junction acts as a capacitor alright.

So this is what I said, use transistor as far as possible. If you have to make a capacitance of the pure kind the parallel plate well then it is going to be costly you try to avoid it as much as practically, if you're forced to then of course there is no choice, alright.

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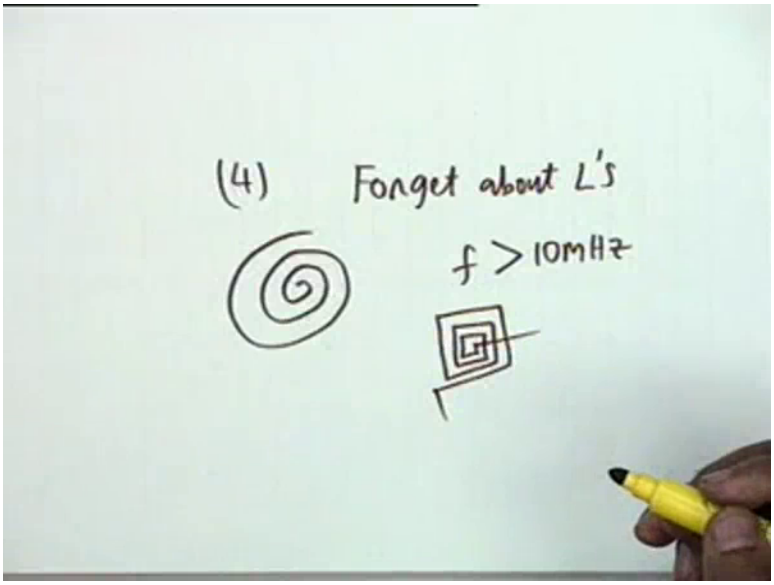

And the fourth guiding principle is Inductors, forget about them. You can't make inductors in integrated circuits, because their basic limitation a fundamental limitation the amount of flux that can be contained in a small volume of dimension microns, the amount of flux that can be contained is very very small. Unless the magnitude permeability or the magnetic field that is causing the flux is of astronomical magnitude naturally you cannot have it in the laboratory. And you cannot have inductors unless you go to frequencies greater than 10 mega-hertz let's say. If the frequency is very high, very small piece of spiral for example will act as an inductor, good inductor, you require very small inductors nano-henry order and you can make it by depositing a conducting spiral for example or there are many other many other geometry, you can make a look like this. And this is one of the terminals, this is the other terminal okay.

But this is at extreme high frequencies, now therefore if we had to be guided by this in integrated circuits we cannot use that self-biased BJT's 4 resistors or FET with so many resistors. We can't make them, so we have to think of something else.

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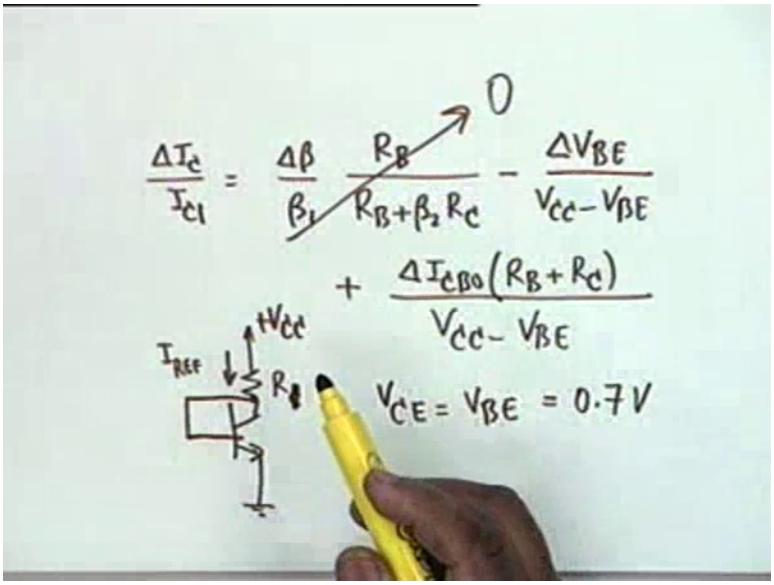

And this is done by what is known as Current Mirrors. In a current mirror not only, you see if you have a if you have a BJT what you have to do is to stabilize I C and V C E. This is the basic problem okay. And if I C is stabilized then V C E is also stabilized because V C E is V C C minus the drop in the collector resistance minus the drop in the emitter resistance. So basically our, our problem is to stabilize I C and what is the stabilization. I C has to be stabilized against variations of beta V B E and I C B O alright. One of the simple things.

In our mirror the guiding the basic principle is that you make I C in a particular transistor, independent of the parameters of that transistor that is you make a reflected, I am using a shakesperean term “reflected glory” what you do is I C is controlled by another circuit okay another circuit and therefore I C you make independent of the particular transistor in which it is flowing this is why it's called a mirror. Mirror is what you see here is a reflection as I said reflected glory, is a reflection of what happens in another circuit alright. Let's see how this is performed. This is the significance of the term mirror nothing else. It's a reflection pardon me, purpose is to stabilize I C. If I C is independent of the parameters of this transistor naturally it's stabilize.

Student: But then it will depend on the stability of…

Professor: Okay, that we will see, that we will see.

We will make that transistor under very controlled conditions. So one transistor one spot in the circuit, we will control stable collector current so many other transistors okay. Let's see how it is done. We recall this circuit for BJT biasing. We have an R C then the emitter goes to ground and there is a base resistance R B you recall this biasing? In this biasing in this biasing where there is a feedback that R B is split and all that is a different story, that only only affects the AC signal part not the DC okay. Now in this circuit I had told you that delta I C by I C 1 that is the percentage change in the collector current is given by delta beta by beta 1 let's recollect R B divided by R B plus beta 2 instead of R E we shall have R C that's the only change. R E has changed to R C and V B B is changed to V C C. Then due to V B E change it is delta V B E divided by V C C minus V B E. Plus delta I C B O do not forget this this negative sign. Delta I C B O, R B plus instead of R E it is R C divided by V C C minus V B E alright.

You also recall in the specific calculation that you have made that this beta variations accounted for the major change I C, it was 9.2 in the particular example that you took. This was of the order of 4.6 or something about half and this is of the order of 0.66 percent. So major variation occurs due to beta, and if I can make that 0 then obviously I would have improved matters. And making it 0 simply means make R B equal to 0. So if I use this circuit R C let us see what happens. This goes to ground and instead of a resistance we simply this use okay. Then what is V C E? Well this goes to 0 alright. And therefore the I C is stabilized to a degree greater than when R B was there alright. But what happens to V C E now?

For this transistor isn't it the same as V B E? V C E is the same as V B E, is it a diode basically?

Student: Yes

It's basically a diode, a transistor is being operated as a diode. Now V B E in active region as you know is about 0.7 volt. Is the transistor then in the active region? Well it is greater than 0.2 so it is very close to saturation but in the active region. We will not require this transistor to amplify. What we will do is, we'll use this current as the reference current. We will use this current as the reference current so, we shall call this uhh we shall call we shall change the nomenclature a little bit. We shall call this as the reference current and we shall call this resistance as R 1. Then you see I ref is simply V C C minus V B E divided by R 1 correct? I ref is V C C minus V B E divided by R 1 agreed?

Now this is a reference current, how can (())(0:48:26) change, why should this current change? The current can change if there is change in V B E obviously. The current can also change if there is change in I C B O. But as you know the changes in V B E and I C B O are much less as compared to the change in beta and therefore if this transistor goes bad and you replace it by another transistor nothing happens, because it has been made independent of beta. This is the basic point alright. Now this transistor as a reference is used to control the current collector current of another transistor and the connections are made like this.

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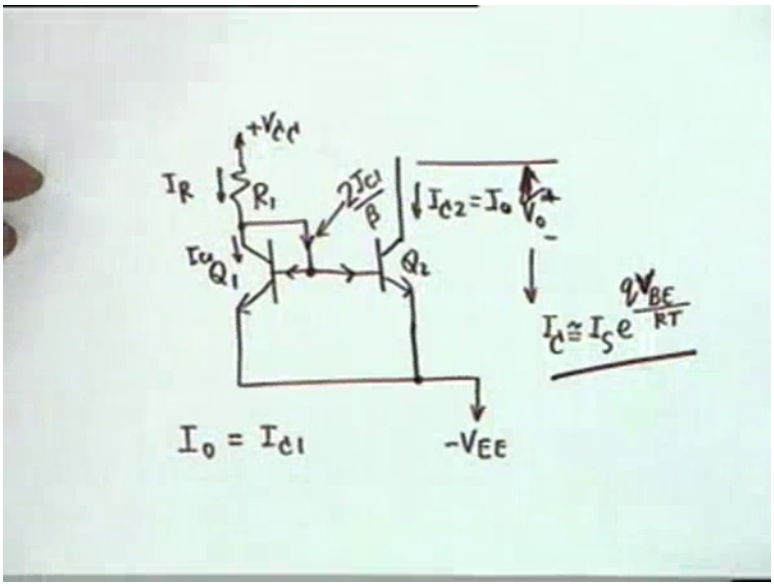

This is plus V C C, there is a resistance R 1. Then you have you have this connection, call this transistor as Q 1 the emitter goes here. This base is then connected to another transistor the current of which has to be controlled or stabilized the operating point of which has to be stabilized, let's call this I C 2, let's call it output current. And let's call this voltage as V 0 okay, this voltage has V 0 I am sorry. That is the V C E of Q 2, this may be connected to a load, we're not showing that part of the circuit we're showing only the DC collector current. Now this goes to the same point the emitters are tied together the bases are tied together okay.

And this goes to, it will go to ground but in integrated circuits usually integrated circuits are operated with a plus minus supply which helps in stabilizing operating point and in getting many other kinds of function, then is possible with only 1 supply. So it goes to minus V E E, this goes to a negative supply. Usual supplies are let's say plus minus 12, V C C would be plus 12 and V E

E would be minus 12. The ground is the middle point of this supply okay right. Now this is a typical current mirror arrangement. Why is it called a current mirror? Because as we shall show I 0 is approximately equal to I R or I reference. Reference I don't want to write I f every time I'll simply say I R okay.

Now you know that the collector current of a transistor, collector current of a transistor is approximately equal to the emitter current, actually it is alpha times I E plus I C B O okay alpha times I E plus I C B O. I C B O can be ignore and therefore it is alpha times I E and alpha is approximately 1 and transistor the collector current is approximately equal to emitter current and emitter current is a diode current and therefore it is of the form I S particularly when it is forward biased. It is I S exponential Q V B E, let's use capital divided by K T agreed? Now therefore the collector current of a transistor depends basically on the base to emitter voltage and since the 2 base to emitter voltages of Q 1 and Q 2 are identical, they are identical the collector currents I C 2 and I C 1 should be identical alright?

So the first thing that you notice is that the output current that we want I 0 is equal to I C 1 alright. How is I C 1 related to I R? As you see I R equal to I C 1 then there is a base current here there is a base current here the 2 base currents will be identical because V B E is the same alright and this these 2 base current must come from here, therefore this is equal to twice I B 1 plus I B 2 or twice I B which is I C divided by beta, so twice I C 1 divided by beta.

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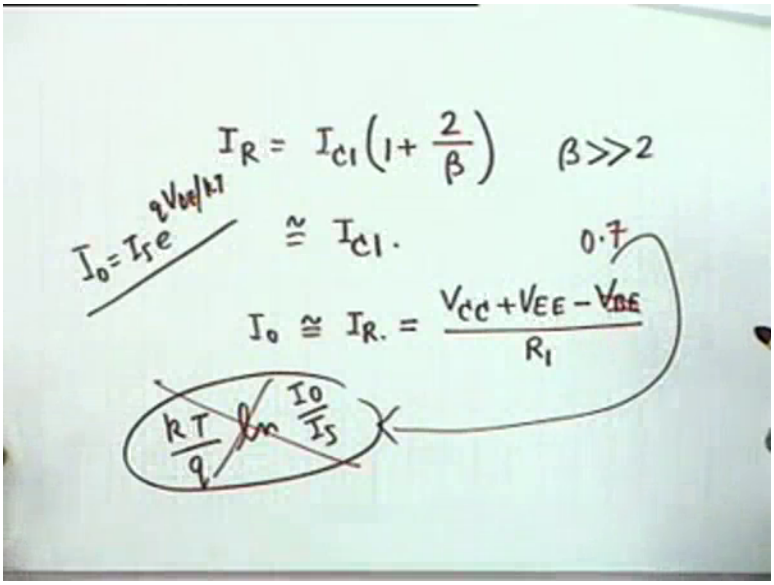

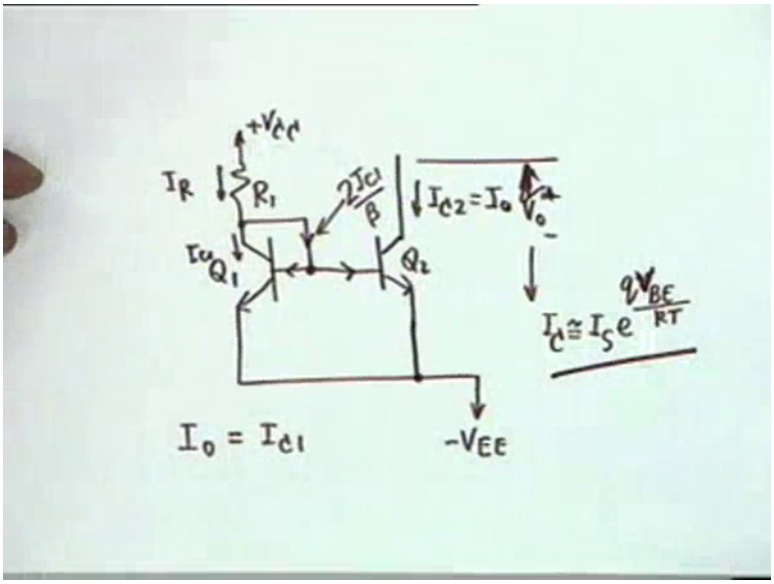

Therefore my relationship becomes I C 1, 1 plus 2 by beta and if beta is much greater than 2 which is usually the picture. If beta is 100 it is 1 by 50 0.02, 2 percent change then I R is approximately equal to I C 1.

Student: Sir, what is I C 1?

Professor: I C 1 is the collector current of the transistor Q1, this is I C 1 collector current of Q 1.

Which means that the output current I 0 is approximately equal to I R, the output current is approximately equal to I R.

Student: Sir, how did we get the first equation?

Professor: This one? Okay, I will explain.

First take I C is I C 1 that is the current through the collector plus this current, by KCL this current must be equal to the base current of Q 1 plus the base current of Q 2 and these two current must be identical. So twice I B and I B is I C over beta, is that point clear?

Student: Yes

Professor: Okay.

And therefore I 0 equal to I R and what is I R now? What is the reference current here? It is V C C minus minus V E E. So it will be V C C plus V E E minus V B E divided by R 1 okay. So this is V C C plus V E E minus V B E divided by R 1. Now V B E strictly should be replaced by K T by q log of why? Because this is a collector current and it is I S it will be power Q V B E by K T. So it should replaced by L N, I 0 divided by I S, isn't it right?

Student: Yes

Student: Sir what should be replaced?

Professor: V B E, because I 0 equal to I S it will be power 2 V B E by K T, therefore V B E should be replaced by this quantity. If I do that then what kind of equation do I get? I get a transcendental equation. And I don't want to solve the transcendental equation. So what is the way out? Way out is engineer, engineering common sense, common sense it is said is the strongest tool of an engineer and here you see V B E would be a small quantity compared to V C C plus V E E in integrated circuits invariably there is a positive supply and a negative supply therefore this would be of the order of let's say 24 and V B E if you know in the active, we want the transistors to be in the active region. So active region V B E is approximately 0.7. Therefore this is the negligible quantity and instead of solving a transcendental equation I replace this by 0.7 and I did a fairly good fairly good work in relationship design relationship for a current mirror.

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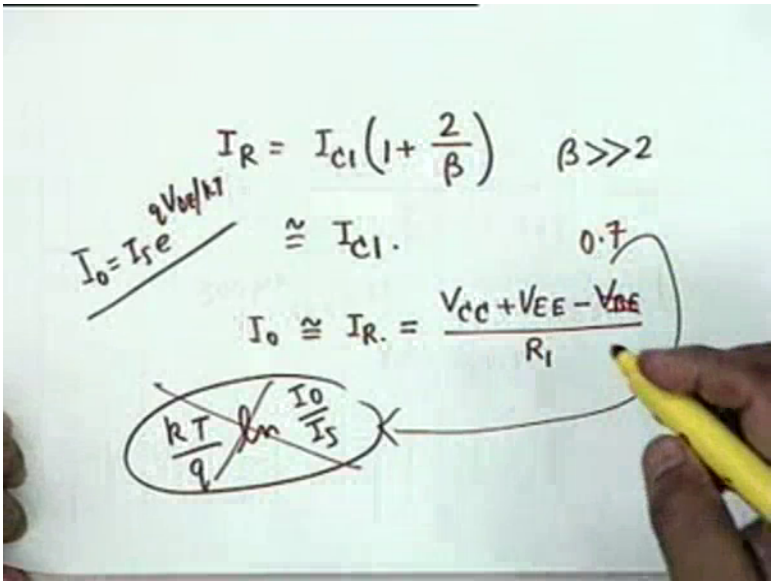

Therefore the resistance R 1 that I need is V C C plus V E E minus 0.7 divided by whatever current I need okay. I C 2 which is approximately equal to I ref alright? Which is approximately equal to I ref. For example if I want, let's say 500 micro-ampere and V C C and V E E both are 15 volt let's say plus minus 15. Then R 1 comes out as 30 minus 0.7 which is 29.3 divided by 500 micro ampere. And this comes out as 58.6K, alas this is a large value.

Student: Sir?

Professor: Yes

Student: Sir in the expression for I R, we're ignoring 2 by beta, but if we're supplying many different circuits, you said you are supplying (())(0:58:09) then you cannot ignore, in that case.

Professor: Wonderful.

Then we will have to have super-betas. If I want to supply 10 of the circuit then obviously if I want to supply 10 transistors from the reference current. If I want to want to supply the base current of 10 transistor from the reference current then obviously this 2 shall be replaced by 10 or 11?

Student: 11

11 why 11? Because the reference transistor also supplies a base current. So it would be 11 therefore beta must be much larger compared to 11. And as I said, if I use a Darlington that's another thing that is used in ICs invariably instead of 1 transistor we use 2 transistor. Let me show you this.

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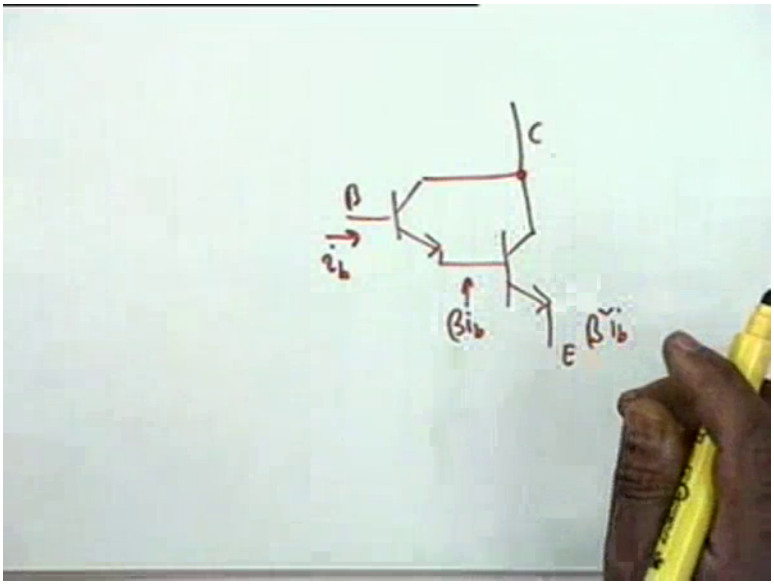

What we do actually is this, the collectors are brought together and this is the emitter, this is the base, this is the collector. There is a composite connection, so if I supply an I B here signal current, this current is approximately beta I B and this current would be approximately beta square I B. So if I have a beta of 50 I can get a beta of 2500 without any problem. Your question is quite valid, if my current level has to supply large number of transistor then the current mirror must be made of a Darlington.