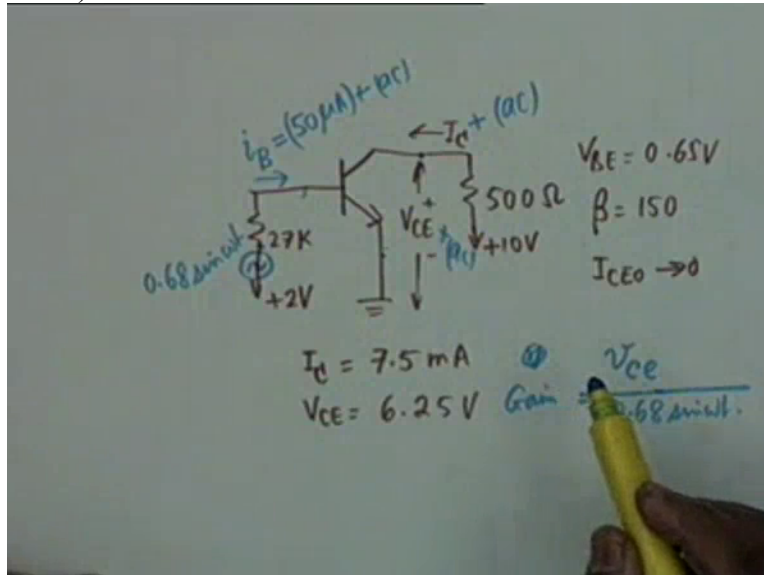


Analog Electronic Circuits
Prof. S. C. Dutta Roy
Department of Electrical Engineering
Indian Institute of Technology Delhi
Lecture No 03

Before we take FETs let us recall an example which we had taken last time and we didn't quite finish.

(Refer Time Slide: 1:02)



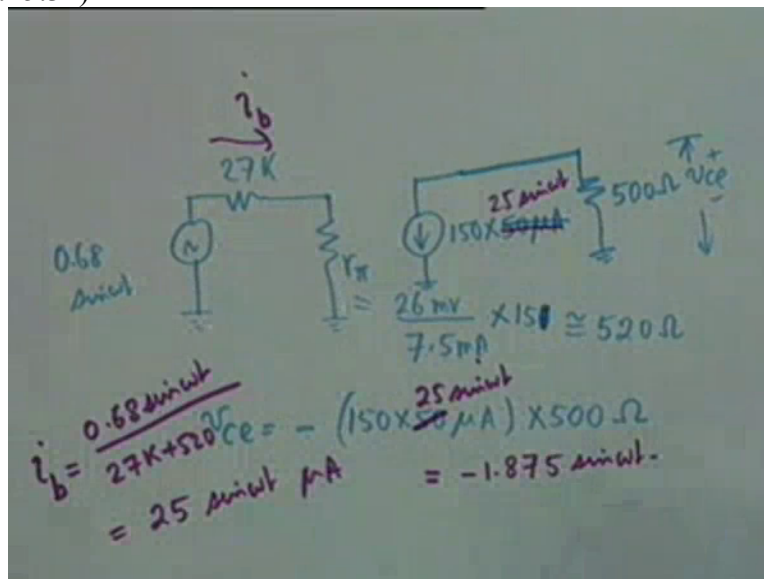
It was BJT with a 27K resistor here and a 2V source, DC source and this was grounded. There was a 500 ohm collector resistance and this went to a 10 volt source. Problem was to find out I_C and V_{CE} the DC values. It was given that V_{BE} is equal to 0.65 volt Beta was given as 150 and I_{CEO} tends to 0 these were the given quantities and we found out that I_C is equal to 7.5 milli-ampere and V_{CE} is equal to 6.25 volt, this is what we found. The next part of the question says suppose in series with this 2 volt source suppose there was a small AC voltage source of value $0.68 \sin \omega t$. Suppose there was a small AC voltage. Why do I say small? Because compared to 2 this is small 0.68. Now you notice that the maxima and minima of the voltage that is applied to the end of 27k is 2.68 and 1.32 whereas this voltage is required to be 0.65 alright. So it is within limits.

Suppose AC source was such where the voltage here fell below 0.65 then there is a possibility that the transistor could be led to cut-off alright okay. Now what you want to find out is, if this is so then obviously V_{BE} I am sorry. Obviously between, let's look at the collector current I am sorry the base current. Obviously i_B would be the DC, what did you find the DC value to be

55 micro-amperes, 50 micro-amperes plus an AC quantity which would be which is required to be small compared to the DC value. In order that the emitter base junction is in the active region okay. We will find this out.

Now if this is so, if the base current has an AC component naturally the collector current shall also have an AC component now and the voltage between the collector and emitter shall also have an AC component. We want to find out this AC component, which obviously we shall denote by V_{CE} and find out V_{CE} divided by $0.68 \sin \omega t$. That is the AC component of voltage developed across the collector and emitter divided by the signal voltage that you have applied. This is the signal voltage $0.68 \sin \omega t$. And this shall be the gain of the amplifier. That is given an AC voltage $0.68 \sin \omega t$ we get an AC voltage across the collector and emitter which will also be of the form $K \sin \omega t$ but this K will be greater than 0.68 and therefore there shall be a gain.

(Refer Time Slide: 5:32)



In order to find out what this gain is, let look at the equivalent circuit. AC equivalent circuit. In terms of AC what you have is $0.68 \sin \omega t$ then ignore the DC value, you have 27k and from base to emitter the DC voltage is 0.65 volt that doesn't change. What you have is the resistance r_{π} which is equal to 26 milli-volt divided by I_C or I_E , I_E okay how much is I_E ? I_E is approximately equal to I_C right and therefore we take 7.5 milli-ampere, then this must be multiplied by beta which is 150 and this is approximately equal to 520 ohms. Actually it should be beta plus 1 to be exact, it should be 151. If you have divided by the base current that would

have been incorrect. No Beta plus 1 factor is needed by since you have divided by the emitter current which is the same as collector current, this is 520 ohms.

Okay and then we have the AC equivalent circuit shall have simply a current generator of beta times i_B beta is 150 and i_B is 50 micro-ampere, therefore this is what will be the current generator. Beta i_B then $I_{C E O}$ is not required. In fact it is negligible but it is not required in the AC equivalent circuit and then we have R_C that is the collector resistance which is 500 ohms and this is the voltage $V_{C E}$. We have thrown out all the VC quantities the batteries and their associated paraphernalia okay. So what is $V_{C E}$ then? $V_{C E}$ is equal to this current generator flows like this therefore it will minus the current 150 multiplied by 50 micro-ampere multiplied by 500 ohms.

Student: Sir I have a question.

Professor: Yes

We have not found out I_B we have to find out I_B . I_B is not 50 micro amperes no this is the DC value. How come you didn't object it? This is the DC value this should not correct; I will answer your question little later. Let me correct this; do not agree with whatever I say. I must put here the AC value. What is the AC value? i_b small i subscript small b is equal to $0.68 \sin \omega t$ divided by $27k + 520 \text{ ohm}$ correct. So you convert this 27 times 10 to the 3, add to 520 and the result is $25 \sin \omega t$ so many micro-amps. So this is $25 \sin \omega t$. This is $25 \sin \omega t$, is the point clear where we made a mistake. We cannot use 50 micro that's a DC value, we must find what the AC i_b is alright. Now if I do that then $V_{C E}$ comes as minus $1.875 \sin \omega t$.

(Refer Time Slide: 9:56)

$$\text{Voltage Gain} = - \frac{1.875}{0.68} = -2.75$$

$$\text{Current gain} = 150$$

$$I_o = \frac{100 \text{ V}}{7.5 \text{ mA}} > 12 \text{ K}$$

$$i_b = \frac{0.68 \mu\text{A}}{27\text{K} + 520 \Omega} = 25 \mu\text{A}$$

$$v_o = -(150 \times 25 \mu\text{A}) \times 500 \Omega = -1.875 \mu\text{A}$$

You see it is of the same form as the input signal voltage. It is $0.68 \sin \omega t$ this is minus $0.1875 \sin \omega t$. So the gain is the ratio of the 2 $\sin \omega t$ $\sin \omega t$ cancel and we get gain as minus 1.875 divide by 0.68 which is equal to minus 2.75. This is the voltage gain okay, that is output signal component divided by the input signal component alright voltage gain. What is the current gain? That exactly equal to 150 agreed? This is equal to beta, output signal current divided by input signal current okay. Now you notice that there is negative sign here, so the gain. Okay let me go back here.

The output voltage signal component has found out to be minus $1.875 \sin \omega t$ apparently there is no phase change because this is $\sin \omega t$ and the input is also $\sin \omega t$ that you must recall, you must remember there is a negative sign here which means phase change of 180

degrees. In general it may be 180 degree or 180 plus some other component ϕ . As we shall see later when we take the transistor capacitance into consideration then there is a phase change which is different from 180. Therefore there is a phase change here of 180 degree. Now I can take your question yes.

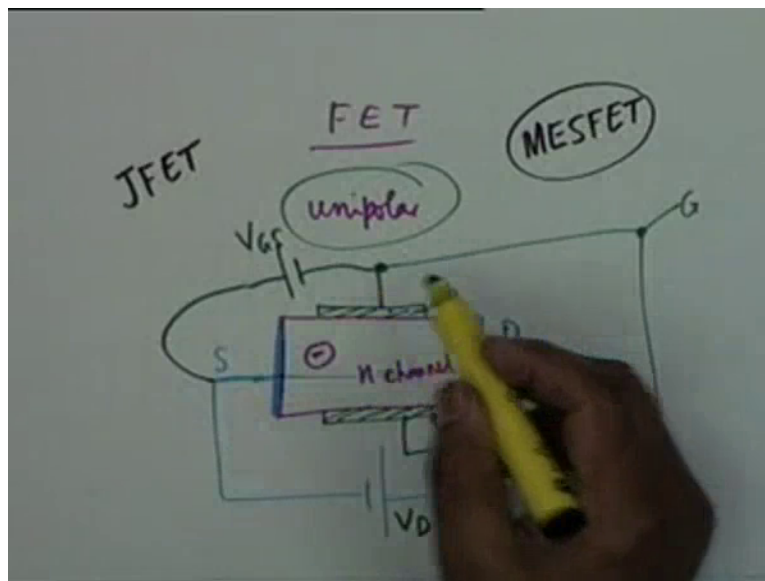
Student: Sir in the small signal model which we have considered in this problem in the output part you have not considered any earlier resistance.

Professor: In the output part we have not considered any, yes okay.

Actually what we should have done is, from here we should have introduced a resistance r_0 but let us see what r_0 is in this case. Let us say that the Early voltage is 100 and Early voltage lie between 50 30 and 150. This is the range, usual range for silicon transistors. This divided by the collect current which is 7.5 milli-ampere. So how much is this? This is k , it is of the order of more than 12k isn't it right? And 12k parallel with 500 ohm is approximately is 500 ohm. That's why we have ignored. r_0 is usually very large compared to r_c but in situations where the load resistance is very large you do have to consider r_0 okay alright.

This leads us to a consideration of FET; more problems in BJT shall be worked out day after tomorrow, Thursday class and in the tutorial class. From the tutorial sheet that I have supplied. Some of the problems will be done in the tutorial class and the rest will be done the tougher ones will be done here by me okay.

(Refer Time Slide: 13:18)



We now go to a consideration of FET. I am told that not much of FET has been done in 110 so we would like to look at FET a little more deeply to be able to understand its circuit models and its performance as an amplifier. As you know F stands for Field E for Effect and T for Transistor this is it Field Effect Transistor. Which means that the basic conduction mechanism in FET should be Field oriented or field induced, that is you create an electric field you create an electric field and you allow the carriers to be drawn away by the field. Or carriers to be accelerated by the field and go to a collector.

Now in contrast to a bipolar junction transistor where conduction occurs basically due to diffusion, due to the flood of electrons coming from the n region and crossing over to the collector region collector n region. So field effect transistor is basic mechanism of conduction is different. Historically field effect transistor has conceived much earlier than BJT but because of fabrication difficulties a commercial FET have to wait till about the middle of 60s 1964-65 commercial FETs came in the market. Whereas the bipolar junction transistor have flooded the market right in 1949 or 1950 okay. 1947 of course was the year 1948 was the year that transistor was first disclosed. Within a year Bell Telephone labs themselves which were responsible for the invention of the transistor Bardeen, Brattain, and Shockley. 1949 itself commercial BJTs came in the market. They were not very good but gradually they were improved. Whereas FETs had to wait for a long time for improvement in technology.

As I said besides the mechanism of conduction there is also a difference that FETs are unipolar in contrast to BJTs which bipolar. Bipolar's because there are 2 kinds of carriers electrons and holes on the other hand in an FET the carrier of current is either electrons or holes, not both. The basic the basic phenomenon that occurs in FET is, suppose you have an n type material a very simple a simple way of representing and FET. Suppose you have an n type material okay, and you have a metallic collection here and metallic collection here. I am taking a cross section okay. Now obviously if connect a battery between these two terminals the current will flow, the n type material will act simply as an ohmic resistance. The electrons which are available will simply drift towards the positive potential. Suppose you connect a connect a positive potential like this, then electrons will be drifted towards this okay, conventionally we say this is the source. Because electrons go (())(16:50) the battery has to supply electrons.

So electrons this terminal is the source and this terminal is the terminal at which electrons are drained away. The terminology is slightly different we could have called it a collector but conventionally it is called a Drain. Source and Drain, if this is the situation then it is nothing different from an ordinary carbon resistor for example. Across a resistor it's a semi-conductor material so the conductivity is in between that of a metal and an insulator. Besides that there is no other difference it's and ohmic resistance. Now what is done is a if this is this is the way, then this is called a channel. That is a channel through which water flow canal through which water flows, channel through which carriers flow so it's an n channel.

The conduction of the n-channel is due to due to electrons only, so it is a unipolar device. This current is controlled by a field. By a field applied between this terminal, let me use some other color. Between let say some mechanism which I shall I shall come a little later. This terminal, while these 2 are connected together. I am showing a cross-section so from the top as well as from the bottom; there is a layer which I shall say what the layer is a little later. This is called a Gate. By application of a voltage between the gate, between this terminal and this source. By application of a source of a voltage between the gate and the source the width of the channel is controlled or the flow of the electrons in the channel is controlled. And this is how the third electrode comes.

If you compare with a BJT gate is comparable to the base the source is comparable to the emitter and D drain is comparable to the collector. Now how this is done differs from FET to FET. There are various types of FETs and we shall discuss a family tree in a minute. But let me tell you how this is done. Suppose this material is p suppose there is a p type material deposited on the n channel okay and suppose there is a battery connected like this, then obviously the source which is connected to an n-type material and a gate which is connected to a p type material obviously there is a reverse biased that is created between the gate and the source and because this is resisted the reverse biased will be 0 here and will increase to a maximum at the gate. Is that correct?

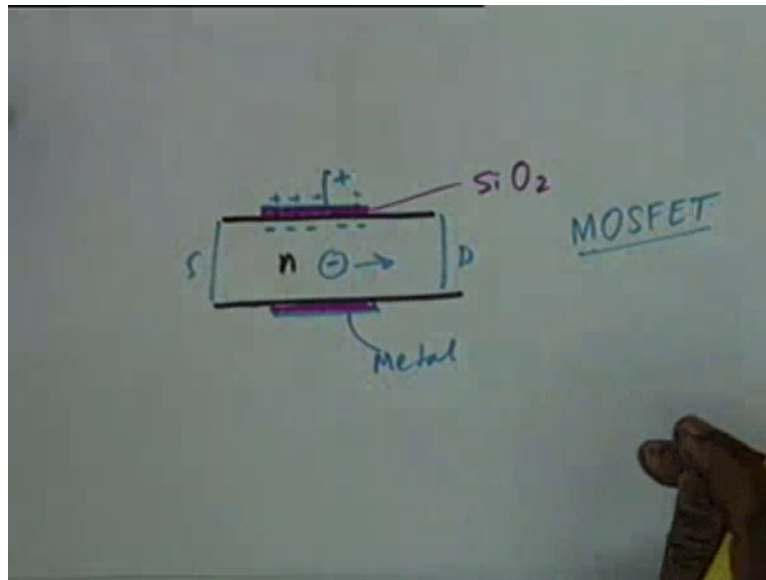
In this channel the reverse biased will increase like this because it's a resistive material. This voltage is dropped from here to here and therefore there will be a potential gradient okay. In other words what will happen is that the depletion region depletion region in the n, there will be created a depletion region and this is a pn junction pn junction reverse biased so there is a

depletion region. The depletion region width shall vary along the channel and will be controlled by this voltage V_{GS} alright? This is the control by appropriately controlling V_{GS} and by appropriately V_{DS} one can get amplification in a field effect transistor. The phenomenon is exactly the same. Exactly of the same qualitative nature as that occurs in a BJT.

That is the gate controls the flow of current in a channel. The current is carried by a single type of carrier that is why it is called a unipolar device in contrast with bipolar BJT. Let's look at the, before we go to the family tree, let's also realize that instead of a pn junction I could have a metal deposit here instead of a p type material here I could have a metal. You know there are metal rectifiers, metal and semiconductors copper and copper oxide for example or selenium rectifiers. You heard of selenium rectifiers? Metals in contact with semiconductors can give rise to rectification because there is a difference in work function, or the contact potential, basically it's a contact potential.

So instead of a semi-conductor material one could have a metal semi-conductor gate and such devices are known as Metal-semiconductor Field-Effect Transistor. This is called a Junction Field-Effect Transistor or JFET. There is nothing sacred about the type of channel. You could have a p channel also. Then the biasing would have been different, agreed? So a JFET could be either p-channel or n-channel. Similarly a MESFET could be either p-channel or n-channel. But MESFET we take out of consideration, they are applied they are not applicable; they are not favored at lower frequencies. They are very useful devices at microwaves so we will not consider them. As I said JFET could be either p-channel or n-channel. But however n-channel is preferred because of the higher mobility on electrons as compared to holes. So we will mainly just like BJT we are taking npn as the basic material. It's not that pnp's are not used. For example in a complementary symmetry you require and npn and also a pnp okay. Now in JFET's n-channel devices are preferred because of the higher mobility of electrons.

(Refer Time Slide: 23:52)

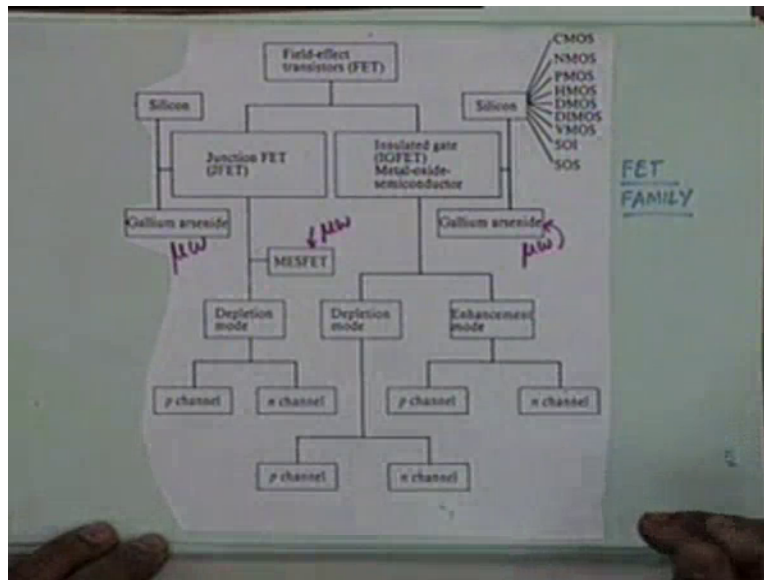


The third way that the electron flow in the channel can be controlled is to have a capacitor that is you have a, let me draw it separately. You have an n channel and then what we do is, you deposit an oxide material here. And this oxide is silicon dioxide because the basic material is silicon. So you simply expose to oxygen then silicon dioxide is deposited. Silicon dioxide is an insulator. And then you deposit a layer of metal here okay. So this is metal, this is silicon dioxide and then you have the semi-conductor n alright. So what you have is metal oxide semi-conductor. This is the architecture of the FET. And it is therefore called MOSFET metal-oxide-semiconductor field-effect transistor. This is another way that the channel current can be controlled.

Obviously the channel current is been controlled through capacitive effect. If you apply a positive potential here for example what will happen no current can flow through the gate because there is an insulator in between but electrons will accumulate here, isn't it right? Electrons will come over here because of the capacitive effect. This is positively charged and therefore this must be negatively charged. And by controlling this voltage, the accumulation of electrons here can be controlled. Now if electrons are bound here obviously less number of electrons will be available for conduction alright. On the other hand if this is negatively charged then holes will come here and therefore more electrons will be available for conduction. This is the way that the electrons current in the n channel can be controlled. There is a source here, there is a drain here and the current the electron current can be controlled.

Now if electrons are bound here obviously less number of electrons will be available for conduction on the other hand if this is negatively charged then holes will come here and therefore more electrons will be available for conduction. This is the way that the electrons current in the n channel can be controlled. There is a source here, there is a drain here and the current the electron current can be controlled. So the other type of the third type of constructional feature of an FET is through Metal Oxide Semi-conductor.

(Refer Time Slide: 26:22)



Now with this brief introduction let's have a look at the at the family tree of FET, this is available in most of the text books so you don't have to copy this. Now started from field-effect transistor, field-effect transistor can be either junction JFET or Insulated Gate or Metal Oxide Semiconductor. Sometimes we call MOSFET also is IGFET. This was the earlier term, but currently we use MOS they are identical. Insulated Gate FET okay. These are the two basic types. Now Junction FETs can be the basic material can be either silicon or gallium arsenide, gallium arsenide is mostly used for microwaves, therefore we shall not consider this in this class. We will consider FETs made of silicon only.

Okay and as I said junction could be created either by semiconductor pn junction or by metal semiconductor junction. And this also is of major applicability in microwaves so we do not consider this now junction FET basically occur in depletion mode because a pn junction is reverse biased and there is depletion created. As you will see MOSFET can work either in

depletion or in enhancement mode. That means it can enhance, it can create more electrons and it can enhance the the current flow. Now as I said Junction FET work on a depletion mode and there could be either p channel or n channel. On the other hand, MOS can again be made of silicon or gallium arsenide. Gallium Arsenide once again is of applicability in microwaves.

In silicon there are various types of FETs these are some of the sample. For example CMOS for example NMOS is N Channel MOS. PMOS is P channel MOS, there are many other nomenclature. CMOS stands for complementary MOS. Some of these you will get to know in details in the digital integrated circuits. For example HMOS is High Performance Metal Oxide Semiconductor, DMOS is Double Diffused and so on and so forth. Now metal oxide semiconductor as I said can work either in depletion mode or enhancement mode. And contrast to junction FET, junction FETs work only in depletion mode okay. And in each mode it can either be a p channel or n channel. This is the tree of FET. One can ask at this point why FETs if BJTs can do all the jobs then why field effect transistors.

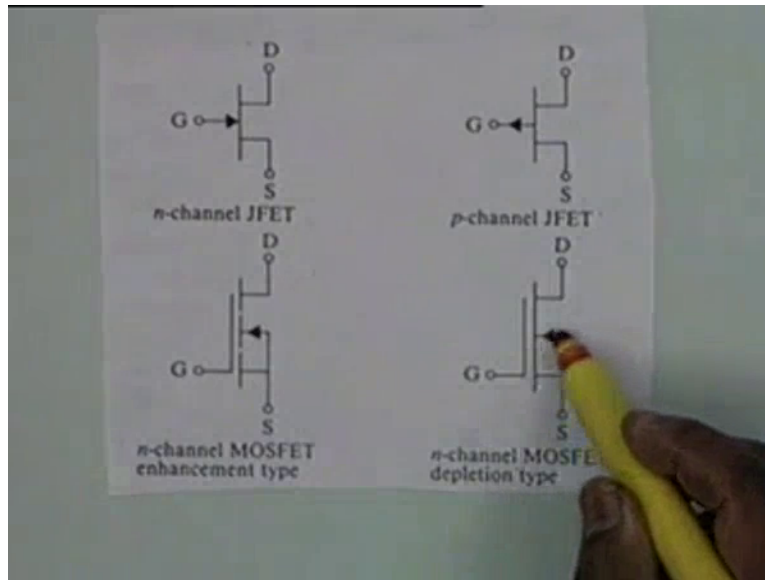
Student: Speed.

No speed is not the consideration. Actually speed may be less because of capacitance, you see the metal oxide you're introducing a capacitance between the gate and the source, gate and the drain. There is a capacitance and capacitance usually reduce speed.

Student: Size.

The size that is correct. You see the packing density of MOS devices is much higher than BJTs and the trend is for smaller and smaller integrated circuits. And therefore MOS has become very popular. Most of the chips that are available unless speed is a consideration are made of MOS. On the other hand if speed is a consideration BJTs have to be used. Sometimes one makes hybrid technology that is BJT as well as MOS on the same device and these are called BIMOS Circuits. BIMOS means Bipolar Junction Transistor and MOS Transistor a combination so they are called BIMOS.

(Refer Time Slide: 30:21)



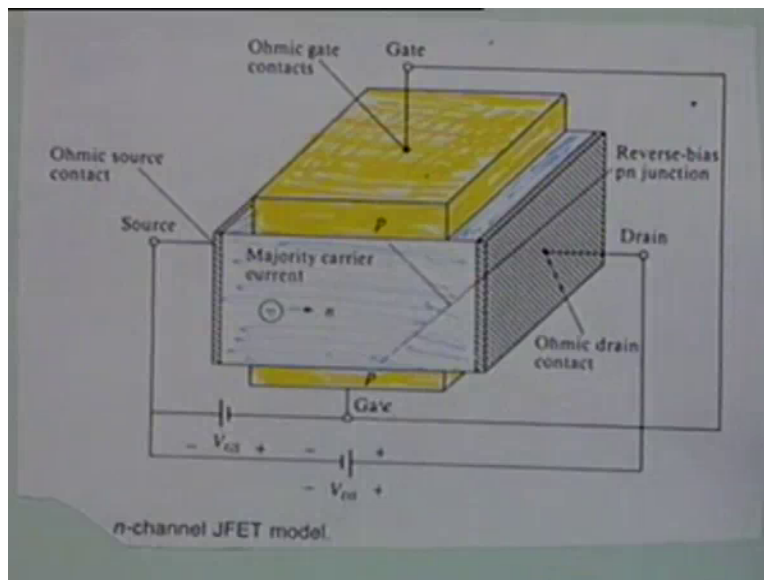
Okay now the symbol that is used for FET is like this. The symbol that is used is for an n channel FET we indicate this, note the direction of the arrow, the gate points inside the gate points towards and there is D and S there are two. The source and the drain they are mostly interchangeable okay. The source and the drain there is nothing to choose between them. On the other hand in a bipolar junction transistor you know the emitter region is more heavily doped than the collector region. The collector region is much larger area because it has to dissipate heat. In a junction field effect transistor or MOS field effect transistor also it is possible to have a drain part different from the source part but usually they are interchangeable. They are not interchangeable in BJT, in a BJT the performance degrades considerably if the collector and emitter are interchanged. Whereas it doesn't happen so much in an FET for a p channel the arrow it points out.

Now for an MOS FET in order to distinguish between the junction and MOS 1 extra terminal is introduced. You can see for enhance type there is a break here. The gate is similar the arrow is here, the significance of these symbols would be clear when you understand or when you go through the physics of MOS devices in a later electric course. So an n channel there is no break it is simply and arrow like this. But let me tell you as far as circuits are concerned amplifiers and other linear analog linear analog circuits, it doesn't matter what the FET is. Whether it is junction or an MOS FET the circuit model is the same circuit model is the same. One difference that you should observe you should immediately conclude about between BJT and FET is that the input

impedance in a bipolar junction transistor is very small because the input is forward biased junction. A forward biased offers very little resistance. That's why R_{pie} is at the most of the order of a K.

On the other hand here the input is between gate and source and the gate and source is a reverse biased junction or a metal oxide semiconductor configuration. And therefore the input impedance should be very high, is that clear. So an field effect transistor is basically if input impedance is very high then what do you apply? You apply voltage source, so it is voltage controlled. FETs said to be voltage controlled device whereas a BJT is a current controlled device. Although we will get voltage amplification and current amplification from both, but basic mechanism is that FET is a voltage controlled device and BJT is a current controlled device.

(Refer Time Slide: 33:48)



Here is a color picture of simplified FET configuration. I have shown a junction the coloring is mine the Xeroxing was in black and white. This is schematic diagram it is not the actual diagram of an FET but to understand what happens in an FET we briefly look into physics of FET, briefly and qualitatively okay. This is the n type box this whole box is an n type semiconductor. The box which I have shaded with grey light grey okay. And it contains majority carriers majority carriers are electrons. This an n type material majority carriers are electrons. On two sides of this box this side and this side there are metal deposition. So this is ohmic contact this is also an ohmic

contact. The left side conventionally is called the source the right side is conventionally is the drain okay.

Between the source and the drain as you can see there is a voltage V_{DS} positive here and negative here. So that electrons are attracted towards the drain. Actually the actual drain current flows in this direction correct. From the battery positive it goes in this direction the electrons come and are drained away drained away to the positive terminal of the battery okay. The control is created by the gate which is through deposition of a p type material on this side and this side and these two are connected together okay. These two, there is a metal contact here,

Ohmic gate contact there is a gate contact here. These two are connected and between the gate and the source there is a reverse biased, you see V_{GS} the negative is connected to p and the positive is connected to the n type material. So it is reverse biased.

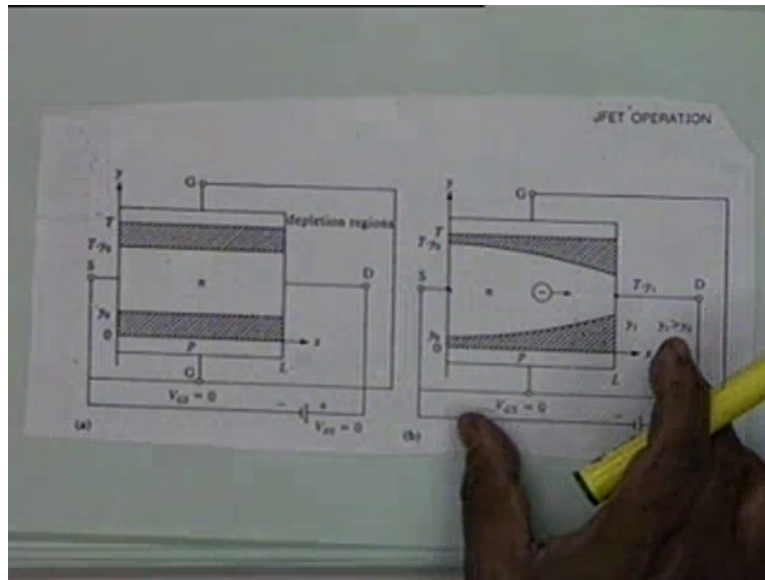
Professor: Yes.

Student: What is the approximate size?

Professor: What is the approximate size? Micron. A few 10s of micron. It's very small.

And the tendency is to go lower and lower dimension okay, as small as possible. Now therefore this junction p and n this is reverse biased, this is also reverse biased. Now let see let see what happens through a cross-sectional diagram. Is there any question on this, the geometry? It's a fairly simple geometry. And this is why it was conceived much earlier than BJT. Actually Shockley first hit upon FET but he couldn't make it and therefore it had to wait for many years.

(Refer Time Slide: 36:43)



Now I have shown here a cross-section of this box with V_{GS} equal to 0. And V_{DS} also equal to 0 no voltage is applied. Let us see what happens. This junction pn junction as you know we will develop a depletion region, the electrons will cross to the p type material and holes will cross to the n type material and they will create a static space charge a charge separation. So this is the depletion region. There will be a region at the metallurgical junction where there are no carriers. The carriers move over to the other side and create a vacant land a no man's land called the space called a depletion region. Depletion region is cross hatched here and its width is y_0 okay. And this width is same throughout there is no bias okay. Because V_{GS} is 0 and V_{DS} is equal to 0.

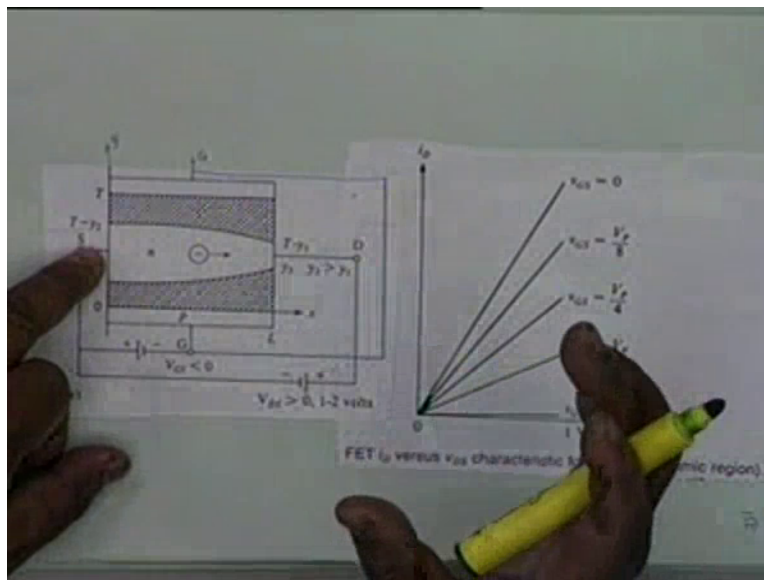
Now suppose, suppose V_{GS} is retained at 0 but V_{DS} is increased to a few volts a small voltage is applied between the source and the drain with this polarity. Then what will happen is, the reverse bias increases from source to drain it is reverse biased you understand this because the n type material is positive and the p type material is at 0 right. So the relative voltage is negative in the pn junction. And therefore this is reverse biased. Reverse biased increases as you go along the channel and therefore the depletion region becomes modulated like this, depletion region becomes curved like this, is that clear. The depletion is highest here because the reverse biased is highest here and it is the smallest here, agreed? It becomes modulated like this.

However current starts flowing because of the battery. Now if you increase the battery, if you increase the battery voltage what would happen, more current will flow. How does this current flow, they don't flow by diffusion they flow by electric field. A field is created between D and this and therefore the electrons are moved away from this source towards the drain.

Student: Sir how is reverse biased increasing (0)(39:19).

Professor: What is the reverse biased here? The battery negative is here and it is connected to the gate so the reverse biased here is 0. Reverse biased here is exactly equal to V_{DS} . And it's a resistive material so the bias continuously increases. There is a drop across the n type material okay, no that's not clear? No. You see let's take this end at this end what is the difference between of voltage between the n type and the p type material 0, isn't that right? Because V_{GS} is connected here and at this point it is highest at this point it is V_{DS} therefore the bias goes from 0 to V_{DS} along the length. So it continuously increases and it's a resistive material mostly this increase is linear. But the depletion region becomes curve line. Current starts flowing. If you apply more V_{DS} more current will flow because it's a basically a resistive material till a certain peculiar phenomenon occurs. And this phenomenon, before we discuss this phenomenon I will come to this phenomenon a little later.

(Refer Time Slide: 40:49)



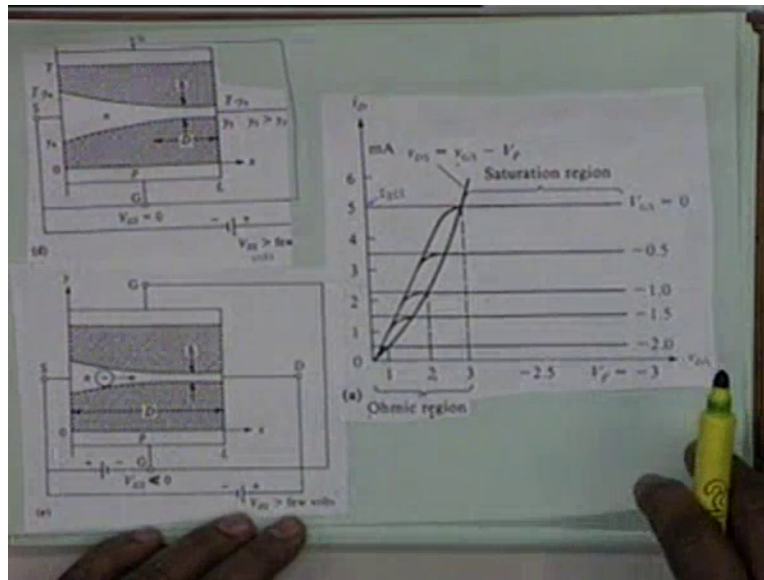
But suppose consider another situation a situation in which V_{DS} is maintained at 1 to 2 volt a small positive voltage and a V_{GS} is applied a reverse voltage with negative connected to p and

positive connected to n is applied. If it is applied then what happens, there is there was a depletion region like this in addition V_{GS} creates a further depletion so they profile changes okay, the profile changes. Suppose V_{GS} is increased reverse biased is increased if the reverse biased is increased no yes this is reverse biased. Let's go back to V_{GS} equal to 0 I_D versus V_{DS} this will be linear because it was a ohmic material okay. Now this linear variation obviously shall be affected if V_{GS} is made negative. If V_{GS} is made negative obviously current shall decrease, so if V_{GS} is some quantity let say V_P by 8 then the current shall, current shall rise linearly but the value of the current will decrease.

Therefore the current is been controlled by V_{GS} and if V_{GS} , V_{GS} is negative is negative terminal connected to p positive to source, so this junction pn junction between the gate and the source is reverse biased. If this reverse biased is increased a point will come at which the the depletion the two depletion regions will meet somewhere near the gate. If that happens then you have emptiness all around. There is no electron alas no electron can cross to the other side correct? So when V_{GS} V_{GS} reaches a voltage V_P which is called a Pinch-off Voltage, Pinch-off because the the two depletion regions come and meet here. They look like a pinch. And the current becomes equal to 0.

The drain current doesn't flow. So V_{GS} can completely kill can completely kill the transistor conduction which means that V_{GS} can make the transistor what is the language? Cut-off no current flows so it's cut-off. V_{GS} can make it cut-off but V_{GS} can make it conducting okay. It can make it conducting to varying degrees by varying V_{GS} is this point clear. But since V_{DS} is small the variation is still linear. That is it's still ohmic the region the n channel still is a ohmic resistance, it behaves like an exactly a small ohmic resistance.

(Refer Time Slide: 44:09)



Now we go back to the situation where V_{GS} is equal to 0. V_{GS} is equal to 0 in between we had take a detour and V_{DS} is increased. Now initially as I said V_{DS} if V_{DS} increases the current increases because it's a ohmic resistance, this is the characteristic for V_{GS} equal to 0 okay the upper line. The initial person is ohmic, it increases linearly. Then obviously a pinch-off condition will occur at terminal at this point. The two depletion regions will gradually try to merge towards each other. And we expect that the current should be 0 no but then as soon as you merge at the drain terminal a very interesting situation occurs the material no longer remains an ohmic material. The electrons which are the carriers they acquire so higher velocity that they pass through the pinch-off and get collected by the drain.

Not only that not only that. The velocity of electrons attains a saturation value due to collisions the high field electrons, when they try to go over to the drain. They are in a hurry they collide with each other. And this collision it's a statistical phenomenon, there is deep mathematics involved in this. But the end results as far as the circuit people are concerns electrical engineers the end result is that the saturation reaches a the velocity reaches a saturation value. And if that happens then the current levels off the current becomes constant, it doesn't become 0. The current levels off at this value. And at V_{GS} equal to 0 the value at which the current levels off is called the I_D the drain current under saturation value. It's called as I_{DSS} . This is the nomenclature that is given to it.

For this typical transistor it is 5 volt 5 ampere 5 milli-amperes I_{DSS} okay. Now this is the situation and V_{GS} equal to 0 suppose more of V_{GS} is made negative minus 0.5. Then obviously this saturation will occur at a lower current right because V_{GS} negative means it has controlled it has reduced the it has increased the depletion region so it is controlled. So it will occur at a lower value. Similarly if we increase it to minus 1 minus 1.5 minus 2 and so on, the current will continue to decrease till V_{GS} reaches the pinch-off voltage. And at the pinch-off voltage no current shall flow and this line the V_{DS} line is the line for V_{GS} equal to V_P and V_P here is minus 3 volt okay. 0 minus 0.5 minus 1 minus 1.5 minus 2 minus 3.

As you notice as you notice the lines are still parallel to the V_{DS} axis, this characteristics are very similar to BJT characteristics except for the fact that these this is more inclined towards V_{DS} the slope here is less. Whereas in BJT it was almost vertical at $V_{CE\ Sat}$ it was 0.2 volt for silicon. Whereas here it goes right up to 3 volts and this voltage obviously is the pinch-off voltage. This in this in this region in this region V_{DS} is less than $V_{GS} - V_P$. In the other region when saturation occurs saturation occurs saturation of the current occurs V_{DS} is greater than $V_{GS} - V_P$ and if a characteristic is given then you can immediately find out which is the pinch-off voltage V_P . Obviously this region is the ohmic region where the current increases linearly with V_{DS} okay. So basically the current I_D is a function of V_{DS} but the functional nature is controlled by the gate to source voltage alright

Now you notice other differences therefore equal change of V_{GS} equal change of V_{GS} the current does not change equally. You see the separation between these lines? And therefore FET is a non-linear device. Even in the active region they would be non-linearity. Linear amplification is more convenient to do with BJT rather than FETs because the separations are not equal. These are not at equal intervals.

(Refer Time Slide: 49:41)

The image shows a whiteboard with handwritten mathematical expressions. At the top, the drain current i_D is given as $i_D = I_{DSS} \left(1 - \frac{v_{DS}}{V_P}\right)^2$, with an arrow pointing to the right. Below this, the condition $|v_{DS}| \geq |v_{GS} - V_P|$ is written. To the left of this condition is the symbol r_0 . The next line shows the partial derivative of i_D with respect to v_{DS} at the operating point Q, which is equal to $\frac{1}{r_d}$. Finally, r_d is defined as the dynamic drain resistance.

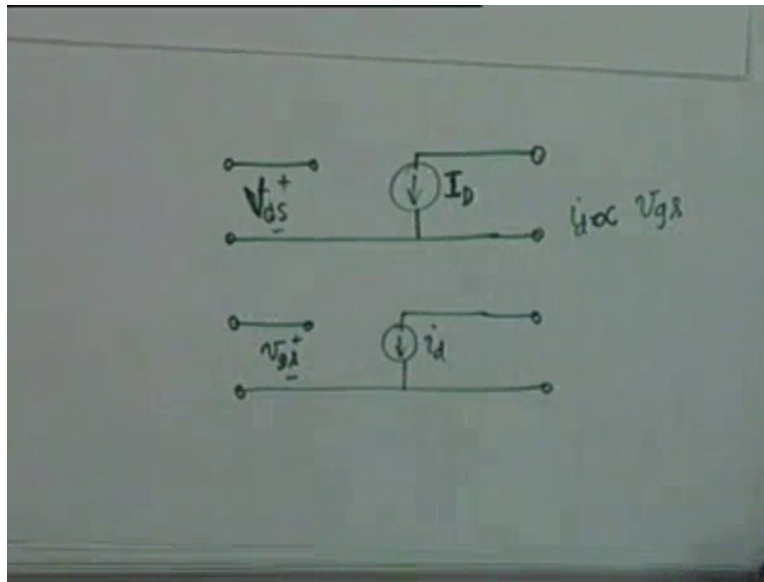
$$i_D = I_{DSS} \left(1 - \frac{v_{DS}}{V_P}\right)^2 \leftarrow$$
$$|v_{DS}| \geq |v_{GS} - V_P|$$
$$\frac{\partial i_D}{\partial v_{DS}} \Big|_Q = \frac{1}{r_d}$$

$r_d =$ Dynamic Drain Resistance

And in fact the current relationships for an FET is equal to I_{DSS} we are considering a junction FET I_{DSS} , that is that saturation value multiplied by 1 minus V_{GS} divided by V_P where V_P is the pinch-off voltage square of this, and this is what gives the non-linearity. It's a square law characteristics rather than a linear characteristic and this is why the separations continuously increase as we will go towards lower and lower V_{GS} okay. This condition happens when V_{DS} is greater than greater than or equal to V_{GS} minus V_P . Which means that we have crossed the saturation value. We have crossed the ohmic region, it is in the saturation region that this characteristic holds good. Obviously obviously this characteristic is independent of V_{DS} . Well it has to be so, because if you look at the characteristics it is independent of V_{DS} the current remains a constant. It only depends on V_{GS} ; it only depends on V_{GS} .

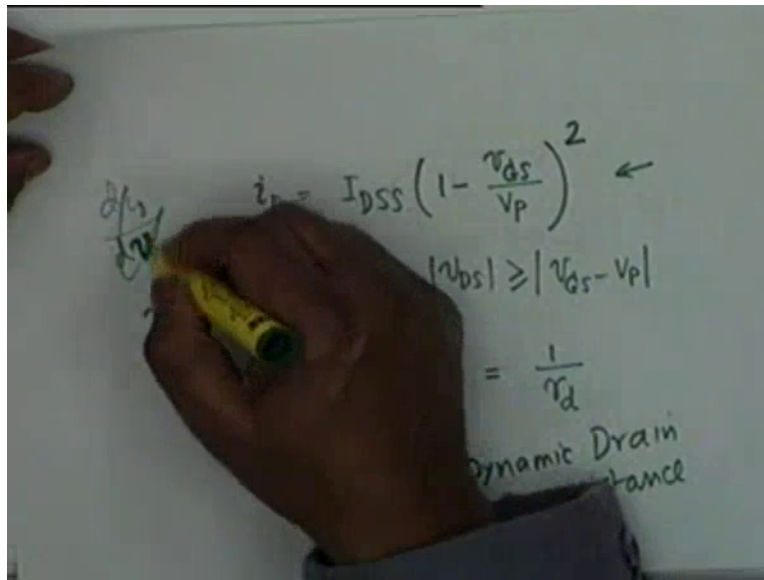
However like the BJT characteristics where you saw that there was a slope a very small slope and you have defined a resistance r_0 as the early voltage divided by the collector current, here also i_D is not absolutely constant. You can define a $\frac{d i_D}{d V_{DS}}$ at the operating point okay the slope. There is a slope which is which is denoted by $\frac{1}{r_d}$ it is the dimension of conductance right? It is denoted by $\frac{1}{r_d}$ and small r_d ; you understand the meaning of d the subscript d ? Small r_d is called the dynamic drain resistance. R_0 in BJTs as per the dynamic collector resistance okay. So r_d is a dynamic drain resistance

(Refer Time Slide: 52:12)



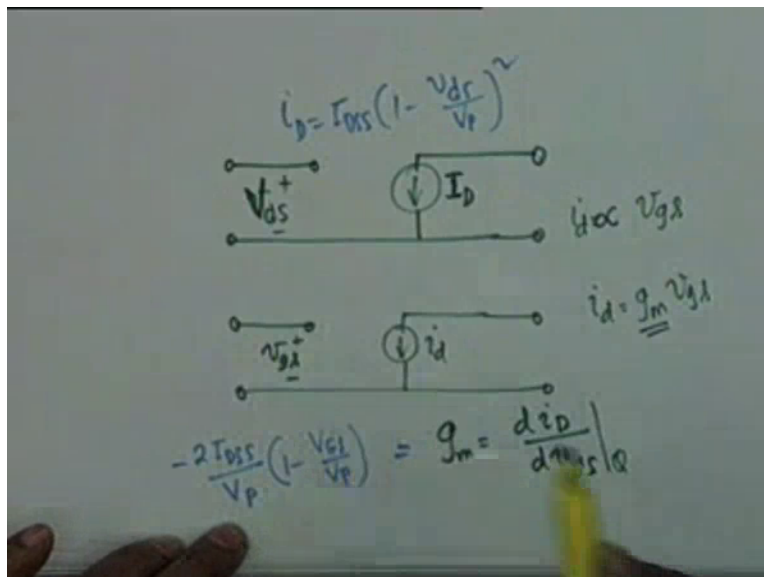
And as you can see as you can see the model for an FET will be much simpler you have a V G S you have a V G S here. And there is a current i_D that's it. As far as the DC conditions are concerned. There is a V G S applied between because it's a reverse biased junction, no current flows so it's an open circuit here and in the output circuit there is simply a collector, there is simply a drain current i_D . So this will be the DC valve to indicate that this is DC, this is the DC model, the resistance is very large and therefore we don't show it here, this is a simple model. Whereas if you take the AC model then what will happen is you take V G S and the current i_D which would be i_D would be what? How is it connected to V G S i_D will be proportional to V G S and the proportionality constant will be $d i_D / d V_{GS}$ okay.

(Refer Time Slide: 53:47)



If you take this relationships here $d i_D / d V_{GS}$, I made a miss.

(Refer Time Slide: 53:58)



No the proportionality constant is, what should be the dimension of the proportionality constant? Conductance so i_D is written as $g_m V_{GS}$ g is for conductance, why this m , subscript m ? M is for mutual that is the current and the voltage do not occur at the same point, it is not self-admittance it's a transfer admittance. And therefore it is called a trans-conductance. g_m is called a trans-conductance and g_m is by definition $d i_D / d V_{GS}$ at the Q point. And if you take the characteristic obviously this will be equal to g_m would be equal to, if you take the characteristics

what is the characteristics i_D equal to $I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$. If you differentiate this, then you get $-2 I_{DSS} \frac{V_{GS}}{V_P} \frac{1}{V_P}$. And you see g_m is indeed linear with respect to V_{GS} , V_{GS} is the operating point that is the DC gate to source voltage. We will start from this point next time.