Analog Electronic Circuits
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Lecture 28
Problem Session 7 on Differential and Power Amplifiers

This is 28th lecture, problem session 7. We will take a couple of problems on differential amplifiers and fairly involved problems from power amplifiers. Three problems we proposed to work out. Before we take up the problem a small point that we missed in class B power amplifiers, I want to illustrate this. The simple class B power amplifier was like this, R L and the two bases were connected and the input was applied here, okay. Now this goes to minus V E E and this goes to plus V C C.

Now you notice that the load current i L is biased the following relationship to i C 1 and i C 2. I L is the difference between the two, is not it right? I C 1 equal to i L plus i C 2 therefore i L equal to i C 1 minus i C 2.

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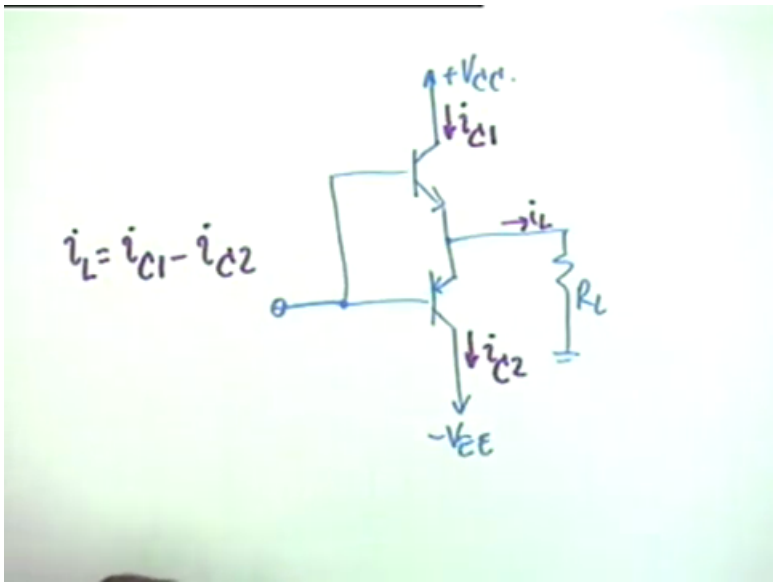

What is the waveform of i C 1? If you ignore crossover distortion or if you have taken care of crossover distortion by using two diodes here then the waveform of i C 1 is half rectified sin and the waveform of i C 2 is also half rectified sin but shifted in phase by 180 degrees, okay. This is the basic form. Now if you expand i C 1, this half rectified sin wave or cosine wave in fully a series then because of this symmetry in the waveform you get only cosine terms.

That is a DC and only cosine terms, no sin term and therefore I can write i sub C 1, this half rectified sin wave as some DC A 0 plus A 1 cosine of omega 0 t let us say. This is the signal that I have applied plus its harmonics due to distortion, okay, because power amplifier are large excursion amplifiers, large excursion of signals and therefore there will be distortion and this distortion maybe A 2 cosine of 2 omega 0 t plus etc. I do not know how many harmonics are there. Fully a series gives infinite number of harmonics.

So if we expand this in fully a series we get something like this. Similarly i sub C 2, the only difference between i C 1 and i C 2 is that they are 180 degrees phase shifted. In other words it becomes A 0 minus A 1 cosine omega 0 t, then this would be plus A 2 cosine 2 omega 0 t and so on. The next would be minus and so on.

Now if I take the load current i L as the difference between the two, obviously the DC terms cancel, no DC flows through the load. We get twice A 1 cosine omega 0 t and the next term is twice A 3 cosine of 3 omega 0 t, okay, and so on. So only the fundamental and its odd harmonics are present.

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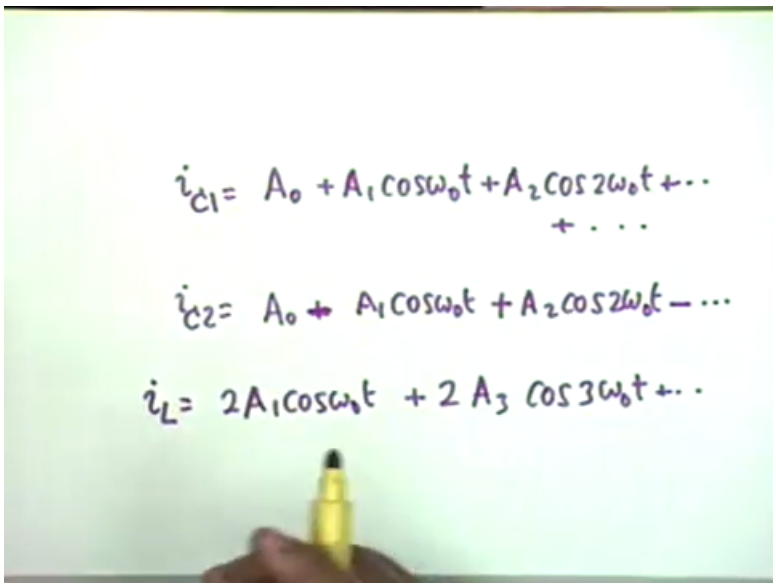

As you know from general experience of fully a series expansion that these amplitudes A 0, A 1, A 2 usually for a half rectified circuit they are in decreasing orders of magnitude and therefore this second harmonic is the major cause of distortion in i sub C 1, okay. The major harmonic component in i sub C 1 is the second harmonic because the amplitudes are in decreasing order, alright.

And the second harmonic gets cancelled out therefore class B only retains third and higher harmonics which means that the THD total harmonic distortion would be square root of 4 A 3 square plus 4 A 5 square and so on divided by twice A 1, agreed? This 4, 4, and 2 could be cancelled out.

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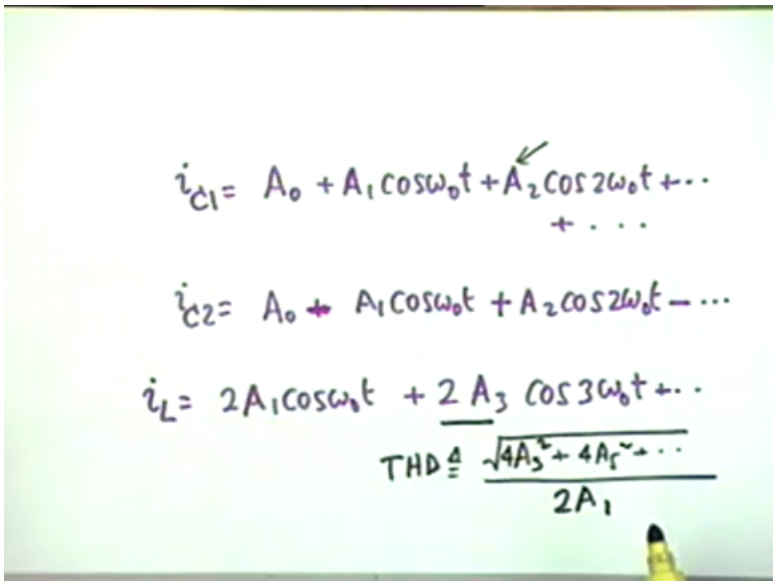

Now this is one of the advantages of class B amplification that the distortion automatically is less because the strongest harmonic component in either of the two waveforms i C 1 and i C 2 gets cancelled out, okay. This is the point in favour of class B amplifier and of course the point that no V C flows through the load. The DC, the average value of current is 0, okay. Now we take up the problems. Okay, I did not set any problem in the tutorial sheet on FET amplifier so we will take FET differential amplifier.

Two examples of FET differential amplifiers, one of them is this. Draw with me a differential amplifier. We did not discuss the theory in a great detail either because the theory was very similar to BJT. So we shall illustrate this through a couple of examples. We have the Q 1, no I should have drawn like this, Q 2. Then the two sources this is the drain, this is the source terminal.

The two sources are connected together so it is a source coupled pair rather than an emitter coupled pair and then we have an R sigma. This goes to minus V S S, okay, and this current is I S S. I S S naturally is twice of I sub D, okay. I S S is twice of I sub D because of the complete symmetry and then of course you have the signal source here and a signal source here. This is the circuit.

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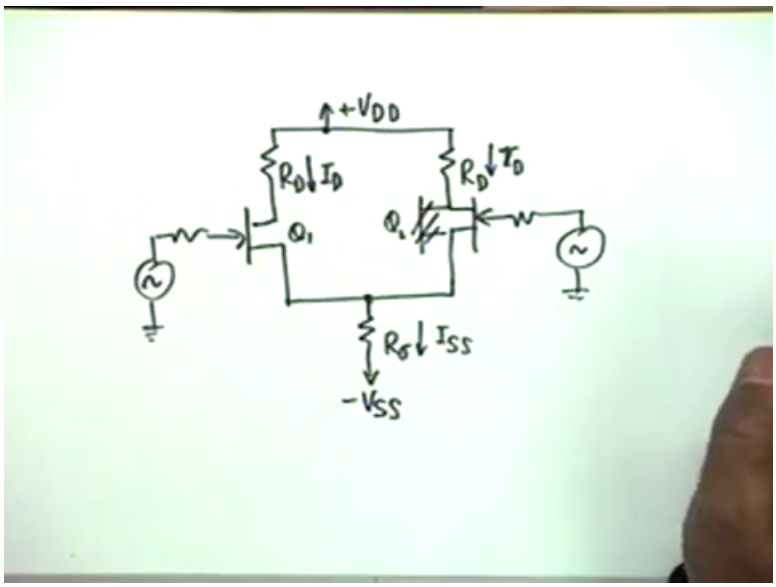

Now the problem says that R sub D is given as 50 K. Obviously it is not an IC, it is a discrete design. R sub D 50 K. I D S S, you require this quantity. This relates current to V G S. I D S S is given as 2 milliampere and the biasing is such that I S S is 500 microampere which means that I sub D is 250 microampere. And in addition you also require the data on V P, the pinch of voltage that is given as minus 3 volt. The questions are to find out the following. A sub d, the differential gain.

Then R sub sigma if V D D equal to V S S is equal to 10 volt. These two quantities are to be found out and we also need the C M R R in decibels. These are the problems. These are the given conditions. You are required to find out A d, R sigma if V D D and V S S both the supplies are plus minus 10 volts and the C M R R in decibels.

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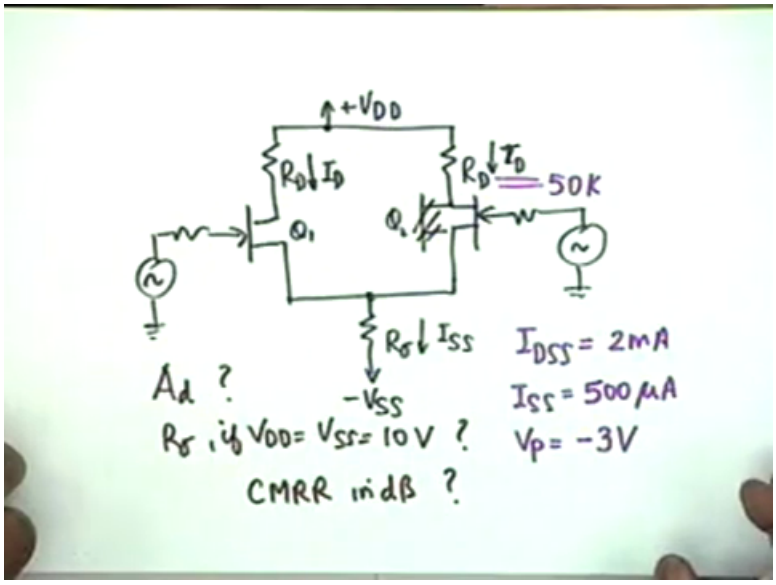

The first thing we do is find out g m, okay. You know the relationship is I D equal to I D S S 1 minus V G S divided by V P whole squared and g m is d I D d V G S and we had shown earlier that this can be written as by differentiating this and simplifying minus 2 by V P. And then you can write square root of I D I D S S. This can be very easily established. We have eliminated V G S, okay.

Student: (())(10:01)

Small i D and small v G S, okay fine. And we are finding this at the Q point, correct. And this is the final result.

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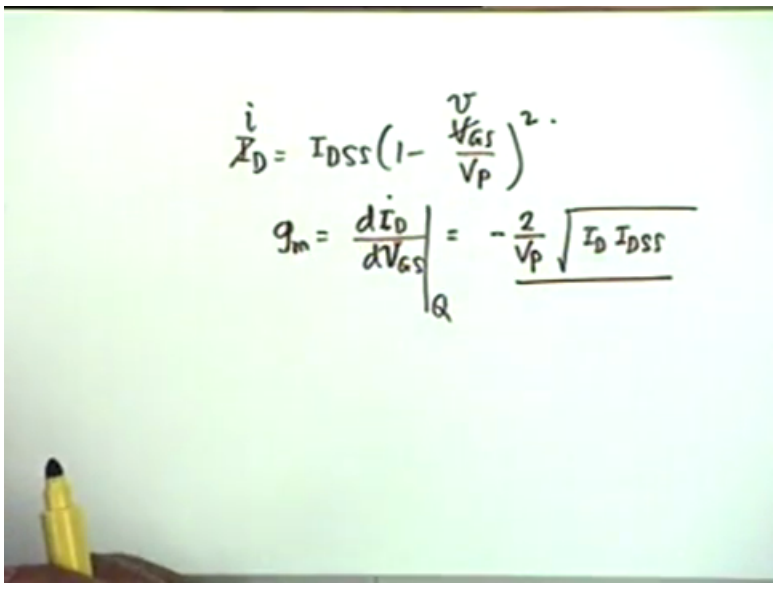

Now if I substitute the values you see g m is minus 2 divided by minus 3, i sub D is 250 microamperes and I D S S is given as 2 milliamperes, 2 times 10 to the minus 3 and so many moles. If you calculate this out my result is 471 times 10 to the minus 6 moles. Why did we find out g m? Because this we required for calculating the differential gain A d.

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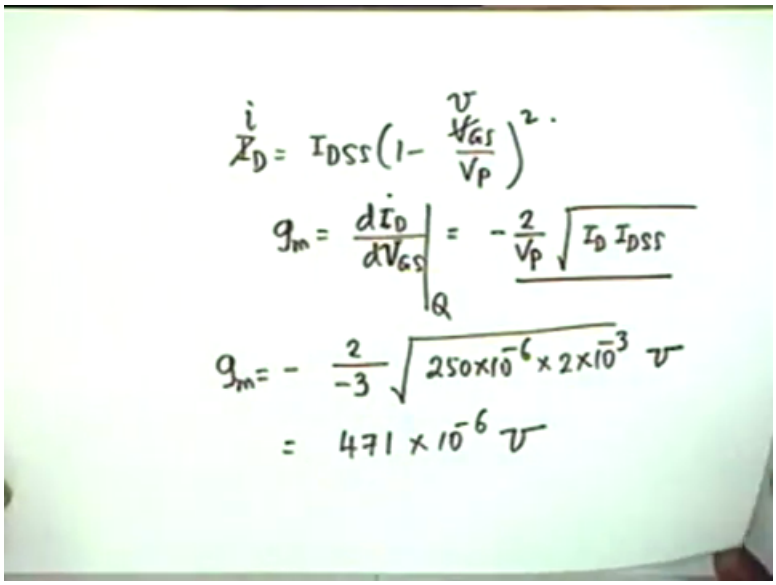

A d therefore, the differential gain is simply equal to minus g m times R D. Therefore it is 471 minus times 10 to the minus 6 multiplied by 50 into 10 to the 3. It comes out as minus 23 point 6. I do not know how that point 6 comes? It should have been, okay. That is how they simplify. This is 23 point 6, okay. Now in order to calculate R sigma you first note that from I D, R sigma obviously has to be calculated from application of the KVL, okay. And that KVL we want to do it through V G S, okay.

V D D, I D R D, V D S Q and then V G S then we go to ground, okay. So I calculate V G S first. I D is I D S S 1 minus V G S by V P whole squared. I know I D, I know I D S S, I know V P and therefore I can calculate V G S. V G S, my calculation gives it as minus 1 point 94 volt. It has to be negative. Gate has to be negative with respect to source.

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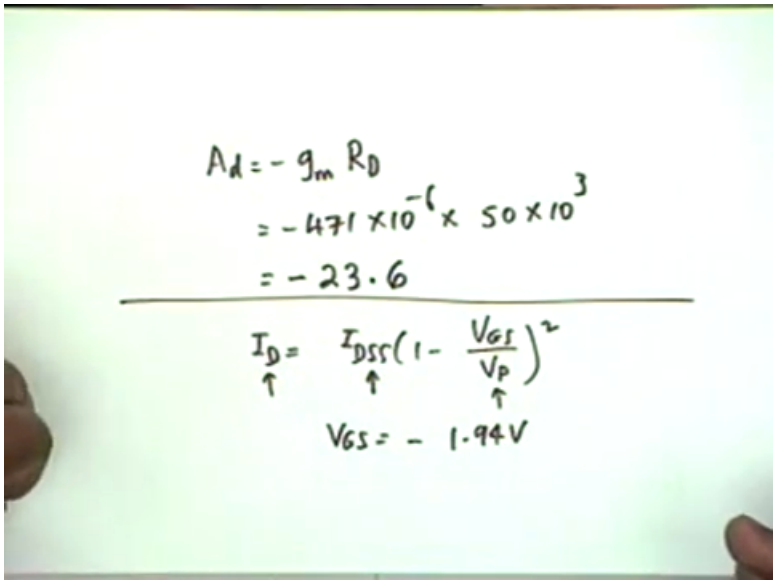

Then I write a KVL like this. I come from here . What is the DC voltage at this point, 0, because the source is grounded for DC there is a resistance. So V G S plus I S S R sigma minus V S S would be equal to 0, is that clear? Okay, so I write this V G S plus I S S R sigma minus V S S equal to 0 in which you know V G S. We have already calculated minus 1 point 94 volt. We know V S S, it is 10. We know I S S which is 500 microampere.

Therefore I can calculate R sigma and my calculation gives 23 point 8 K. Finally I require the C M R R and if I know g m and R sigma, C M R R is cleared. It is 1 plus twice g m R sigma. It was 1 plus twice g m R E E in the earlier case, it is R sigma and if you substitute the values this comes out as 22 point 44. I am skipping this numerical calculation. I have already done that so I do not guarantee that it is correct. So I argue to verify this.

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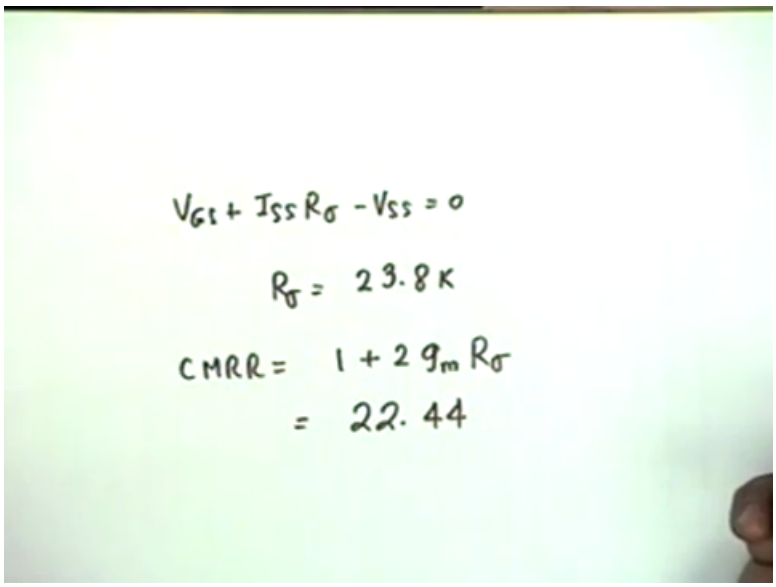

Now the point is you have to find C M R R in dB. So you write not equal to, equivalent to, okay. Three parallel signs. 22 point 44 is the ratio of A d to A c. If you want to calculate this in dB this is 20 log 10 of 22 point 44 which is equal to, now you can write an equal to sign. Be careful about this okay. You cannot write 22 point 44 equal to 20 log 10 22 point 44. It is equivalent to, okay. So three signs and this comes out as 27 point 4 decibels, my calculation. I made some s numerical mistakes somewhere so you please do check this.

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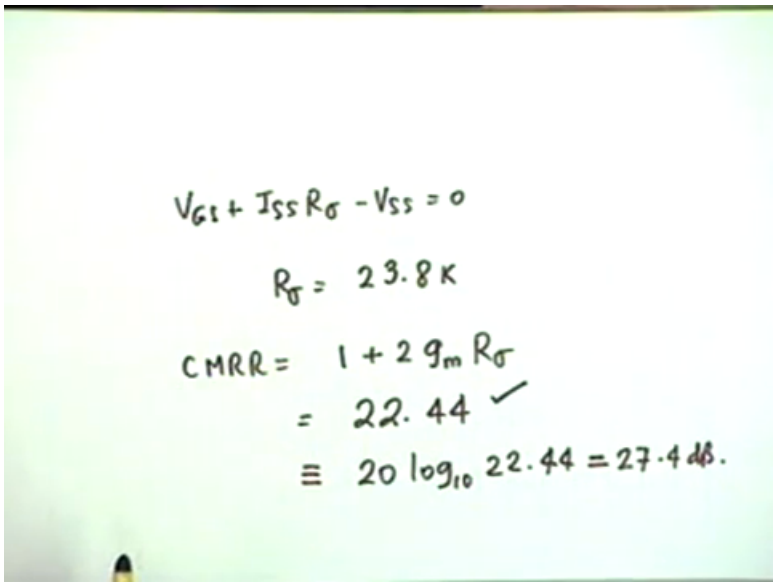

The second problem that we want to take up is a design problem. The problem is to design a source coupled n channel JFET. Design a source coupled n channel JFET differential amplifier to meet the following specifications. One is that the differential gain should be minus 10. The V D S Q, we have the Q point, it should be equal to 5 volt. Under this condition compute the C M R R.

What is the C M R R? For your design what is the value of C M R R in decibels? That is what is wanted and the data given about the n channel JFET is that I D S S, this must be given, is 1 milliampere. It may be given directly or indirectly, okay. It may be given such that when V G S equal to this much, the drain current is this much. This indirectly gives you I D S S.

So you will have to find this out. I D S S is 1 milliampere, V P is minus 3 volt. It is also given that the load is restricted to be 20 K and it is given that if small r d is not infinite then you have to parallel it with whom? Capital R D. Capital R sub capital D. Small is given as negligibly large, okay.

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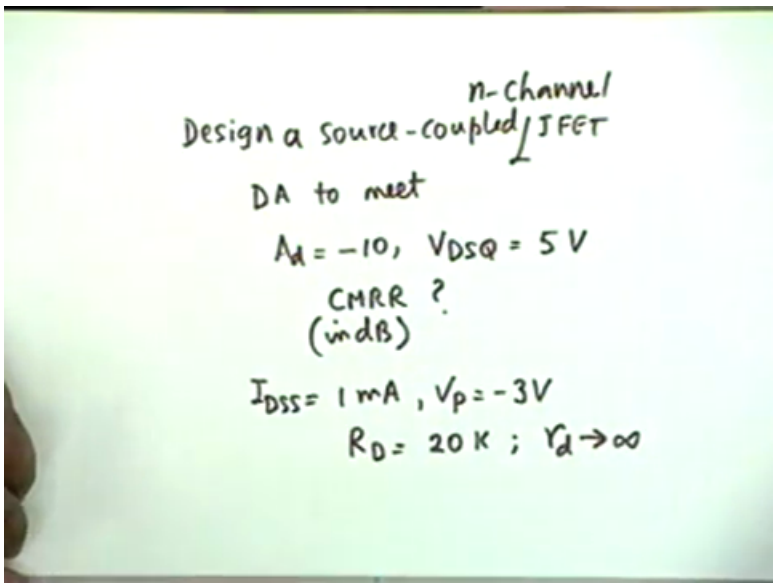

It is so large that its effect can be neglected, okay. Now the first thing we do is we start from A d because we know R D, therefore we can find out g m. A d is minus 10, this is given and this should be equal to minus g m times, R D is 20 K and therefore we find out g m. G m is 0 point 5 millimoles.

G m is also equal to minus 2 divided by V P square root of I D I D S S, okay, in which we know V P, we know I D S S, therefore I can calculate I D, okay, the drain current. Therefore I D which is equal to g m squared V P squared divided by 4 I D S S. This calculates out to point 56 milliampere.

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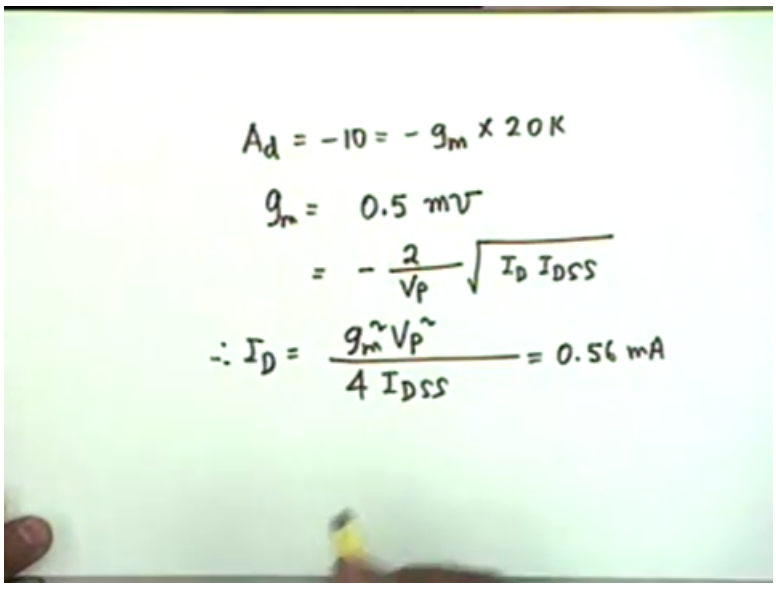

And if I know I D then I can also calculate V G S which I require. From the relation I D equal to I D S S 1 minus V G S by V P whole squared I get V G S is equal to V P, then 1 minus square root of I D by I D S S, okay, and this calculate out as minus point 75 volt, alright? So the design means what? We have to fix the supplies now V D D, V S S and what else? In the simple differential amplifier, R sigma.

Now for V D D you notice that V D D is equal to I D R D plus V D S Q which is given, the operating point is given, then when you go to S you can then go to the ground via V S G which is minus V G S, agreed? Is this equation clear? We come from V D D, I D R D, V D S Q, then from source to ground via gate V S G which is minus V G S. So let us substitute the values then we get this as point 56 milliampere multiplied by R D is 20 K. V D S Q is given as 5, minus V G S would be plus point 75 and this comes as 16 point 95 volt, okay.

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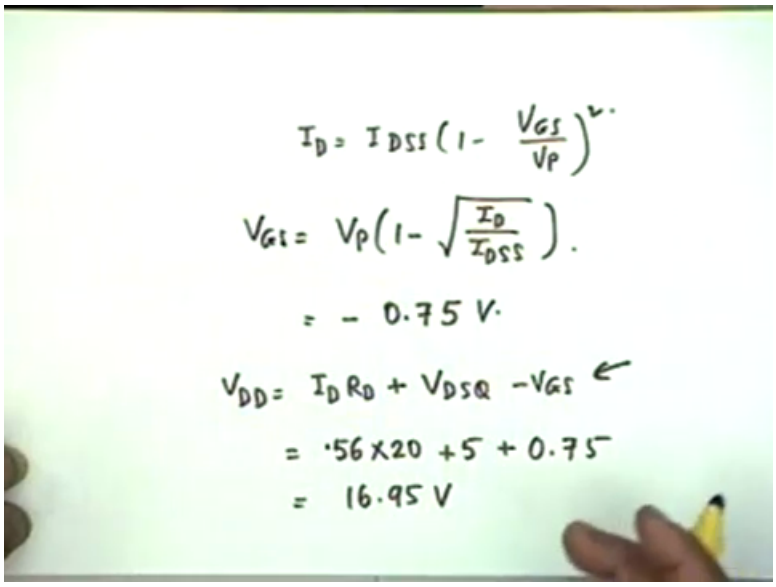

An odd value but it can be adjusted. You can make slide adjustment in R D to make it 17 volts or reduced it to 15 and so on. Now as far as V S S is concerned for V S S we can write the following equation. V G S plus I S S, we are coming from the ground, V G S plus I S S multiplied by R sigma then minus V S S equal to 0. Now we know V G S which is minus point 75, we know I S S. How much is that?

Student: 1 point 02.

1 point 02, twice point 56, okay. Multiplied by this is milliampere. So if I write R sigma this will be in K, alright, minus V S S equal to 0.

Student: Sir, it is 1 point 12.

What is 7 point 1? Oh! This is 1 point 12, yes. Point 56 multiplied by 2 is 1 point 12. I agree. I could not but agree, okay. Now the point is from one equation obviously. We have no other knowledge. From one equation we cannot determine two quantities. But it is a problem with design therefore you should be happy you can choose one according to your convenience.

Now if you have chosen V D D to be equal to 16 point 95 there is no reason why V S S cannot be minus 16 point 95. So you choose V S S as 16 point 95 volt, chosen. Then you can find out R sigma and this R sigma comes as 15 point 8 K, is the point clear?

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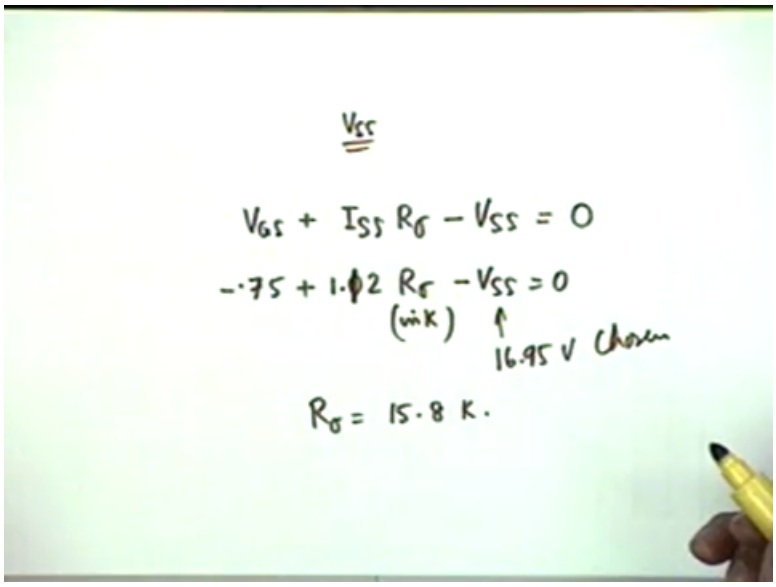

There is one equation, two unknowns, you choose one and the guideline is you choose V S S equal to V D D. There is no hard and fast rule. You could choose V S S. Could you choose V S S equal to 0?

Student: No.

Why not?

Student: (())(22:43)

No, but the drop in R sigma how can you avoid that? V G S should be negative. So V G is 0, V S should be positive, okay. Now R sigma what I am saying is could this be taken to 0. This is I S S flowing through this so this potential obviously should be positive.

Student: Sir minus V S S plus I S S R sigma should be less than 0.

That is right. That condition V D S should be greater than V G S minus V P that puts a constraint. In some cases you may be able to put V S S equal to 0. But as I said there is no point in choosing a V S S equal to 0. During our power supply and all power supply usually IC power supply are plus minus and equal voltages. There is no reason why you cannot choose this.

Finally we calculate the C M R R as equal to 1 plus twice g m R sigma. Everything is known and therefore this ratio comes at 16 point 8 and my calculation shows that it is 24 point 5 decibels, done.

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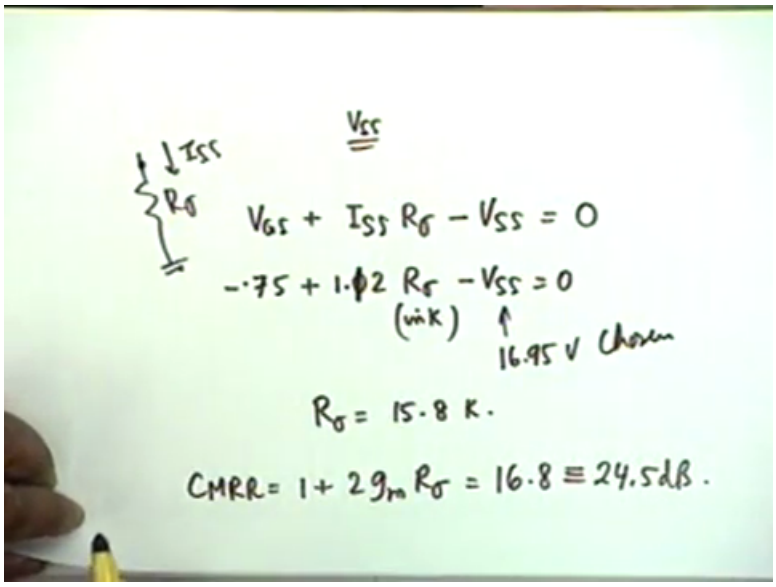

What else was needed in this? C M R R and that is all, okay. Then last problem of the day. Please pay attention to this because through this problem I also want to illustrate a practical output stage of an operational amplifier and this opium is mu A 725, not 741, 725. The actual circuit I am going to draw and then set out what we are required to calculate. The actual circuit is this. You will see that the numbers of the transistors are very large numbers.

I mean these are parts of the total circuit. So I am drawing only the output stage. Output stage is required to drive some current through a load and therefore it is a power amplifier stage. It is a class AB stage so that there is no distortion, okay, the output stage. Q 21 and then this goes to plus V C C. I would like to start from another page because it is a fairly large circuit and I cannot use space. V C C, this goes to Q 21 which is an NPN transistor. Then we have a resistance R 16.

There is a variation in the class B stage, okay. R 16 which is 25 ohms. We have another resistance also R 16 which is also 25 ohms. It has to be symmetrical. In all the circuits that we drew so far the emitter was connected to the collector of the next transistor. But here it is connected to two resistors and then of course we have the PNP transistor and this is Q 26 and Q 26 goes to minus V E E. The collector goes to minus V E E, the load is connected from the middle point.

Obviously it has to on the symmetry. I will explain the purpose of R 16 a little later and then you have the R L here and of course the voltage output is across the R L, V 0 t.

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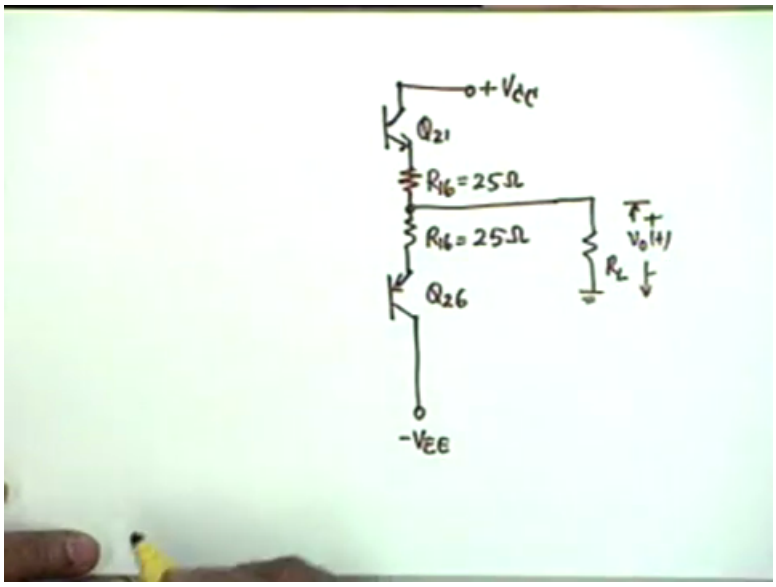

Now from the collector you require the drive to avoid crossover distortion. You required two diodes which have exactly point 7, point 7 drops, okay. Those diodes are obtained in a peculiar manner. the base of Q 21 goes to a diode connected transistor Q 18. These numbers are there because there are other transistors which we are not drawing, okay. This is a diode connected transistor but not from here, it is from this base, okay.

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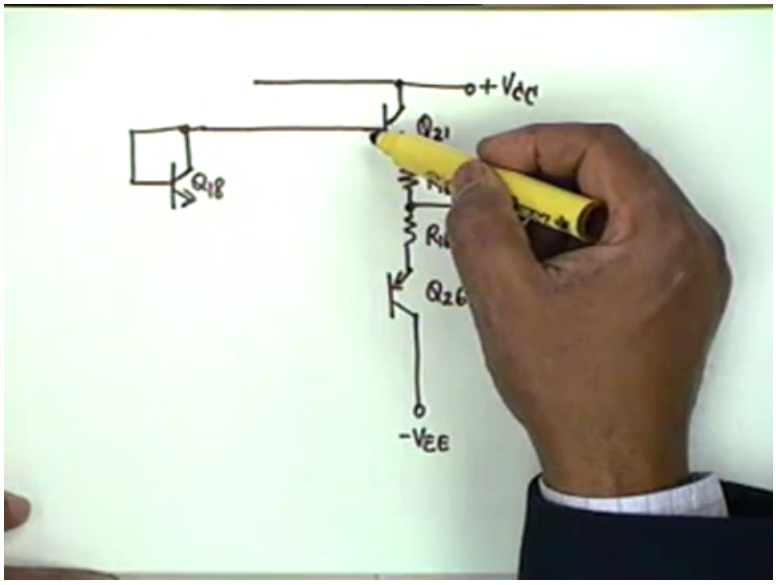

And in order to drive a current through this we require a resistance from here which is R 15, okay. Then we require another such diode connected transistor but for reasons of the overall mu A725 design it is connected like this. It is not connected as a diode, it is connected like this. This is the V i t, the input from the previous stage. The previous stage could be a differential amplifier, okay.

And instead of getting this connected as a diode, this is connected like this. Does this make a difference? As far as the balancing is concerned this base to emitter shall be point 7 and this base to emitter shall also be point 7. All that we needed was that this junction should be the same potential is this junction.

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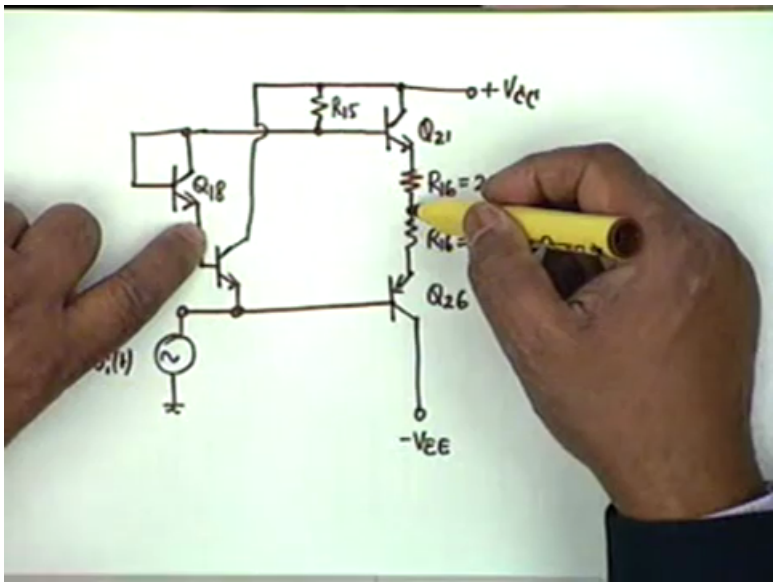

And from symmetry there is no reason why these two voltages should not be equal. Q 18 and this is Q 19, are identical transistors and therefore the voltages at the base V B E should be identical, okay. Now, why these R 16s? What is happening is that there are two more transistors. I will shortly explain why this is so. There are two more transistors Q 23 and the emitter is connected here, the base is connected here. Is the connection clear?

The base is connected here that means across the base to emitter there is a resistance R 16 and a very similar thing repeating here that is you have a PNP transistor like this. This comes here and the base is connected here.

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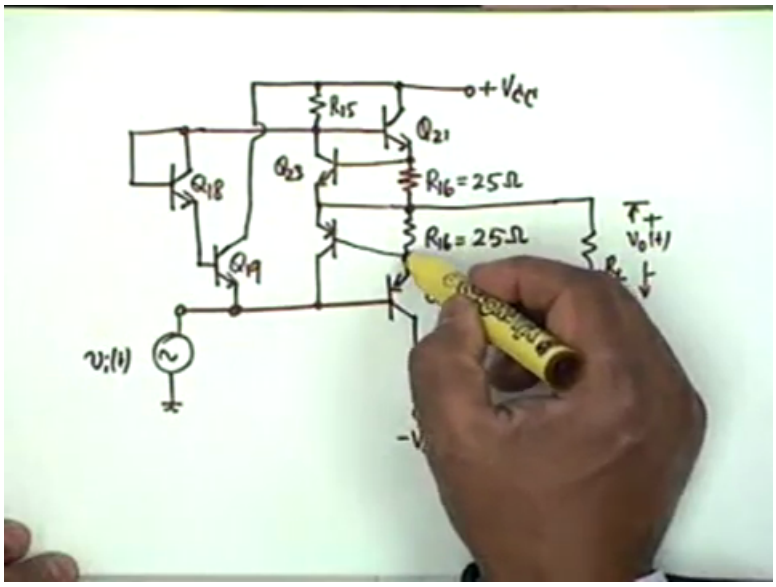

Absolutely symmetrical. This is Q 24. Is there a 24 here? No. This is Q 24, okay. And like R 15 there is an R 15 here. V C C and V E E are usually identical. Why is this R 15? To be able to drive this transistor, the PNP transistor, okay.

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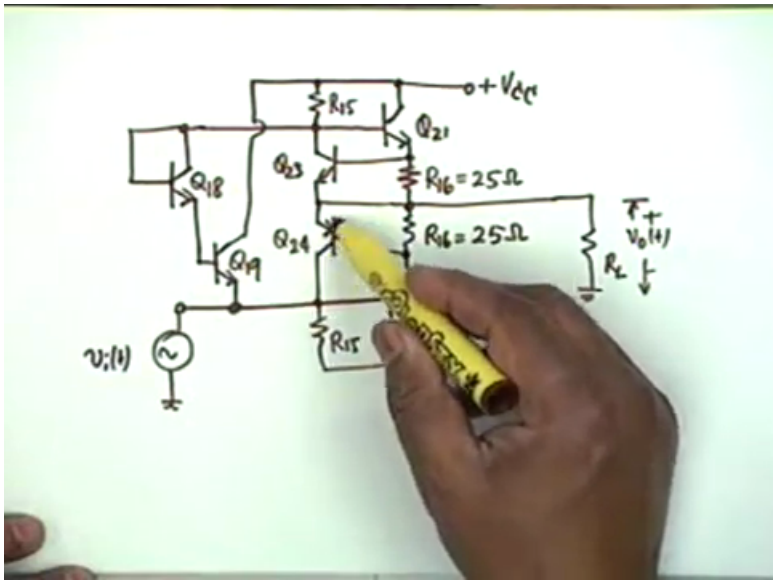

This is the actual circuit, what goes on inside the 725. Actual circuit of the output stage of a mu A725 amplifier, okay. I have already explain the purpose of Q 18 and Q 19. These are to avoid the crossover distortion. Now why Q 23 and Q 24? Let me first explain qualitatively then I shall discuss what the problem asks for. Qualitatively you see suppose R 16 was not there. R 16 is 0, this transistor is not there. R 15 is there to be able to drive the base of Q 21 and Q 18 and Q 19, okay.

Suppose R 16 Q 23 are not there, alright. Then if R L is accidentally short circuited, okay, if R L is very low then what is the drop across Q 21, collector to emitter? It is V C C, plus 15 whatever voltage it is, okay. Now therefore Q 21 will draw a large current and it might go. We do not know what the V C C supply is. It might go into the breakdown region or it might get so saturated that it is difficult for it to come out of saturation.

Saturation means charge accumulation and the charge requires a long time to come out of saturation, okay. So this resistance and Q 23, the two together, the function for R 16 and Q 24 exactly the same during the negative half cycle of the input voltage, okay.

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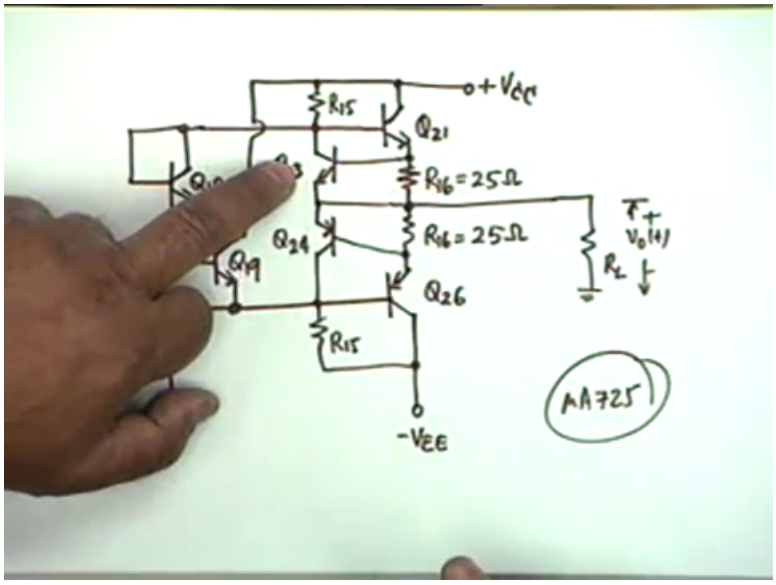

So it suffices to consider the positive half cycle. During the positive half cycle Q 21 is supposed to conduct and if R 16 is 0 and R L becomes accidentally short circuited the transistor Q 21 will have to put up with the full drop of V C C from its collector to emitter. It may be too much for the transistors.

On the other hand if Q 23 and R 16 are there then when the drop I C 1 is small, when the collector current of Q 21, I C 21, when it is small, the drop across the base to emitter of Q 23 will be less than V B E 23 on which is about point 7 and therefore Q 23 does not come into picture and the total current goes to the load R L. But as soon as I C 21 is large enough to make the transistor Q 23 on the verge of conduction, okay, then what happens is the input current does not totally go to Q 21, right?

When this transistor starts conducting Q 23, input current has to have two parts. One goes through I C 23 and the other is I B 21. So I B 21 is not equal to the input current, it is only a part of the input current and therefore when I C 21 increases, I B 21 decreases. And if I B 21 decreases, I C 21 also decreases, alright.

Which means that this voltage is limited to point 7 approximately taking Q 23 into the active region and therefore I C 21, well if you write the current equation at this junction, I C 21 this is the same I C 21 minus I B 23 should be equal to the load current, okay. No, there is another current here I E 23. So if I write the equation I C 21 minus I B 23 then plus I E 23 should be equal to I L, agreed?

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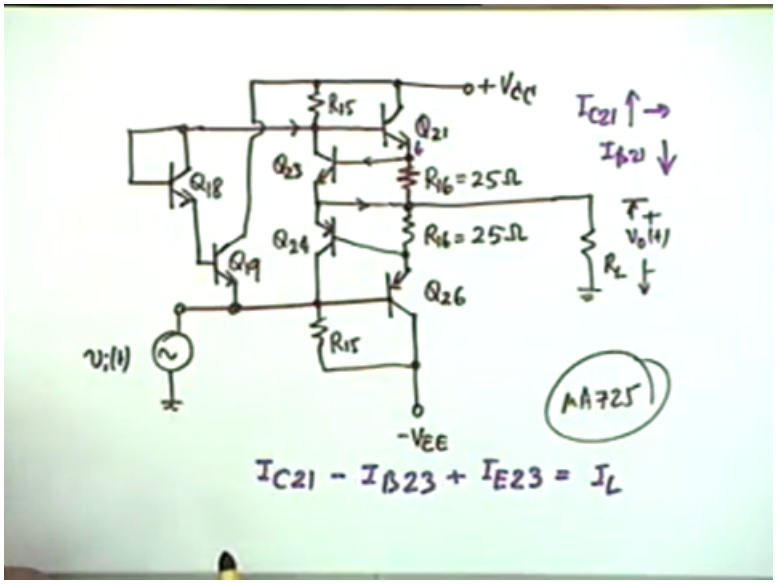

Student: (())(34:58)

Oh! When Q 23 conducts, Q 24 does not. You see this half does not carry any current when the other half is carrying current, right? This is the class B stage. The Q 21 conducts, Q 26 is off. Q 26 conducts in the negative half cycles, Q 21 is off. So it suffices to consider only the upper half of the circuit, okay. So now these I B 23 and I E 23 obviously are much smaller compared to I C 21. The beta is usually very large so I B 23 can be ignored. I E 23 which is a part of I B 21, previously we had I B 21, part of it is diverted as I C 23.

Therefore these two currents are very small. And since I C 21 is constrained to have a maximum value of V B E 23 divided by R 16, I L is also constrained, agreed? In other words this Q 23 and R 16 have been used for the purpose of short circuit protection, okay, short circuit protection that is if accidentally R L becomes short, the large current cannot flow through this transistor Q 21, agreed? A large current cannot flow since it is a short circuit protection.

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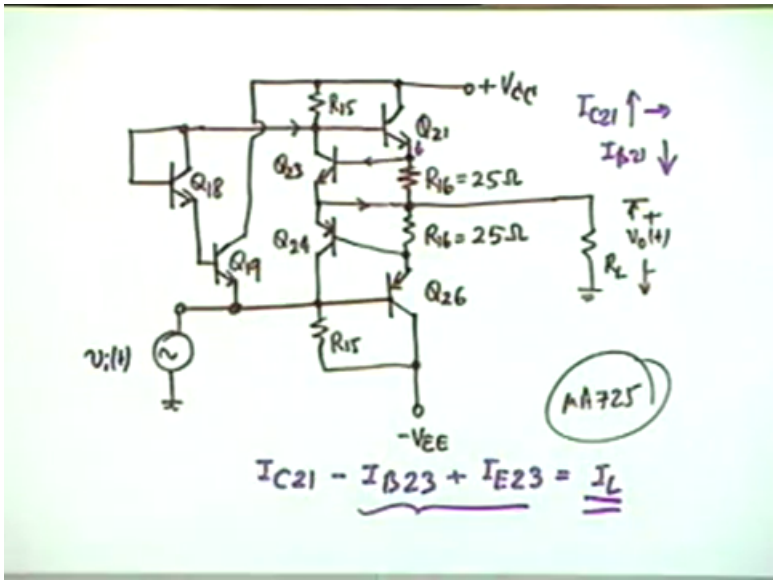

Now in this problem what is asked for is the following. Please follow this carefully. Have you been able to draw the circuit totally? Okay. What is being asked for is the following. Let V E E equal to V C C equal to 15 volt and R L is given as 2 K. First you neglect the effects of the 25 ohm protection resistor for normal operation. That is the 25 ohm protection resistor is not there.

First ignore R 16. The question that is asked is what is the maximum average power that can be delivered to the load? What is the maximum average power that can be delivered to the load by this circuit? Okay. This answer is absolutely simple. What is the maximum swing that is permitted across the load? Maximum possible swing. Pardon me. What is the maximum load that can be permitted?

Ignore the effect of R 16. R 16 is V C C minus V C E sat, okay, and therefore the answer to this question is very simple. If V C E sat is ignored compared to 15, point two can be ignored, it will simply become 15 square V m squared divided by 2 R L . Why 2? Because it is the root mean square value, okay. V m divided by root 2, is the root mean square value. 2 times and R L is how much? 2 K, and this comes out as 56 point 25 milliwatt. This is the simple answer.

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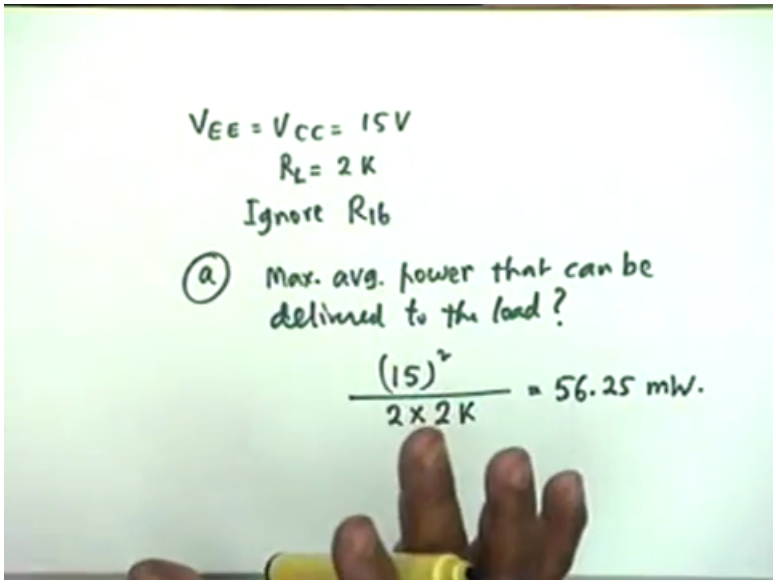

This has nothing to do with the complication of the circuit and things like that, alright? Okay. If you are fussy, instead of 15 you take 14 point 8, okay. If you do not want to ignore the V C E sat you take 14 point 8. But at this power level that is 56 point 25 milliwatt, at this power level what is the power required to be delivered by the power supply? How much power is required to be delivered by the power supply? That is how much is P D C?

If you recall we found out this as twice V C C multiplied by V 0 max divided by pie R L. V 0 max by pie was the average DC current. V 0 max by pie R L and we multiply it by twice V C C. That is V C C minus minus V E E, okay. Now we know everything. We know V C C is 15 volt, we know R L, we know V 0 max. Again we take either 15 or 14 point 8. I have taken 15 and it comes out as 71 point 6 milliwatt.

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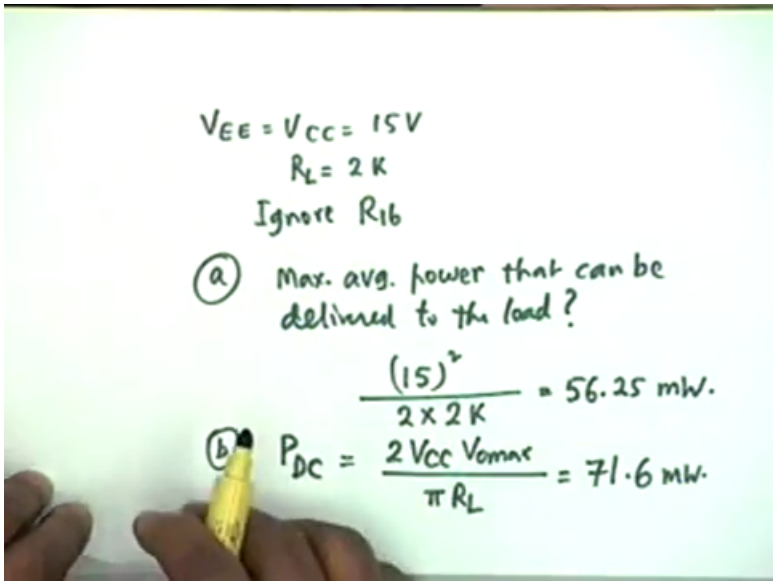

Can you see what the efficiency is? Eta C is therefore 56 point 25 divided by, yes, 71 point 6 multiplied by 100. Is this the correct figure? How much is this approximately? Approximately 75 percent, alright? That is not too bad because your maximum is 78 point 6 percent. This I guess is more than 75. no, it cannot exceed 78 point 6, alright. Okay. Last question. Pardon me.

Student: 78 point 56.

That is the actual value?

Student: Yes.

That is what I expected. I did not expect a large drop like 75. Why did not I expect it? Because we have calculated. Pardon me.

Student: 78 point 57.

78 point 57, okay, approximately 78 point 6.

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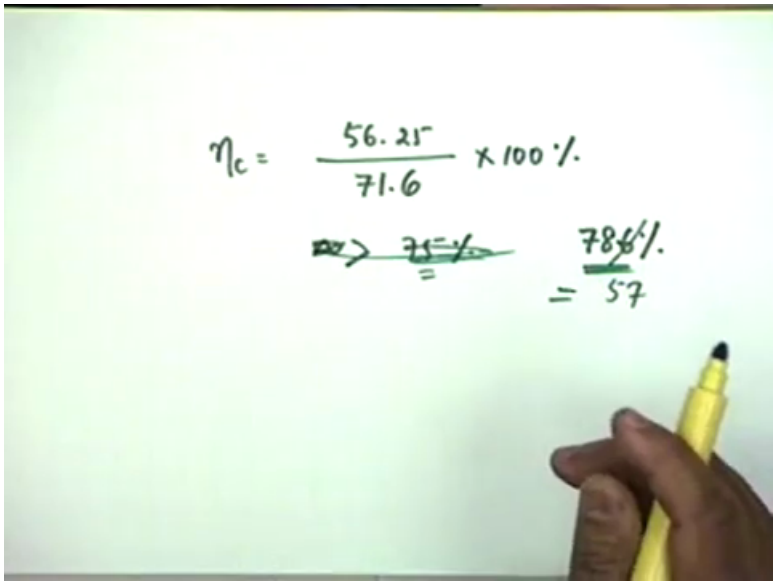

Now why I was fussy about this figure? Why I did not get satisfied with 75? Because we have calculated under the maximum possible swing. We even ignored V C E sat and then there is no reason why it should not come to 78 point 6 percent. It should be coming to pie by 4, alright. 78 point 57 is okay. It must be because of my rounding in the powers and all. Otherwise it should have been exactly 78 point 6. That is pie by 4.

The last part of the question. What was the last part of the question? Or I have not given you the last part of the question? No, I have not spelled out yet the last part of the question. Last part of the question is what is the smallest R L that can be used before the protection circuitry starts to operate? Smallest R L that can be used before the protection circuitry starts to operate.

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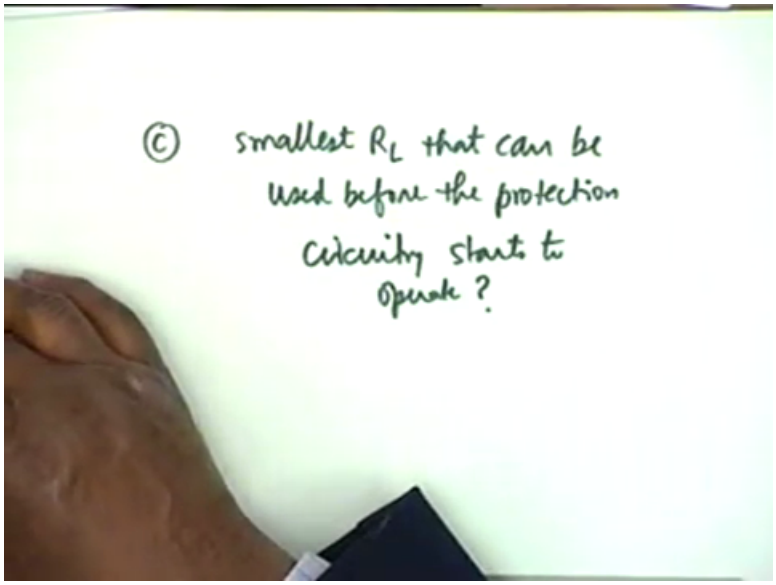

Now how do I attack this problem? To attack this problem we see that I sub C 21, that upper transistor that is limited. That is the maximum possible value that I C 1 can have, alright, to make Q 23 just on is given by V B E on that is point 7 divided by that is 25 ohms, okay. That is equal to 28 milliampere.

Student: Sir it should be point 5.

Alright, take point 5. If V B E on is point 5 you take in this figure as point 5. We can take point 5. If this is point 5 obviously this will be 25 milliampere, okay. Now if I C 1 is limited to 25 milliampere you cannot increase beyond that, obviously this must be equal to the maximum value of the load current I L m, agreed? So I L m is equal to 25 milliampere.

Student: Sir, I C 1 is 20 milliampere.

Oh! Okay, I stand corrected. So the maximum load current must also be 20 milliampere. Load current cannot exceed the maximum I sub C 21. And if this is the maximum load current then the minimum load R L min at which this will occur is given by V C C. Why V C C? Because

it is the maximum swing across the load. So V C C divided by I L max which is equal to 15 divided by 20 milliamps. That is equal to 750 ohms, is that right?

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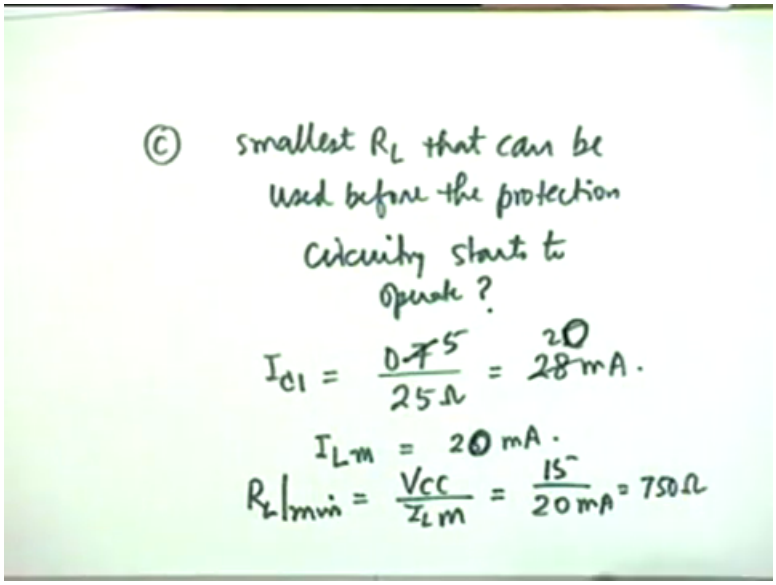

Milliamps 15000 divided by 20, 750.

Student: Sir now we should account for the drop in R 16 also.

Now we should account for the drop in R 16, okay. Let us go back. Good question. R 16 is 25 ohms so this swing cannot go to 15 volt. It must be 15 minus I L m multiplied by 25, is that clear? So this would be slightly less but the end justifies the means. We found out this minimum load to be 750 ohms. Obviously when R L goes below 750, suppose R L becomes (comprit) comparable with R 16 then obviously the efficiency would be decreased. Efficiency would be hard.

But on the other hand if R L minimum is much larger as compared to 25, 750 is 30 times and therefore this drop is negligible and the efficiency level is maintained. We are justifying in ignoring the drop in 25 ohms because the ultimate value that we get by ignoring this is 750.

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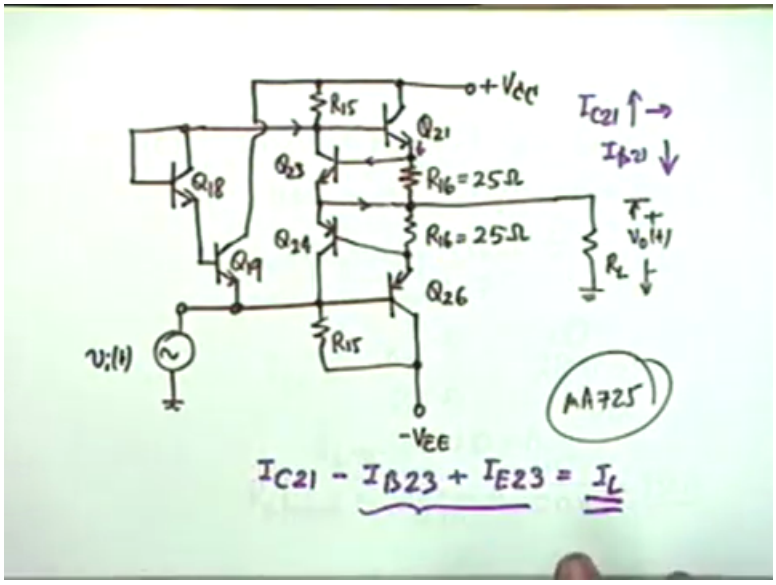

But suppose R L goes to 25 ohms or goes towards short circuit then obviously R 16 will consume the major power, alright, and the efficiency will go zooming down, okay. That is a good point to stop. I have given three interesting problems in the tutorial sheet which you should try to solve.