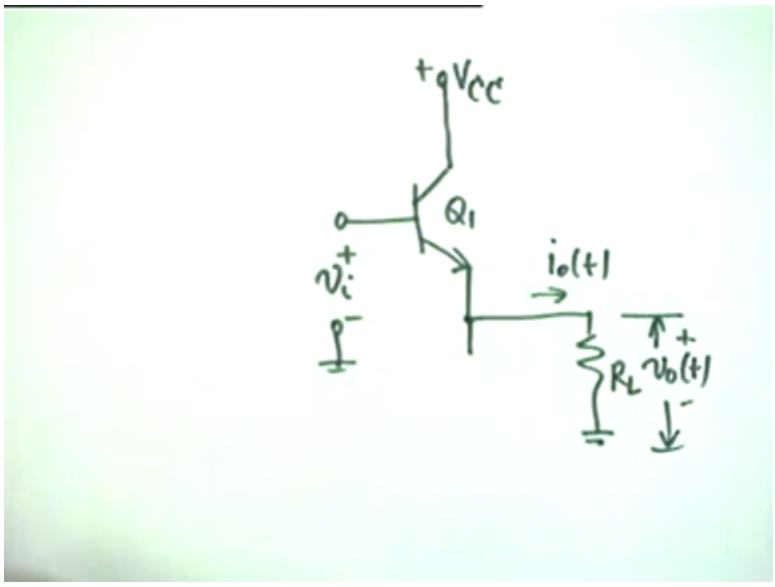
Analog Electronic Circuits
Professor S. C. Dutta Roy
Department of Electrical Engineering
Indian Institute of Technology Delhi
Lecture 27
Class A Power Amplifier: Efficiency Considerations

Today we are going to look at class A power amplifier and calculation of efficiency both in class A and also in class B and class AB under some idealized assumptions. If you recall the class A power amplifier circuit, a very simple circuit that was drawn yesterday with integrated circuits in mind. That is we used the minimum number of resistors and as many transistors as required.

We have a V i plus minus, the main transistor Q 1 which is operating in the emitter follower mode. That is the collector is connected directly to plus V C C and this emitter goes directly to the load R L. The voltage here is V 0 of t. We have gone back to the time domain and the current through this is i 0 of t.

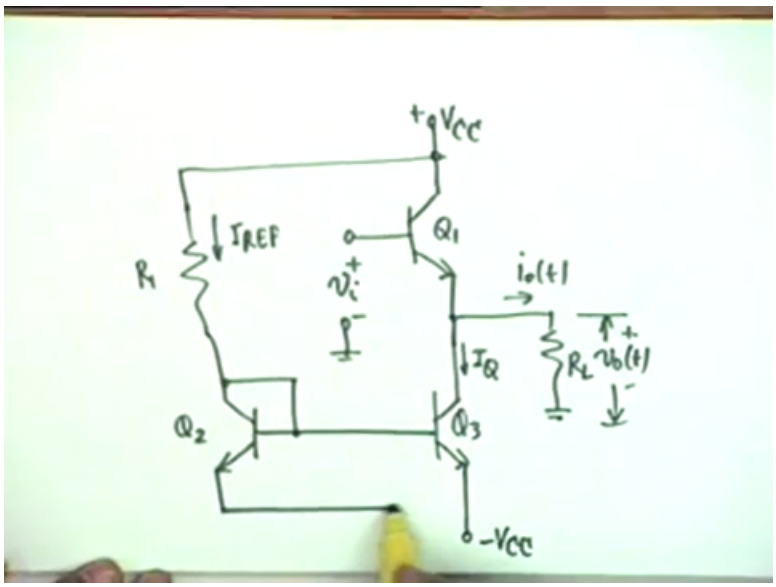
(Refer Slide Time: 01:56)



In order to bias the transistor we use another transistor in the current mirror mode. That is we use a Q 3 whose emitter goes to minus V C C and the current I Q of Q 3 is decided by the main transistor which is the current deciding transistor which we have called Q 2.

Its collector is connected to the base and this is connected to a resistance R 1. The current through this is I REF, the reference current and this naturally has to go to plus V C C, okay. This is the transistor and the emitter is connected to this.

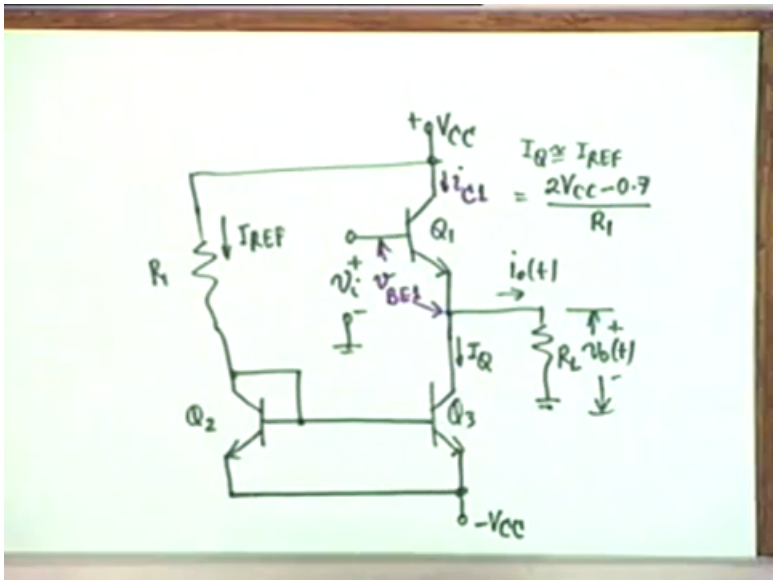
(Refer Slide Time: 02:57)



I have shown a simple current source but it could be a wiggler source depending on what value of I Q you want. If you want a very low as compared to I REF then you use a wiggler source, another resistance here, okay. Obviously I Q is approximately equal to I REF, okay. And this I REF is equal to twice V C C, yes, minus V B E on which we will use as point 7 divided by R 1, okay. This is the value of I Q.

Now in order to determine the transfer characteristic of the class A amplifier that is transfer characteristic is plot of V 0 versus V i. In order to determine that we take the total currents in total voltages. Let us called this current as I sub total current capital C 1. Small i subscript capital C 1 if you recall our terminology, I sub C 1. And then this voltage this will change with the applied signal. So this voltage will no longer called capital V B E but we call small v B E 1, the total voltage, alright.

(Refer Slide Time: 04:34)

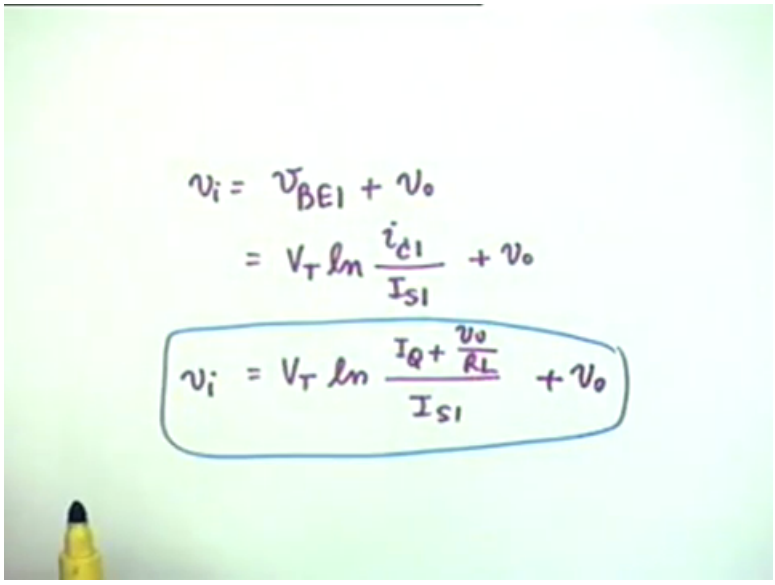


Then obviously the relationship is that V i is equal to v B E 1 plus V 0, agreed. Let us write this relationship that is worth 1000 words. This relationship as we will see V sub i is equal to v sub B E 1 plus V 0. If you recall the current versus base emitter voltage characteristics v B E 1 can be written in terms of I sub C 1 and the relationship is that this is V T log of the current I C 1.

Please be careful about the notation. It is the total current divided by I S 1, alright. Plus V 0, okay, V 0 and you also notice from this circuit that I sub C 1 if we ignore the base current that is if we consider beta to be very large compared to unity which we assumed throughout then I sub C 1 is obviously the sum of I Q and i 0, is not it right?

And i 0 is obviously V 0 divided by R L and therefore from these observations I can write this as V i equal to V T log of I S 1 and this can be written as I Q plus V 0 divided by R L plus V 0. If you see it carefully unfortunately this is my relationship between V i and V 0 and obviously it is a transcendental equation and it can be solved only by iteration, alright?

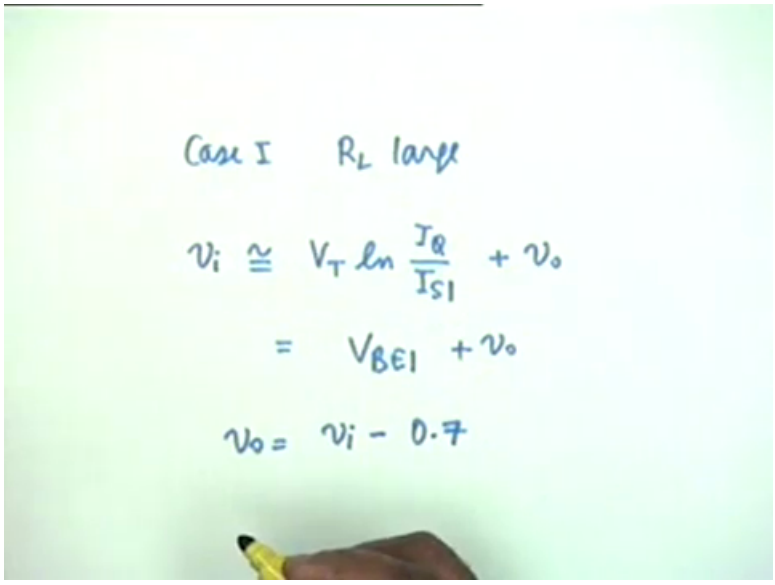
(Refer Slide Time: 06:26)



That is for a particular V i you assume a value of V 0, see if the right hand side is equal to the left hand side. If not, change it and go ahead doing it till you get a reasonably good approximation between the left hand side and the right hand side. Maybe the difference is of the order of 10 to the minus 4. The error criteria you have to decide yourself, okay. However for very large R L such that V 0 by R L can be ignored compared I Q, we can find an approximate relationship, okay.

So we consider a case, case 1 in which R L is large. If R L is large then obviously the relationship is V i approximately equal to V T log of I Q divided by I S 1 which is a constant now. We approximate this term which varies with V 0 by a constant plus V 0 and this obviously is V B E 1, the DC voltage across the first transistor between the base and the emitter plus V 0 which means that V 0 is equal to V i minus point 7 volt, our usual relationship that we got in class B also. It is the same relationship, okay.

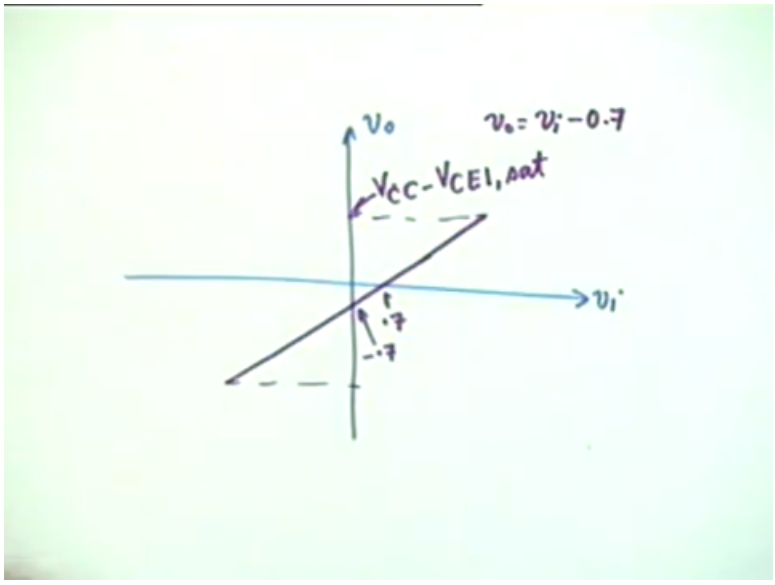
(Refer Slide Time: 07:53)



And therefore for large load where V 0 by R L can be ignored compared to the quotient point current I Q, I Q was established not by load line but by a current mirror, okay. Now this relationship obviously is very easy to plot. We shall have when V i equal to point 7, the output voltage is 0. V i, V 0. V 0 is 0 when V i equal to point 7 which means that the characteristic would be something like this. It will have an offset here. This voltage would be point 7. What would be this voltage? When V i is 0 it should be minus point 7, okay.

So you know these two lines and then the relationship is V 0 equal to V i minus point 7. So the slope would be unity however it does not go indefinitely because the maximum output voltage and the minimum output voltage they are both limited. What is the maximum that is permitted? V C C minus V C E 1 sat. There is a reason why I am saying V C E 1.

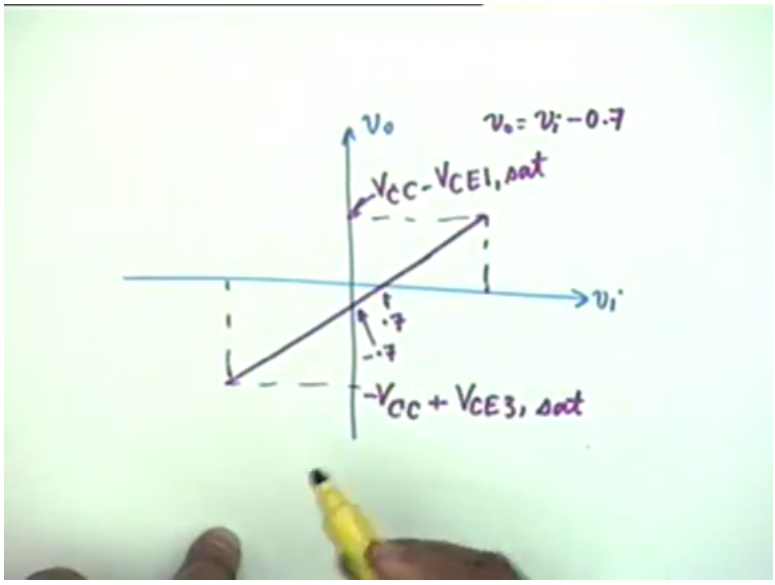
(Refer Slide Time: 09:22)



Let us look at the circuit. This voltage the maximum that can happen is in the positive side is plus V C C minus the voltage up here. On the other hand on the negative side the minimum value when V 0 is negative the minimum value that can occur is minus V C C plus V C E 3 sat. Is the point clear? Okay. So we have found out what the minimum is. Minus V C C plus V C E 3 sat. It is therefore important.

You see even with these symmetries, even with these lower limit and upper limit the swing is not symmetrical because it does not pass through the origin. Do you not see that? But it is class A operation. Class A why do we refer to class A? In order to reduce the distortion as much as possible therefore we shall never go to saturation. But theoretical limits of the maximum positive swing is V C C minus V C E 1 sat, your input voltage. What is the input here? Input voltage is this plus point 7. Similarly this voltage would be this plus point 7, okay.

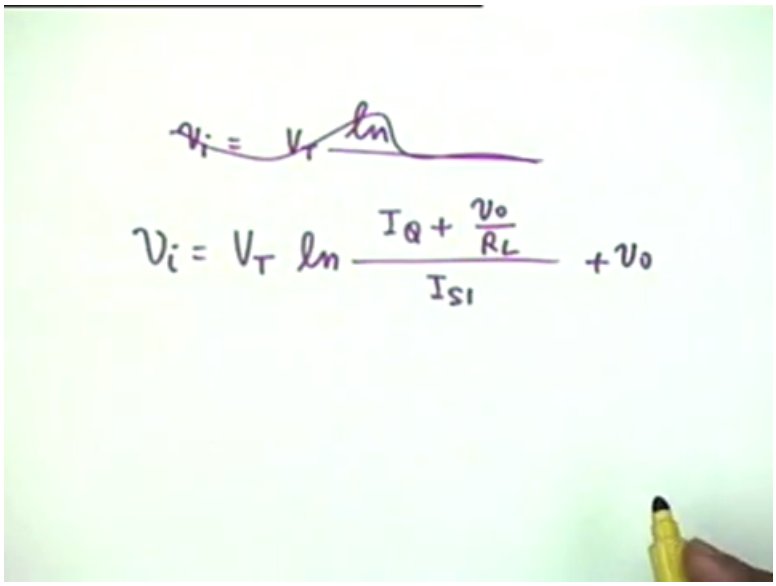
(Refer Slide Time: 10:52)



So you know the input voltages. The input voltage must not exceed these two values either on the positive side or on the negative side. You must be well within these limits. This figure only shows the limits, okay. You should not operate the transistor so that the peak swing goes here because then you are asking for distortion. You can as well go to class AB or class B amplifier, okay.

Class A amplifier is for low power level and very little distortion, okay. However if we go back to the relationship, what was the relationship? V i was equal to V T log of I Q plus V 0 divided by R L that divided by I S 1 plus V 0. This is our exact relationship, the transcendental.

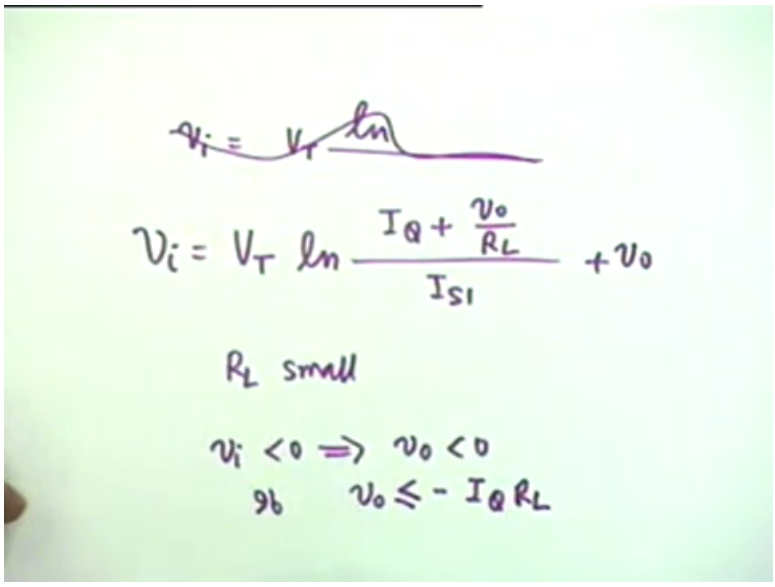
(Refer Slide Time: 11:58)



Now a problem arises when R L is small. When R L is small in the previous case we considered R L large so that the first term could be approximated by a constant, then the task was easy. When R L is small and these two terms are comparable to each other then the problem arises because when V i is negative, V 0 will also be negative. It is an emitter follower after all.

V 0 will also be negative and there is a possibility that this term may go to 0 or negative. Is that clear? So when V i is less than 0, V 0 less than 0 and if V 0 is less than or equal to minus I Q R L what will happen? This term cannot be found out.

(Refer Slide Time: 13:05)



Physically what will happen? Physically suppose V 0, let us consider this point. V 0 equal to minus I Q R L. Under this condition this will be 0, log of 0 would be minus infinity and therefore V i would be minus infinity and infinite negative voltage is required. Obviously this does make sense. There must occur something physical. If we look at the circuit what will happen? Pardon me. Say it loud even if you are saying it wrongly. How does it matter?

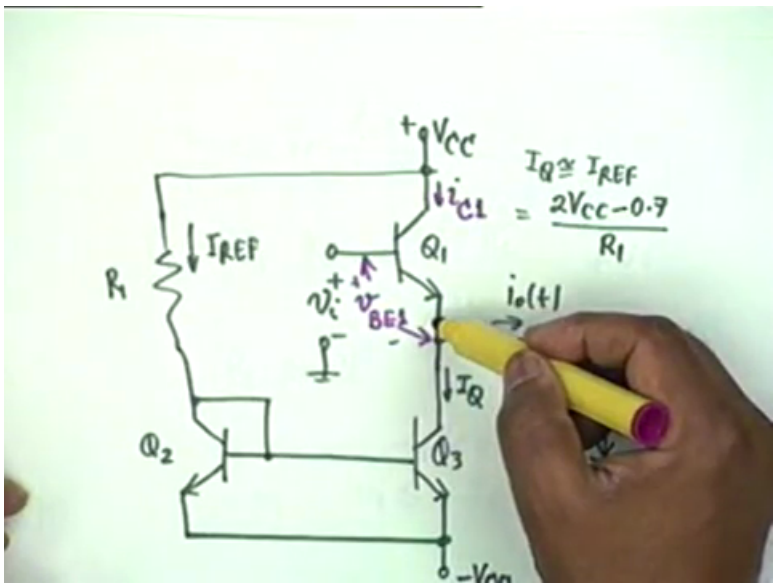
Student: Q 1 will cut off.

Q 1 will cut off. Why? That is a good answer. Why? Yes, what was the question?

Student: I could not understand that if V i is negative how can V 0 be negative?

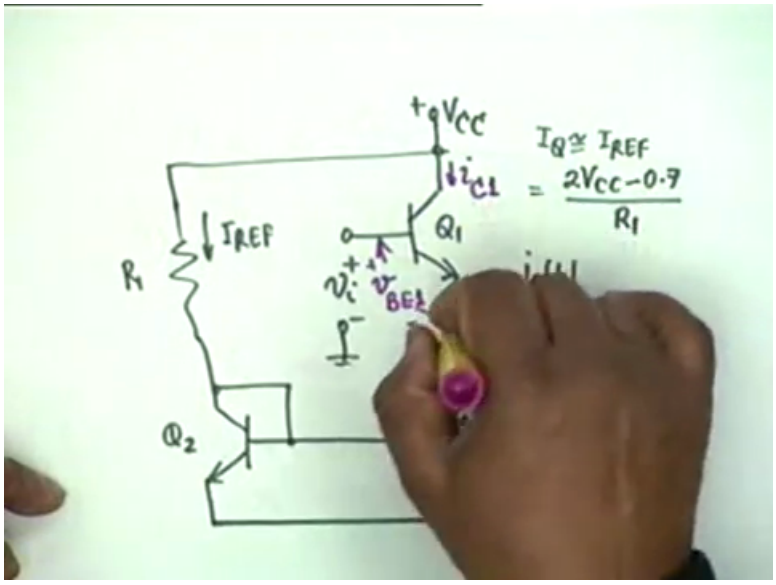
Because it is an emitter follower basically, is not it right? The collector is connected to plus V C C and therefore whatever voltage appears should appear here except for this drop, agreed, okay.

(Refer Slide Time: 14:13)



Now if V 0 is equal to minus I Q R L, what does it mean? V 0 is i 0 R L which means that i 0 is actually in this direction and the actual current would be I Q here, right? When V 0 equal to minus I Q R L this must be the direction of the current, agreed? So I Q comes like this and flows like this. In other words nothing flows through Q 1. So Q 1 goes into cut off, not saturation. Q 1 goes into cut off. Saturation it flows a current. But if it does not give a current, if it does not contribute to a current at this junction means it is cut off.

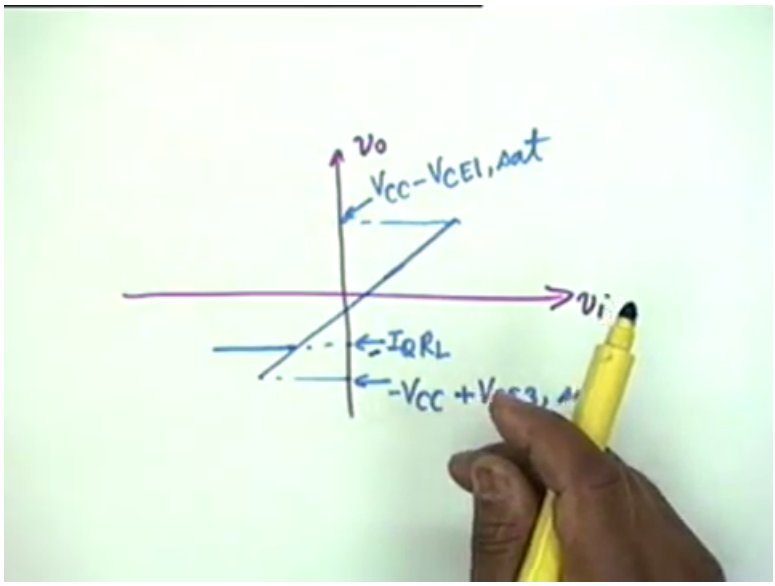
(Refer Slide Time: 15:02)



So physically much before this inequality starts affecting the circuit Q 1 shall be cut off which means that if we plot V 0 versus V i well we will have a plot like this. I am showing it a straight line. It will not be a straight line because there is a logarithm involved. It is a transcendental equation but it is very nearly a straight line . It is not exactly a straight line.

While the upper limit is still set by V C C minus V C E 1 sat. The upper limit the maximum positive voltage, maximum positive value V 0 is still set by this. The maximum negative voltage will be set much before that at the level minus I Q R L. The absolute minimum that is possible is minus V C C then plus V C E 3 sat. That we have already seen but what happens is before that I Q R L puts Q 1 off and if Q 1 is off then no amplification, alright, okay.

(Refer Slide Time: 16:34)

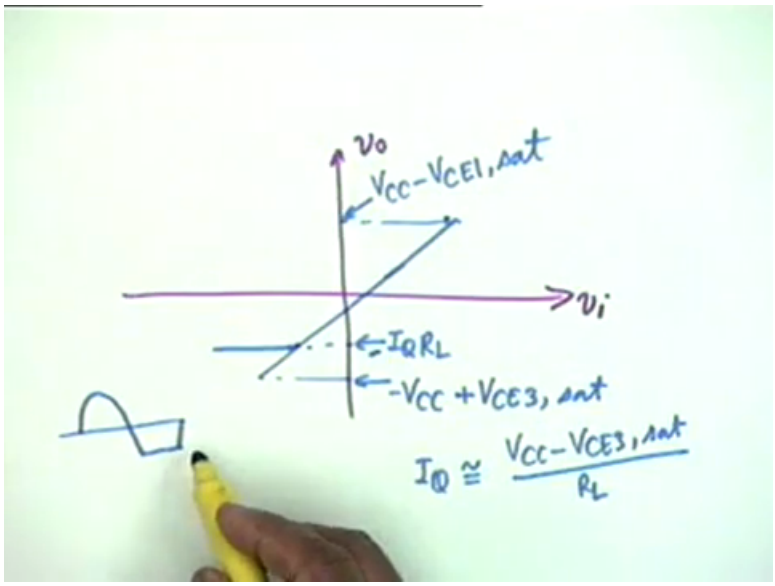


So in the case that R L is small, one has to be careful. The swing in the negative direction would be limited unless, now this also shows you a design criteria. What should be your design criteria? Design criteria if you want as large a swing as possible, since I Q R L is limiting your swing and R L is given, R L is not your choice, R L is known and therefore you have to design your current mirror such that I Q is approximately equal to V C C minus V C E 3 sat divided by R L. Do you understand this? You have followed this?

This picture clearly shows a design criteria that if you want as large a swing as possible, you have to take care of the negative swing. Positive swing will occur automatically because I Q plus V 0 by R L when V 0 is positive is positive. There is no problem but when V 0 exceeds minus I Q R L then obviously Q 1 goes into cut off and therefore your I Q should be approximately equal to V C C minus V C E 3 sat divided by R L.

Then we shall get an approximately equal possible swing in the positive as well as negative direction without distortion. It is not that you cannot apply a large input voltage but its negative swings will be clipped. Your wave form if it is this situation and if you have driven the transistor to insanity which means saturation on the positive side and beyond this saturation, beyond cut off in the negative side what you will get is your output waveform would be like this, agreed? Highly distorted because cut off at minus I Q R L.

(Refer Slide Time: 18:41)



If you want to restore this obviously you will have to go back and redesign your current mirror such that I Q approximates this. Point clear? We will have problems on this later to be

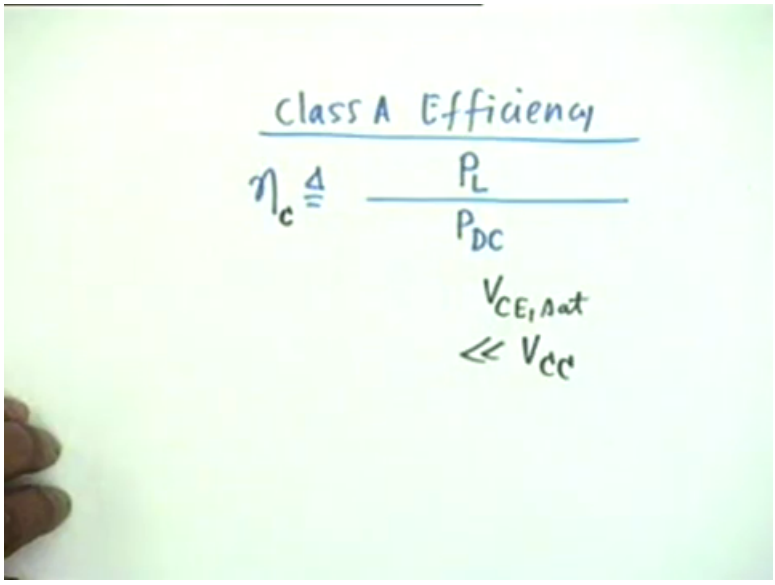
worked out, okay. With all these now let us look at the efficiency that a class A power amplifier can give. Efficiency as I already told you is defined as the P L average load power. The load power will be a function of time V L V 0 t multiplied by i 0 t. You have to take the average value over one cycle.

You are basically asking for undistorted amplification so one cycle of sin wave is good enough. Divided by the DC power that is supplied by the battery. And as I had told you earlier this DC power is mostly dissipated in the output transistors and therefore if you calculate the dissipation in the output transistors that is good enough. Or the other way is take the supply and connect an emitter there, DC emitter. The supply multiplied by the DC emitter that will be P D C.

If you want to emphasize that the power is being dissipated only at the collector then one sometimes uses the symbol eta C and calls it collector efficiency which means that the actual efficiency of the amplifier, power efficiency would be less than the collector efficiency because in collector efficiency you are not taking care. You are only taking care of collector dissipation you are not taking care of the other transistor, the current mirror transistor for example, okay.

In any case we shall ignore all other transistors. We shall also ignore in our calculation very conveniently V C E sat. We will assume that V C E sat is much less than V C C. It is true in practice, 15 and point 2 and therefore it can be ignored. That will keep our calculations simple.

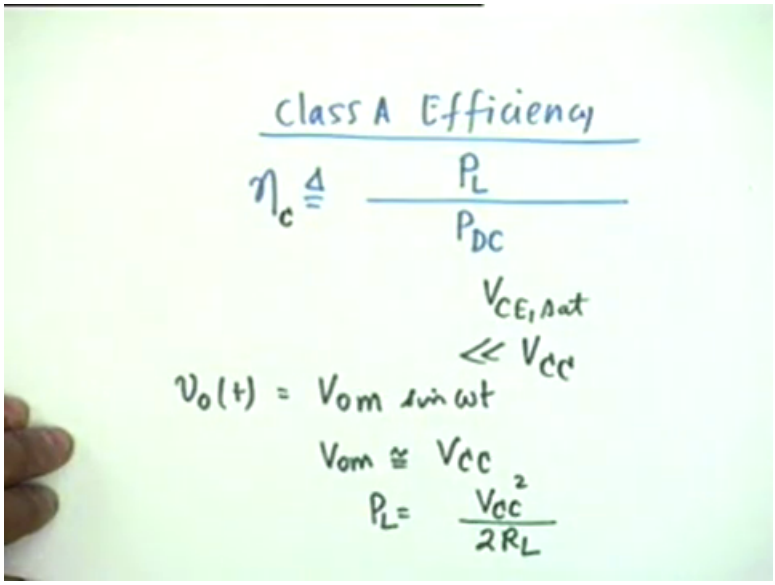
(Refer Slide Time: 21:07)



Now suppose in the class A amplifier I Q R L has been so selected that V 0 t is equal to V 0 m, the maximum value multiplied by sin omega t. And V 0 m that is the transistor has been driven to its maximum possible swing then V 0 m would be approximately equal to what? V C C because we are ignoring V C E sat, okay.

And therefore if you have a sinusoidal voltage V C C sin omega t across a load R L then what is P L? P L is V C C peak value is V C C so root mean squared value V C C by root 2, square of that divided by R L. So it would be V C C squared by 2 R L, agreed?

(Refer Slide Time: 22:16)

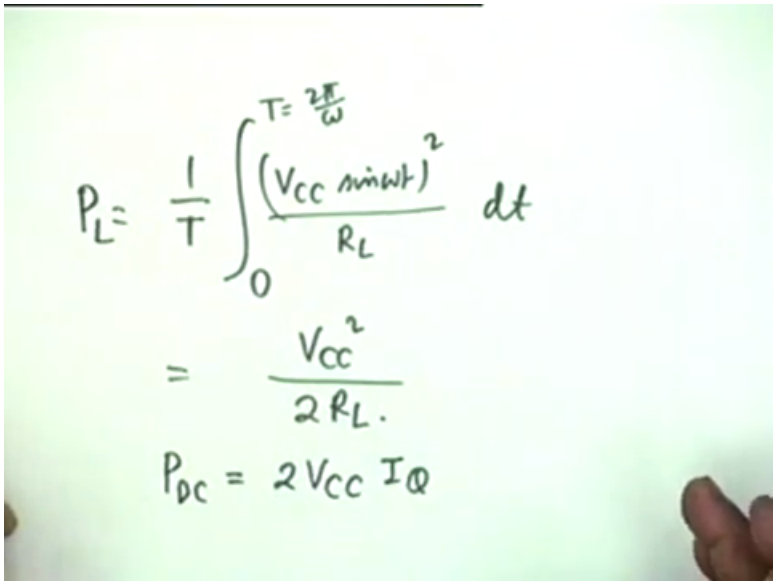


If you are not convinced you calculate it out like this. V C C sin omega t whole squared divided by R L is the instantaneous value integrates from 0 to capital T. Capital T is 2 pie by

omega and divide by capital T. This is P L and you can verify that this is equal to V C C squared divided by 2 R L.

Now what is the DC power supplied by this source? The effective source is twice V C C and the quotient current is I Q. We are ignoring all base currents, okay. The average current, the DC flowing through Q 1 Q 3 combination is I Q. So P D C must be twice V C C I Q, very simply, okay.

(Refer Slide Time: 23:13)



And therefore the efficiency eta which is the ratio of the two is simply 1 quarter V C C by I Q R L. You know let us multiply this by 100 so on a percent. You know that you have to adjust I Q, you have to design I Q such that I Q R L is approximately equal to V C C. V C C minus V C E 3 but we are ignoring that and therefore eta max is only equal to 25 percent, maximum efficiency. Therefore every watt you have to be prepared to supply 3 watts, 4 watts.

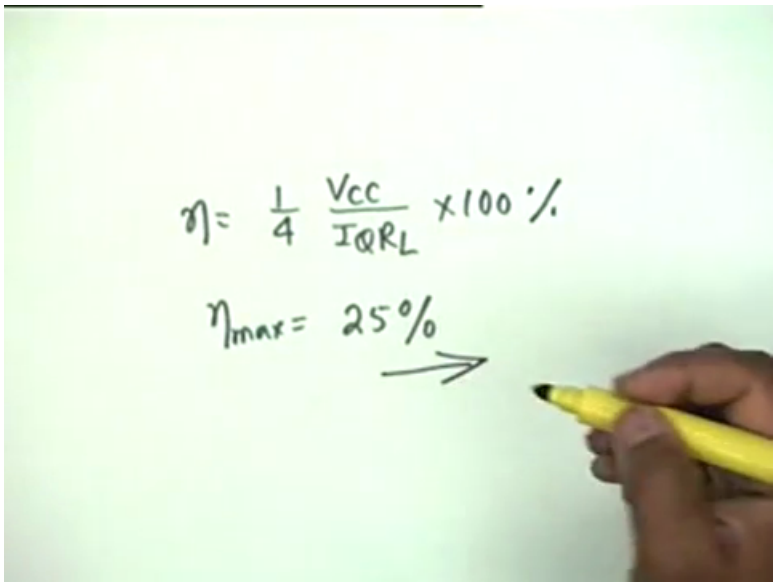
Every watt of load power you have to be prepared to supply 4 watts and 3 watts are wasted. Where? Obviously in the transistors and you must allow for dissipation of these 3 watts that is wherever these output transistors are either you have to supply a cooling fins or you have to physically force cool air into them, okay. So that is the story. Class A therefore is very inefficient and I had told you that class B and class AB is resorted to when you want a higher efficiency.

And the reason for higher efficiency in class B or class AB should be clear that there is no quotient current or the quotient current is very small. You see V B E is kept at point 7 or

minus point 7 in the PNP. Then the transistors are on the onset of conduction. So the Q point in the absence of the signal, the DC that flows through Q 1 and Q 2 in the class AB amplifier is very small and therefore the quotient power dissipation is approximately 0. Power dissipation however occurs when there is a signal.

Why? Because each transistor conducts only for half the cycle. Each transistors acts as a half way rectifier and half way rectifier waveform has a DC and therefore that is a dissipation and we will show now that this efficiency in class B can be increased to 78 point 5 percent. You see the increase it is approximately pie by 4 percent.

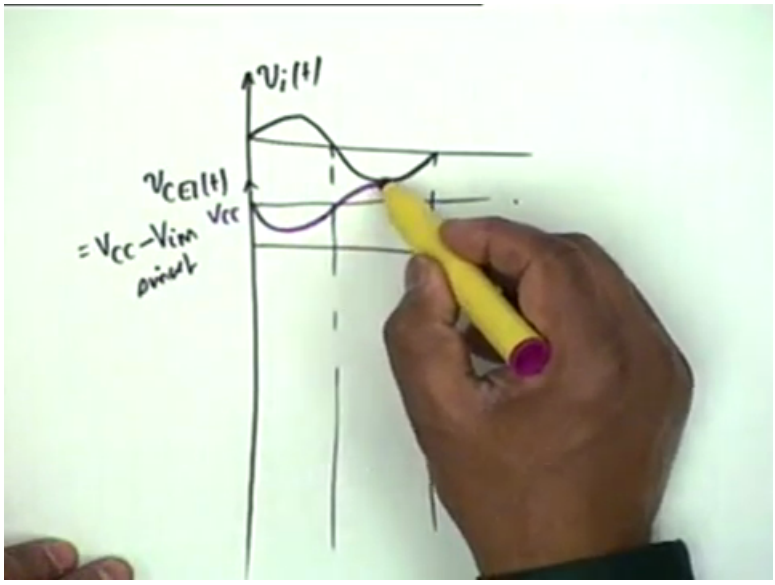
(Refer Slide Time: 25:41)



We will see how this comes about. But before that let us look at the power distribution in class A amplifier, okay. It is instructed to draw these diagrams. Let us say my V i t is of this form. I am drawing only one cycle. Draw these vertical lines. Suppose this is V i t then V C E 1 t would be V C C minus V 0 t, okay.

V C E 1 t, collector emitter drop if you recall the circuit, would be V C C minus V 0 of t. But V 0 is approximately equal to V i if you ignore that V B E 1 so it would be of the form V C C minus let us say V i m sin omega t which means that if this is the level V C C then to start with V C C minus V i m sin omega so to start with it will go negative, agreed? And then it will go positive like this.

(Refer Slide Time: 27:33)



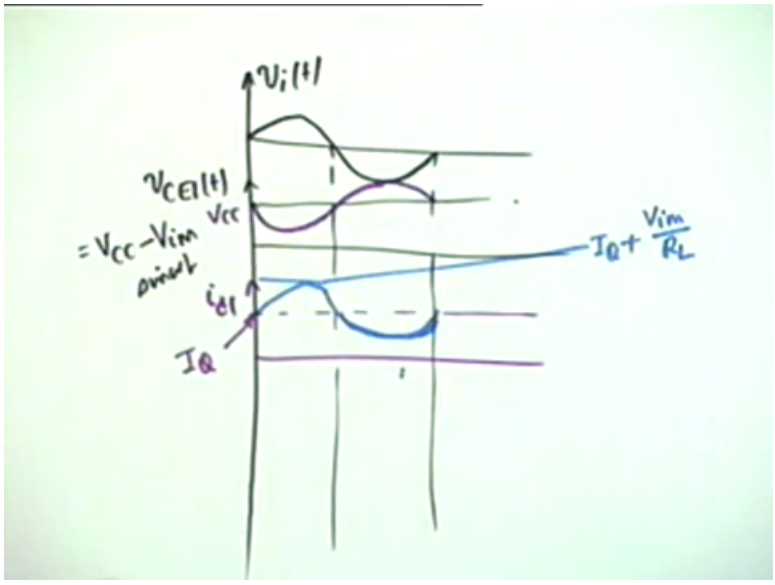
The maximum value here would be V C C plus V i m and the minimum value would be V C C minus V i m, is the point clear? Okay. If superimposed on V C C we are not assuming that V i m is equal to V C C that means we are assuming that because it is a class amplifier it is not driven to the maximum. We will see what happens when it is driven to the maximum.

So the minimum that it can come to is 0 and the maximum it can go to twice V C C, agreed? That is the absolute maximum possible for V C E 1 t, okay. As far as the current is concerned I sub C 1 that will also be sinusoidal about what value? What is the average value of I sub C 1? What is the average value?

Student: I Q.

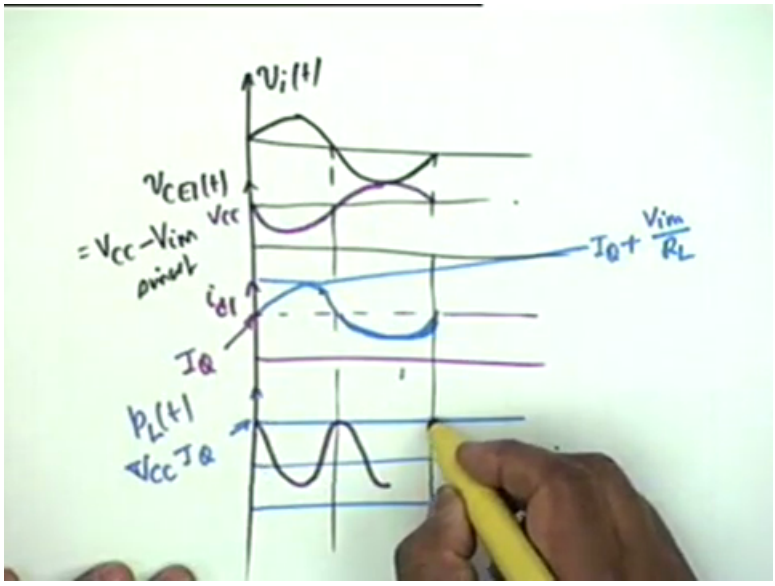
I Q and therefore now current waveform would it follow? Would it be like this? In phase with V i or out of phase? That is very simple. When the input increases, the current increases. When the base drive increases, the current decreases. So it is like this. Sorry, it is sinusoidal. The maximum is I Q plus i m and what is i m? What is this maximum value? I Q plus V i m divided by R L, agreed? V 0 m is approximately equal to V i m and the minimum value is I Q minus V i m by R L, alright?

(Refer Slide Time: 29:27)



My drawings are not very good but you should take this with a pinch of salt, okay. Then the power P L t, the load power obviously shall be the multiplication of the black waveform and the blue waveform or you could simply square this and divide by R L, alright? In any case it would be something like this. It is V C C I Q, this is the maximum value say it starts from here V C C and I Q then it goes down like this, goes down like this and comes like this.

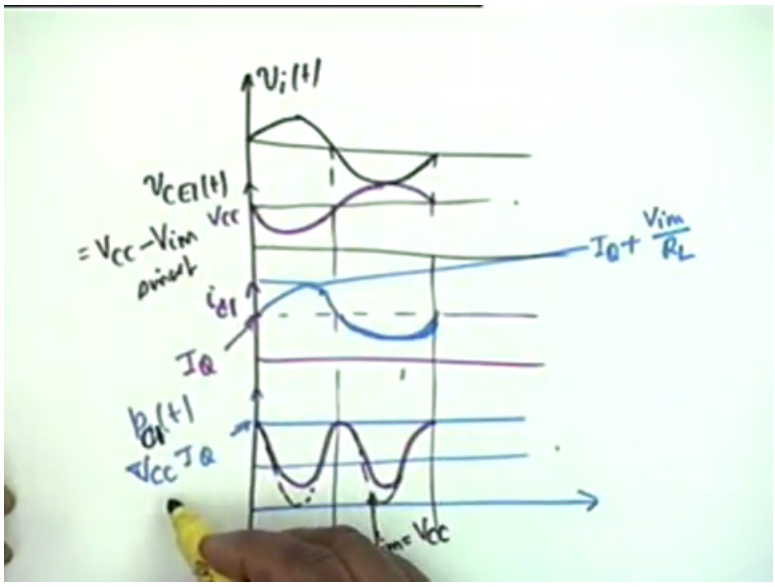
(Refer Slide Time: 30:23)



This is the power which is simply the square of this curve, alright, divided by R L, agreed? Now the power curve P L t can reach a minimum value of 0. That is I might be able to come, let me use some other colour, I might be able to come up to this under what condition? Pardon me, V i m is equal to V CC, alright.

And under this condition that is when the class A amplifier is driven to its limits you can show very simply that. I made a mistake. This is not P L t. This is P C 1 t. This is the power dissipated in the collector. V C E 1 t multiplied by I C 1, okay, so I made a mistake here.

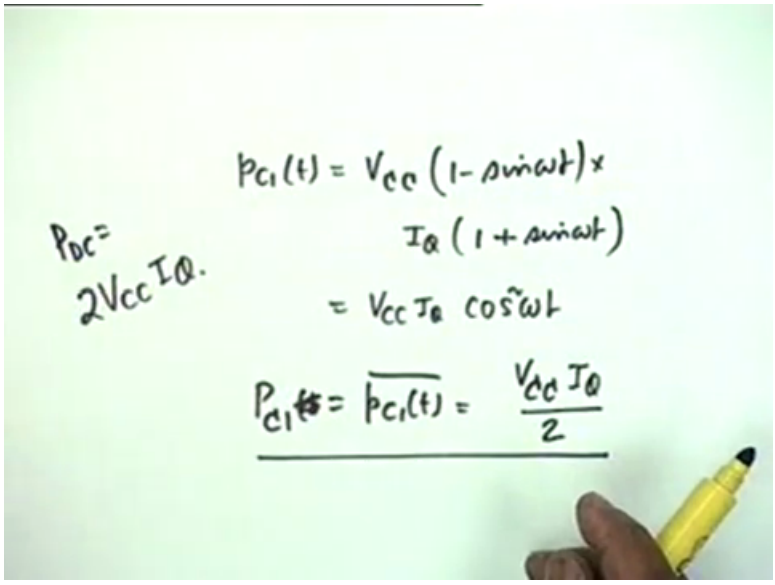
(Refer Slide Time: 31:36)



You can show that when the transistor is driven to (satura) its limits then V C E 1 t is simply V C C 1 minus sin omega t, agreed? V i m becomes equal to V C C multiplied by I Q then 1 plus sin omega t. The maximum value would be equal to I Q, agreed? When the transistor is driven to its limits, let me look at this, this minimum will come to 0 and that can happen when i m the maximum is equal to I Q, okay. So this is V C C I Q multiplied by 1 minus sin squared omega t which is cosine squared omega t.

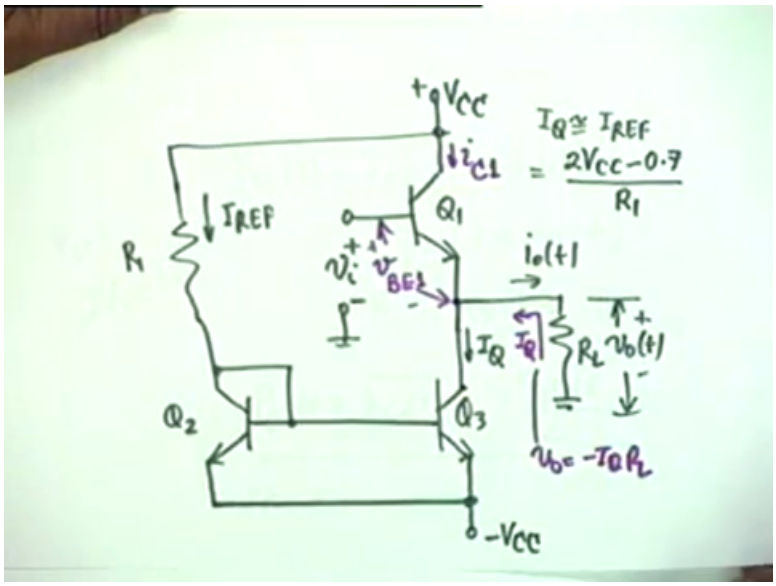
And if you take the average value of this P C 1 which is p C 1 t average, if you integrate this with respect to t and divide by capital T what do you expect what would be the value? V C C I Q divided by 2, alright? Whereas what we have found out is that the total power supplied P D C is equal to twice V C C I Q. So where are the other components? We have found out the dissipation in Q 1, average dissipation in Q 1 is this V C C I Q by 2.

(Refer Slide Time: 33:25)



I require another 3 V C C I Q by 2 to be able to get this figure. Where are the others? What does Q 3 dissipate? P C 3, what does Q 3 dissipate? The current is a constant I Q and the voltage across it is average voltage V C C, is not it right? If you look at the circuit, let us go back. I have lost it. Here you see the voltage across Q 3 the average voltage is V C C, is not it right? Because this voltage is a fluctuating sinusoidal voltage. The average value of this voltage is V C C. The average current is I Q and therefore the dissipation in Q 3 is equal to V C C times I Q.

(Refer Slide Time: 34:27)

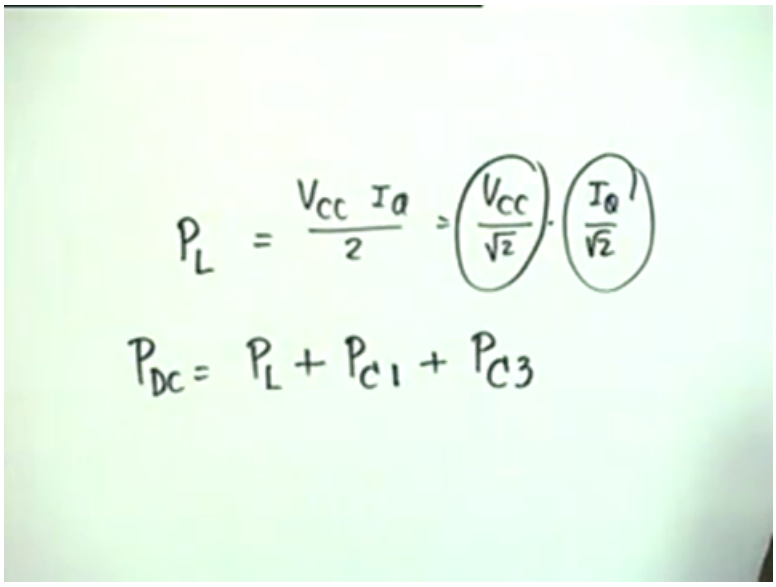


So P C 3 is V C C I Q. Now I have been able to get 3 V C C I Q by 2. What about the other one? Load power that is correct. What I missing is V C C I Q by 2 which I can write as V C C divided by root 2 multiplied by I Q divided by root 2. This is the RMS value of the load

voltage and this is the RMS value of the load current and therefore this is equal to the load voltage.

And indeed P D C is equal to P L the load power plus the power dissipated in the transistor Q 1 plus the power dissipated in the transistor Q 3. And that checks. This is only to give you a physical picture of how the power is being distributed, distribution of power.

(Refer Slide Time: 35:25)



Now let us look briefly at the class B amplifier. If you recall we will ignore crossover distortion, alright? We will ignore crossover distortion and we will also ignore V C E sat, is it convenient? Yes.

Student: Sir, we find out that the maximum power dissipation 50 percent is in the transformer Q 3 in this case, transistor.

Transistor Q 3. That is correct.

Student: Sir is there any major implication of this?

Any major implication? Well it has to be designed to.

Student: Sir, can I reduce this to anything?

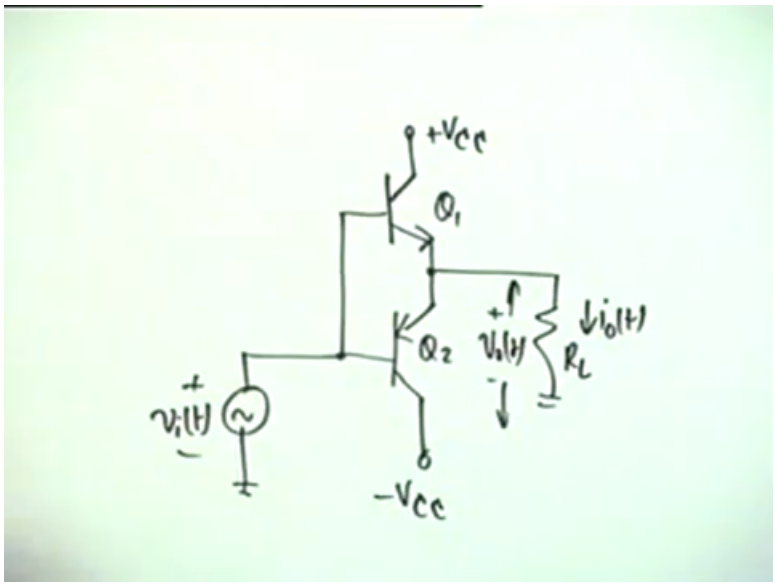
Yes there are modifications but then what you do is you distribute it somewhere else. You see the point that is making is that Q 3 dissipation V C C I Q it is double the power dissipation of transistor Q 1. But you see in the worst case Q 1 also has to be prepared to dissipate V C C I Q. But during the operation when there is a signal transistor Q 3 dissipates twice the power

that transistor Q 1 dissipates. And transistor Q 3 has to be more robust. There is the implication.

Now what we can do is transistor Q 3 can be replaced by 2 in parallel. Then the power is split or the circuit can be modified so that this power dissipation is shifted somewhere else, is distributed, okay. Nothing else can be done because class A is class A and the maximum is 25 percent. For every watt load power you have to be prepared to dissipate 3 watts. It is unfortunate that the main transistor or it can even be fortunate because the current mirror may be added externally if it goes off. But the main transistor still remains.

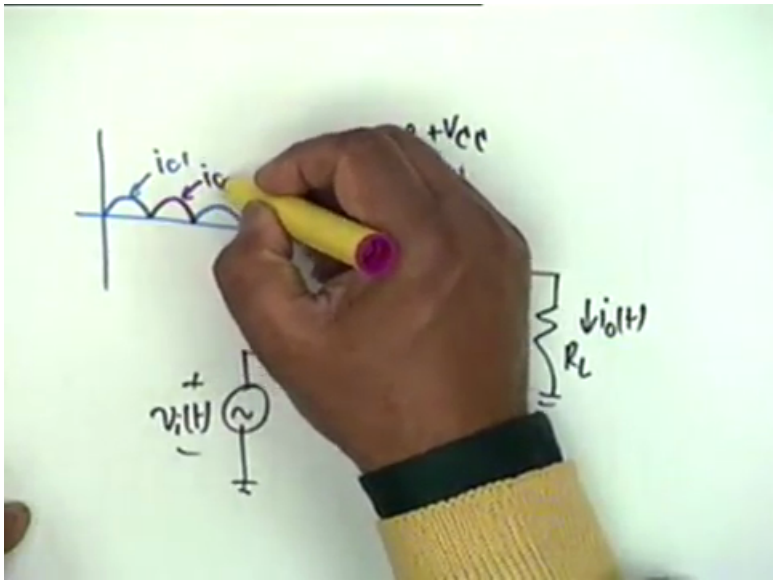
Well it is a matter of opinion. But let us look at class B. As I said we ignored crossover distortion, we also ignore the V C E sat. This is for convenience in calculation. This is the transistor Q 1, then we have a transistor Q 2 which is a PNP transistor and this voltage is minus V C C. The power goes from here to R L. This is i 0 t and this is V 0 t, very simple circuit. The two bases are connected together and this voltage is V i t, okay.

(Refer Slide Time: 38:14)



Now to have a picture of what goes on, okay, let us call this as i sub C 1 and this current as i sub C 2. Then you know that i C 1 will take care of the positive half of the load current and i C 2, the negative half of the load current. So if I plot i C 1 it would look like this, okay. This is i c 1 whereas i c 2, I have taken care of the direction, i c 2 would be in between ones, is that okay?

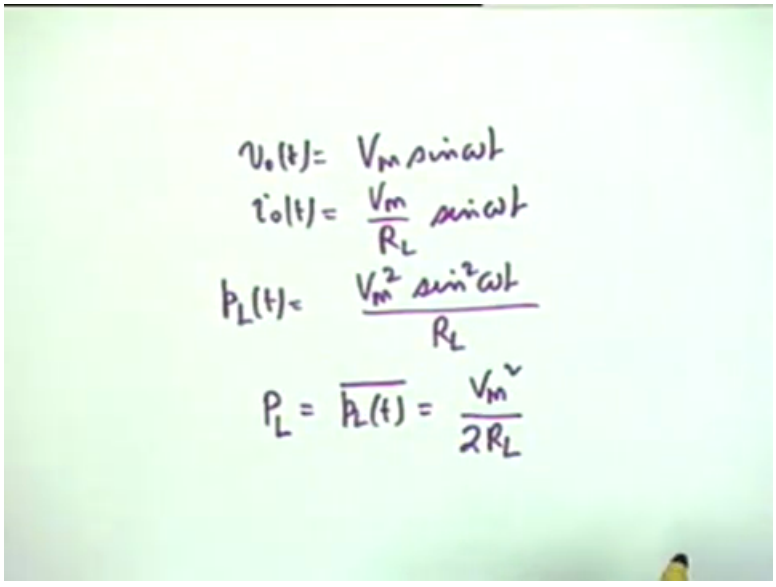
(Refer Slide Time: 39:08)



I C 2 are the negative half but the directions i c 2 comes like this so the load current is in the opposite direction. They help the load current to remain sinusoidal, okay. And I think that is all the picture that we need. Let us go into the calculation. Suppose the V 0 t is suppose V m sin omega t, alright? Then i 0 t would be equal to V m by R L sin omega t. It is a resistive load, agreed?

So p L t would be simply V m squared sin squared omega t divided by R L and the load power which is the average value of p L t would be simply average value of sin squared omega t is half, so it would be V m squared by 2 R L. We could write this term without going to the average value because if this is the voltage across the resistance R L, the power dissipated is V m squared by 2 R L, okay.

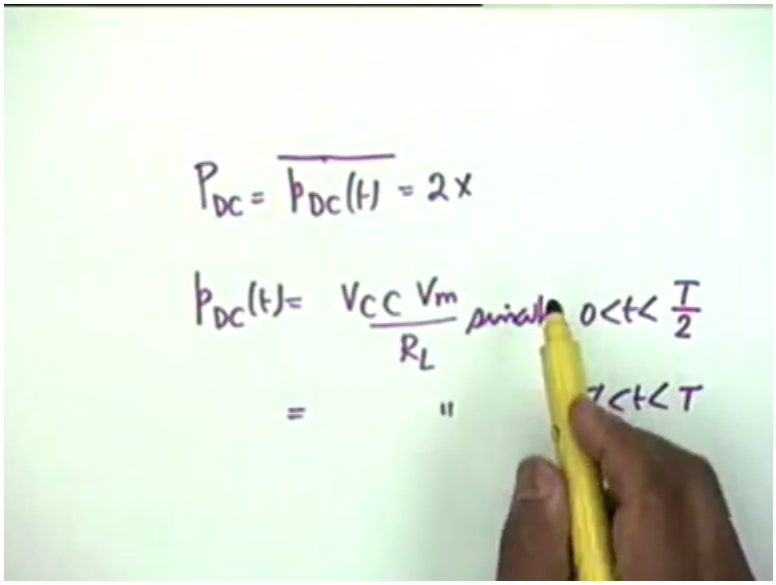
(Refer Slide Time: 40:36)



Now what about the DC power supply P D C. P D C which is equal to small p D C average, okay. Let us see what is small p D C t? When Q 1 conducts what is small p D C? V C C multiplied by the load current which is V m by R L sin omega t, is this point clear? When Q 1 conducts Q 2 does not. The drop is V C C and this is the load current and this is for 0 less than t less than capital T by 2.

And when Q 1 does not conduct, Q 2 conduct, the instantaneous power expression is the same, okay. So this would be T by 2 less than t less than capital T. In other words the P D C which is the average value of small p D C would be twice the average value of this expression, okay, over half the period, 0 to t by 2.

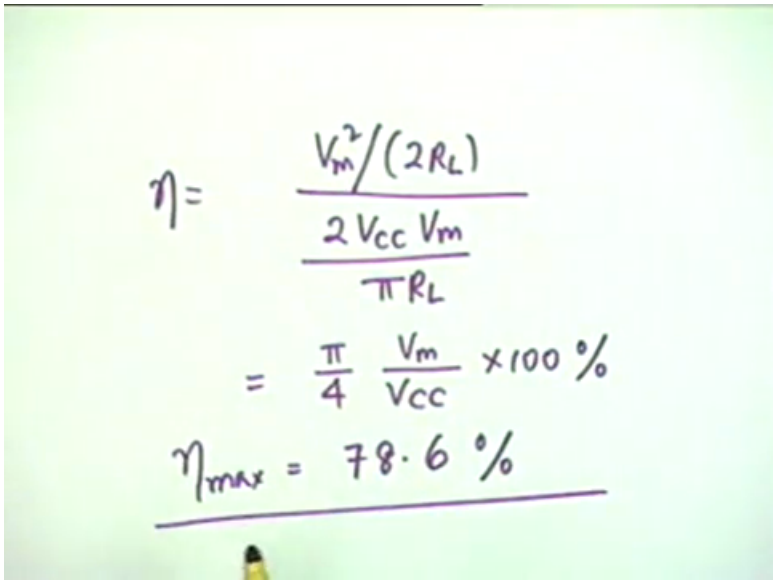
(Refer Slide Time: 42:17)



What is the average of sin omega t over half the period? So it would be 2 V C C V m divided by pie R L, is that clear? The average value of sin omega t over half the period is 1 by pie and I multiply it by 2. Why? Because there are two half periods. To make one complete period there are two half periods and therefore I can now find out my efficiency.

My efficiency would be P L is V m squared divided by 2 R L and P D C is twice V C C V m divided by pie R L and this works out to pie by 4 V m divided by V C C multiplied by 100 percent, okay. And you also know that the maximum swing that is possible at the load is V C C. V m, absolute maximum is V C C therefore eta max is pie by 4 which is 78 point 6 percent.

(Refer Slide Time: 43:38)



That is the major advantage of a class B amplifier. That is for every watt of power to be dissipated in the load you have to be prepared to supply how much? 1 point?

Student: 1 point 3.

Approximately, no it is less than 1 point 3. 1 minus point 786, okay. 1 point 214, okay, so many watts. This is the major advantage of a class B amplifier. Now in the subject of power amplifiers the quality of a power amplifier whether it is class A, class B or class AB are determined by two parameters, okay. Just like a voltage amplifier you require A v s, R i and R 0.

In a power amplifier the impedances are not of consideration because in most of the power amplifiers it is a (amp) common collector for an emitter follower circuit. Emitter follower circuit is characterized by high input impedance and low output impedance. So it is eminently suitable for power amplification because who is feeding a power amplifier? The voltage amplifier and who is taking power? A small load maybe a loudspeaker, okay.

So input and output impedances are of no consideration. What is of consideration is efficiency. How good a power amplifier is depends on how much power you waste. How much power you can deliver to the load and how much power is delivered by the supply. The other parameter is the so called THD. All stereo amplifiers have this specification, total harmonic distortion. And this is defined as follows.

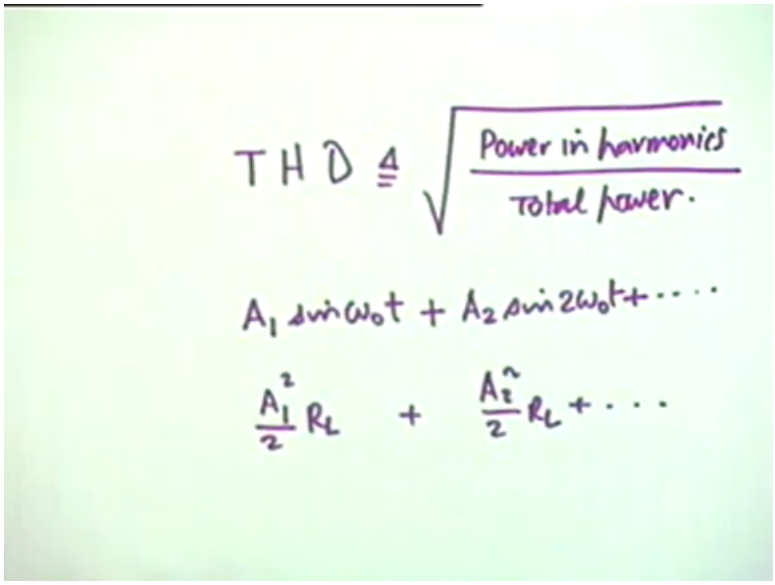
It is defined as the square root of power in harmonics divided by total power. It means what we want across the load is let us say a voltage or a current of the form A 1 sin of omega 0 t. If

omega 0 is your input frequency this is what we want across the load. Unfortunately due to large excursions there comes nonlinearities and we get let us say A 2 sin of 2 omega 0 t plus etc. We get the higher harmonics.

Harmonics means frequencies are integral multiples of the fundamental frequency and therefore if this current flow through a load then it would be square of this multiplied by the load R L. And you know that if you have a sum of currents of different frequencies flowing through a load R L then the power would be simply the average power dissipated due to each component. It is super position.

In other words the load power, if this is the current then it would be A 1 squared by 2 multiplied by R L and the power due to this would be A 2 squared by 2 multiplied by R L and the total power would be a sum of these two, okay.

(Refer Slide Time: 47:28)

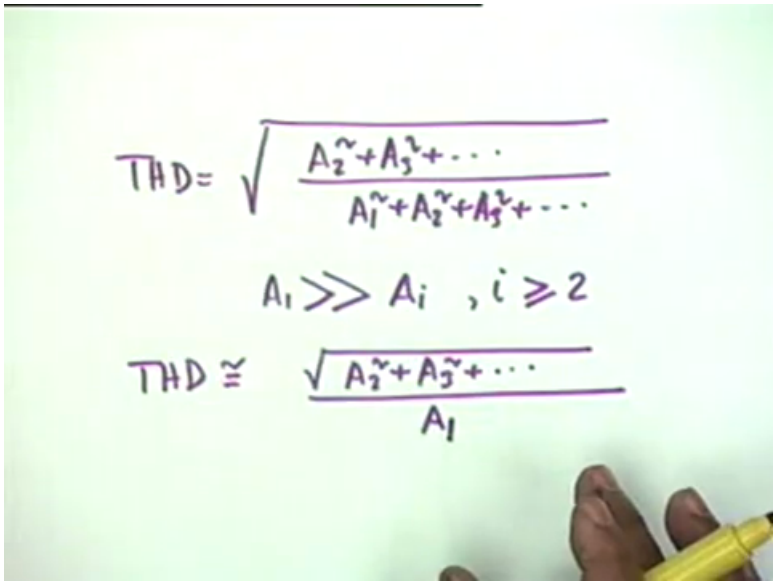


This could be very easily shown. Can you? Take two terms and show that this is so. So the total power in harmonics what would it be proportional to? A 2 squared plus A 3 squared plus etc. Whereas the total power in the load would be A 1 squared plus A 2 squared plus etc. So THD total harmonic distortion would be square root of A 2 squared plus A 3 squared plus etc divided by A 1 squared plus A 2 squared plus A 3 squared and so on.

Usually what is our aim? Our aim is to make A 2, A 3, A 4 as small as possible compared to A 1. So A 1 is usually much greater than A i, i greater than equal to 2 which means that THD total harmonic distortion can be expressed as square root of power in the harmonics divided

by A 1. That is the amplitude of the fundamental. Amplitude or root mean square value whatever you want. This is an approximate measure and this is what is used.

(Refer Slide Time: 48:54)



People sometimes use a percentage measure which means that you multiply this by 100 and use a percentage, okay. We will stop here. We will in the Monday class work out problems.