Analog Electronic Circuits
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Lecture 26
Class B, Class AB and Class A Power Amplifiers

In the last lecture we had introduced power amplifiers and the classes of operation. We discussed today class B then class AB somewhere in between and class A power amplifier. We recall that class B power amplifier was for integrated circuit very simple circuit. Two transistors NPN and PNP with the bases tied together and connected to the source and the load is connected from the two common emitters to ground.

And essentially Q 1 conducts during the positive half cycle, Q 2 conducts during the negative half cycle and if there was no V B E on then the (am) amplification would have been undistorted power amplification. However because of V B E on because of a minimum threshold voltage for the transistor to conduct, the characteristic is like this. If the slope of the inclined portion is unity that is d V 0 d V i is equal to 1 but for V B E on that is this portion which is the dead band.

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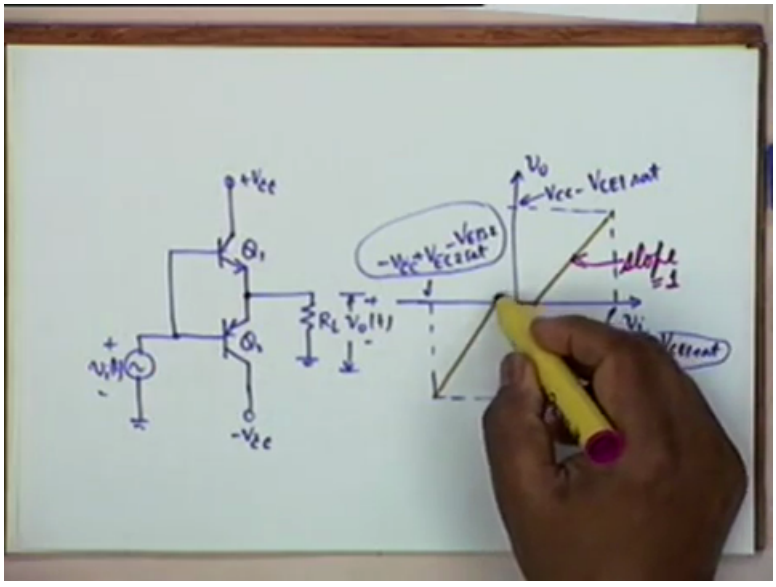

Then obviously what we will get if we have a sinusoidal input and if this is point 7 and this is minus point 7 we take V B E on as point 7.

And this is V i then V 0 would start here and end here during the positive cycle so it will be something like this where the two curves are exactly parallel with a difference of point 7 volt and this would be the output V 0 and on the negative cycle the conduction will start here and you will get a curve like this which is also exactly parallel to the V i curve but with a difference of point 7, okay.

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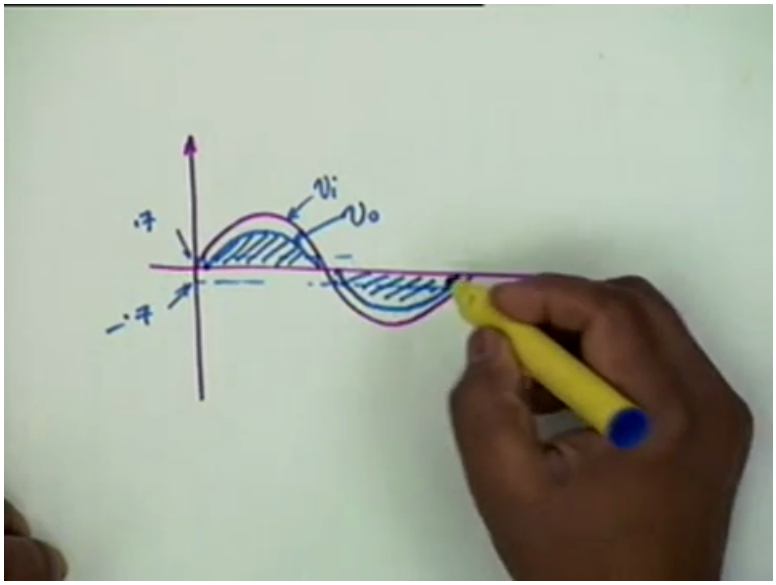

And this is the region where there is no conduction and therefore you get a distortion and this as I had told you is the crossover distortion. Suppose now the input voltage is increased, input voltage is like this. The amplitude had increased. Obviously the crossing with point 7 shall occur earlier and therefore the width of the dead band shall decrease and therefore crossover distortion decreases with increase of maximum input voltage, okay.

Crossover distortion decreases however as you know we cannot increase V i m indefinitely because of again distortion considerations, okay. We cannot increase V i m indefinitely. We cannot increase it beyond V C C anyway. That is the limit. No? What is the limit?

Student: V C C minus V C E sat.

V C C minus V C E sat. That is the limit of the output voltage therefore the input voltage cannot exceed V C C minus V C E sat plus point 7. That is V B E, okay. So we have a limit on this. We cannot increase it indefinitely and crossover distortion in such a complementary symmetry amplifier is a fact of life.

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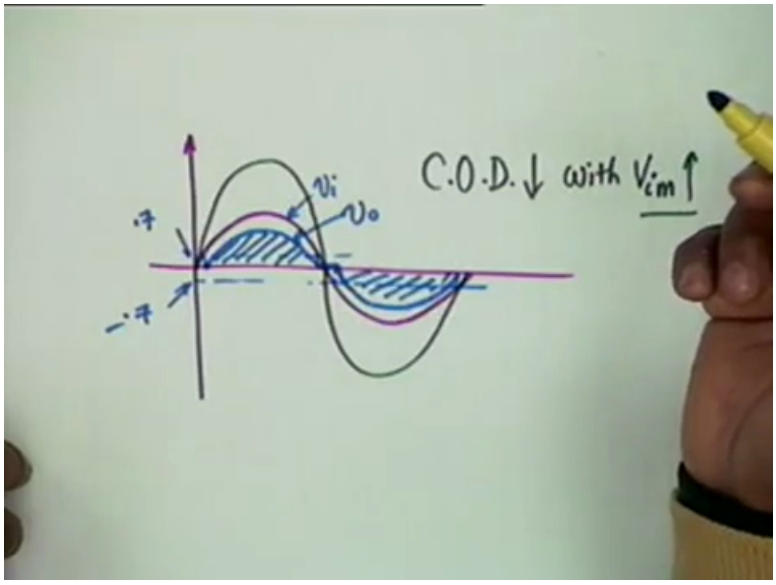

Now this cannot be tolerated in sophisticated applications and therefore we have to find a way to get over the crossover distortion. And the obvious solution is that if in this complementary symmetry circuit the NPN transistor could be biased at point 7. That is if V B E Q was plus point 7 then obviously this transistor shall never put a dead band. Similarly if in the PNP transistor Q 2, V B E 2 could be put at plus point 7 then this transistor will also not set its dead band, alright?

Student: Sir, why?

Why is the dead band created? Because there is a threshold. This transistor does not conduct before V i reaches minus point 7 and therefore if I could bias this at minus point 7 volt and this at plus point 7 volt then there would have been no crossover distortion.

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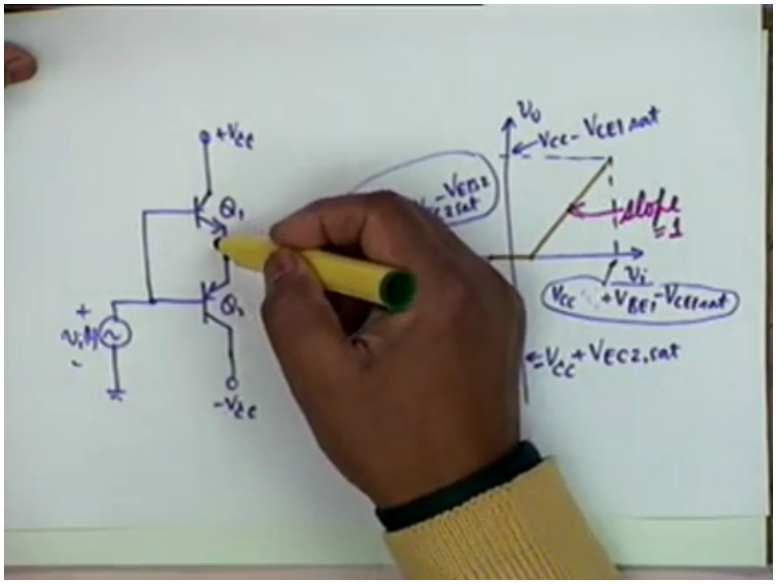

And however the operation no longer remains class B because if you look at the load line we are not biasing at this point we are biasing at somewhere here which means that the conduction angle we are trying to make exactly 180 degrees, that is half of the cycle, but the operating point now shifts from the cut off point to somewhere into the active region and therefore this operation is called class AB. Class AB operation is a modification of class B to take care of threshold conduction in the BJTs, to take care of crossover distortion.

Now how is this done? We obviously cannot use a large number of resistors in an integrated circuit so how it is done is to use more transistors, okay. And the circuit, please draw with me, circuit is very simple and nevertheless at the cost of a few more transistor. Let us see what this circuit is. We have a plus V C C and the main transistors Q 1 and Q 2. From here it goes R L and this is V 0 t. Then you have the PNP transistor Q 2 and this goes to minus V C C, alright.

What we want to do is to bias this transistor Q 1 to plus point 7 and this transistor Q 2 to minus point 7. Now this is done by connecting two PNP transistors in diode connection from here to here. From here to here we connect two PNP transistors in diode connection. So what we do is we have a Q 3 which is connected as a diode and we have a Q 4 which is also connected as a diode.

Student: Sir, are these NPN or PNP?

These are both NPN.

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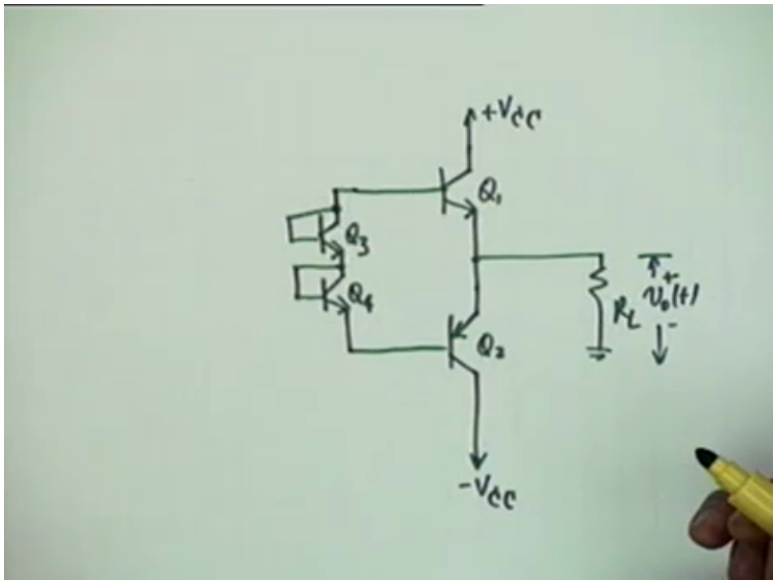

And if somewhere other we can keep these two diode at point 7 volt that is if we can keep Q 3 and Q 4 in the active region, alright, then the drop from here to here would be plus point 7, the drop from here to here would be plus point 7 and that achieves what we want to achieve. Why? Because the symmetry of the two circuits this point and this point, the two potentials would be equal. It is a voltage breach.

Because of symmetry if Q 3 and Q 4 are identical transistors and Q 1 and Q 2 are identical transistors, okay, I am not saying Q 1, Q 2, Q 3, Q4 are identical. I am not saying that. There is a difference. I will tell you what the difference is and this is an intentional difference, okay. So if Q 3 and Q 4 can be kept at V B E or V C E equal to point 7, our purpose is achieved. Now we do not want to draw any current from here. We just want to set up a voltage point 7 here, a voltage point 7 here.

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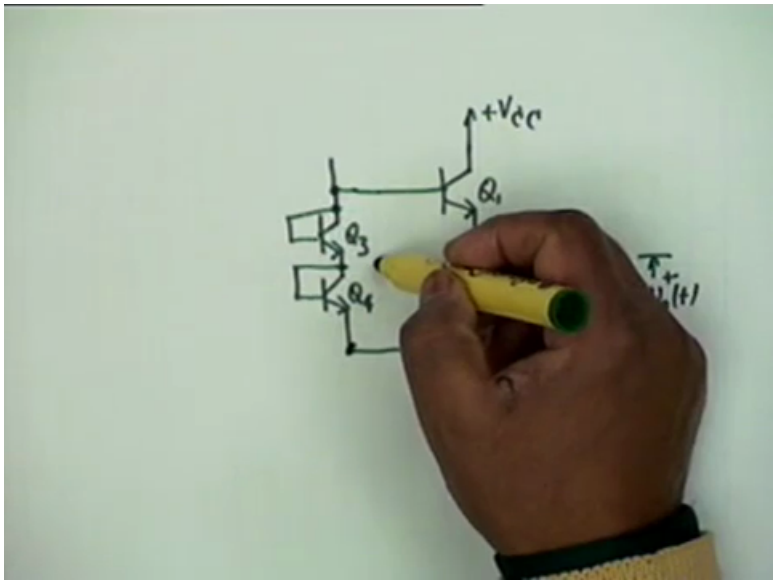

So the current is not important but we do need a current. Now how this current is obtained is we can either use a resistor from plus V C C to here. Then it would be V C C minus 1 point 4 divided by.

Student: R.

Which R? We have to put a resistance here, okay. That will be the reference but since we know a better technique this resistance may require maybe a large resistor which we cannot, so we use a current mirror, okay. That is it. So what we do is from plus V C C we take a transistor. And obviously the current mirror shall have to be PNP, okay. So this is what comes here.

This is Q 6 and this current is let a say, I will do it later and the other transistor the reference transistor is this one. This is also a PNP and we require a small resistance R 1 here and this can go to minus V C C. The current here which direction? Here this direction or upward?

Student: Downward.

Downwards because it is minus V C C. So this is the reference current I REF.

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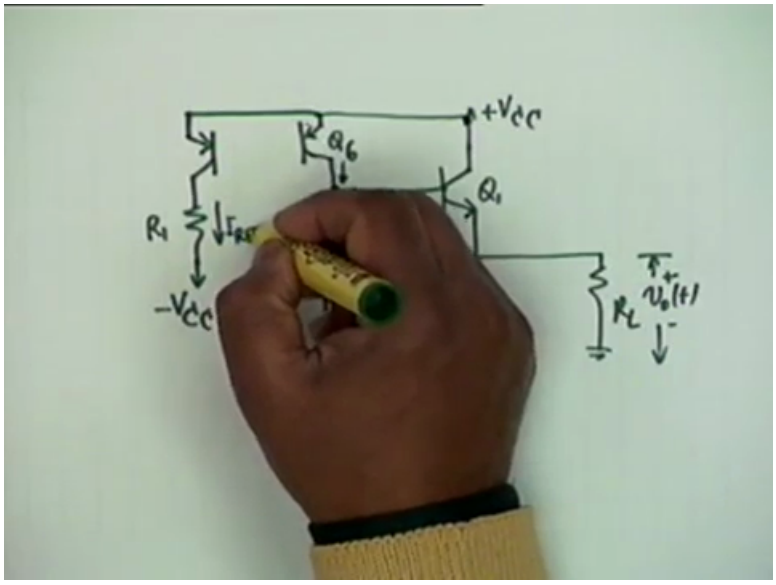

And the two bases have to be connected together and this has to be a diode connected transistor, okay. So this is a current mirror. This sole purpose of this current mirror is to supply a current here to the two diode connection transistors. Not just that you see it also supplies a current to Q 1, I B 1. It also takes a current from Q 2, I B 2. This base current goes away, agreed? Nevertheless if the two betas are large then we can ignore these two currents and as you know in a current mirror this current would be approximately I REF, okay, approximately I REF.

So the current that passes through Q 3 and Q 4 shall be approximately equal to I REF each. Why approximately? Because we are ignoring I B 2 and I B 2, okay. So I sub C 3 is approximately equal to I sub C 4 approximately equal to I REF, okay.

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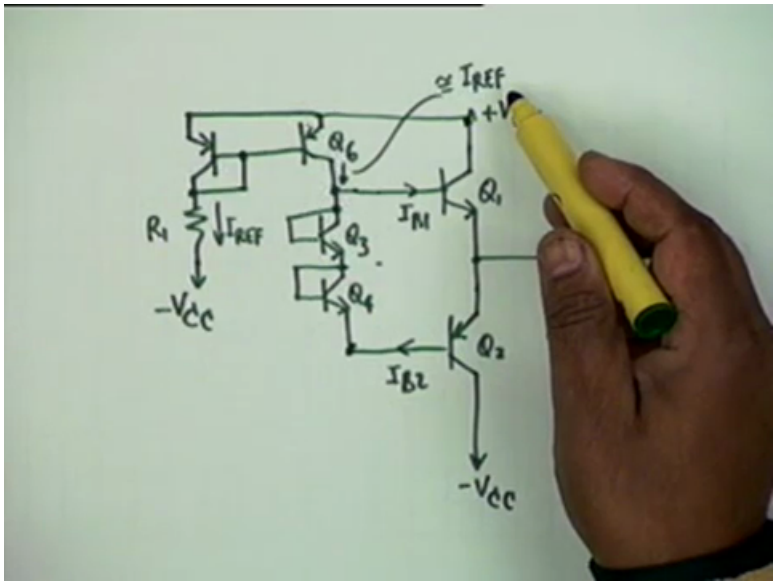

I am explaining qualitatively, when I make a quantitative derivation I will assume all of them to be different and you will see the result. Now the point that I was mentioning (())(13:28) I had assumed I did not mention. I did not mention that Q 1, Q 2, Q 3, Q 4 are identical. I did not mention this. Let us name this transistor also Q 5. The reason is the following that these transistors Q 3, Q 4, Q 5, Q 6 they are not to supply large currents. Large currents are to be supplied only by Q 1 and Q 2, right?

The sole purpose of Q 3 and Q 4 are to establish a threshold voltage, a cut in voltage of point 7. The sole purpose of Q 5 and Q 6 is to supply a reference current to Q 3 and Q 4 and therefore since current levels are not important these transistors can be made with much less junction area than these two transistors. Why much less? Because larger the current drawn from the transistor the more will be the dissipation and the more will be the junction area required to supply this current.

Otherwise the transistor will burn off, okay. So the emitter junction area for Q 6, Q 5, Q 3, Q 4 can be much less as compared to that of Q 1 and Q 2. Now what does this affect? which parameter does this junction area affect? It does not affect V B E. The thresholding of a diode is independent of the junction area. What it affects is you should remember the saturation current I sub S. You remember the relationship I sub C equal to I sub S exponential V B E by V T, agreed? It is this I sub S that is affected. The reverse saturation current by the junction area.

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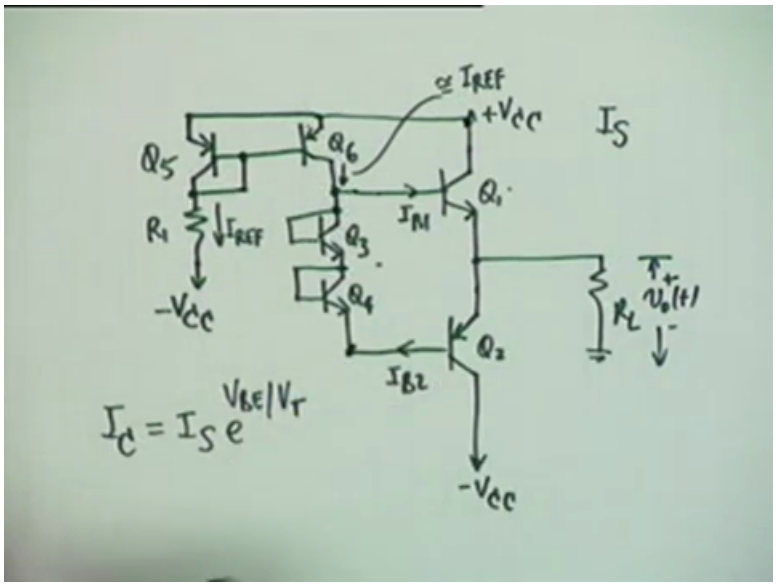

So if the junction areas of Q 6, Q 3, Q 4, Q 5 is less than that of Q 1 and Q 2, I S 3, I S 4 would be less than I S 1 and I S 2, okay. You might ask me why create this complication? Because in an integrated circuit every modified step of fabrication cost money, every modified step. If you have standardized these steps and make 1 million transistors and if you modify one step and make ten thousand maybe the cost will be comparable. Each modification cost money.

We have to regulate the flow of gas and this has to be automatic. Therefore you have to break the process readjust and run it again and this cost money, okay. And so therefore why should we make the junction areas lets. Yes.

Student: (())(16:33)

It flows to Q 3 Q 4 and this is V i. I beg your pardon. I have not shown you this V i. This is V i. Then flows like this and in the path while it flows it gives out a small part I B 1 because there is a bigger Q 1 here, okay.

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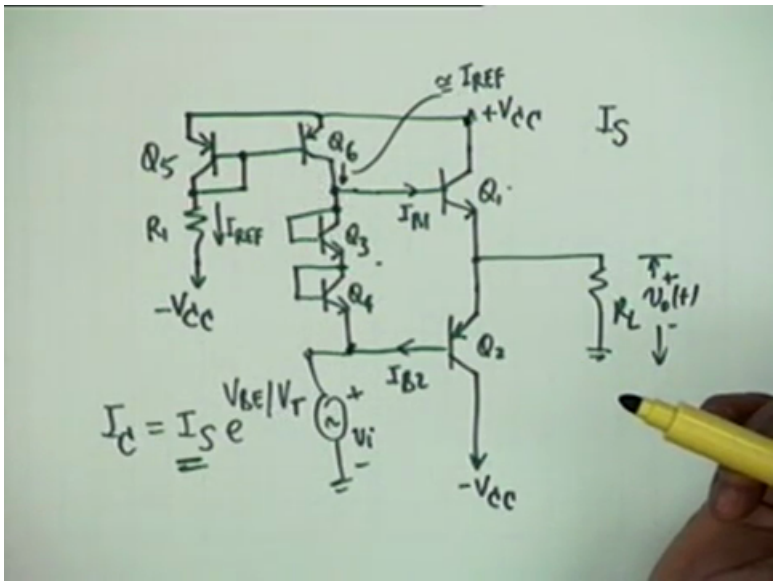

But it gets its prize through I B 2. Q 2 gives some quantity back and that is how it replenishes it. But as I said if beta 1 and beta 2 are large then I B 1 and I B 2 can be ignored. Going back to that question why should one have less junction area in Q 3 Q4? Why not make them identical? That will unnecessarily increase the cost of the chip because the junction area, the cost of an integrated circuit is determined by the number of steps, the time taken by steps, but primarily by the area of silicon that you have to use and therefore there are four transistors here.

If you can reduce the junction area to one quarter then this would be equivalent to fabricating one silicon transistor of a larger capacity, agreed? So I S 3 and I S 4 would be much smaller compared to Q 1 and Q 2. And if we get 1 is to 4 this is what people use in fabrication. Most of the open circuit if you open them up you will see that the main transistors, the subsidiary transistors which are not required to carry large currents are approximately 1 4th junction area.

This is the rule of thumb. You can go to less but then there will be problems of voltage insulation, insulation strength and so on. So 4 is to 4 is determined as a compromise, okay. Now going to an analytical formulation of the whole problem, you see what we want is that V B E 3 plus V B E 4 should be equal to V B E 1 plus V B E 2. That this is a balanced circuit is a different method but analytically you shall bring that balance equation later.

But analytically our simple KVL is that V B E 3 plus V B E 4 is equal to V B E 1 plus V B E 2, okay. Let us write this equation then we shall be able to determine I sub C 1 and I sub C 2, require some values because I sub C 1 and I sub C 2 are determined by V B E 1 and V B E 2, okay.

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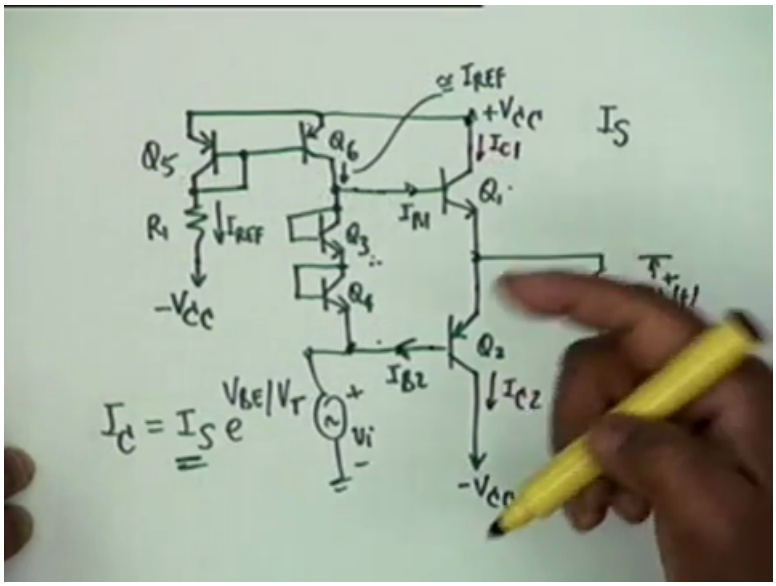

So the simple equation is that V B E 3 plus V B E 4 is equal to V B E 1 plus V B E 2. Let us write these V B Es in terms of the collector currents. Then obviously what we get is V T log I sub C 3 divided by I S 3, alright? Is this equation clear? From that collector current equation so plus V T log of I sub C 4 divided by I sub S 4 would be equal to V T. V T is the common factor, this Q by K T, I sub C 1 divided by I S 1 plus V T log of I sub C 2 divided by I S 2.

And if I combine you can see that I C 3 I C 4 divided I S 3 I S 4 is equal to I sub C 1 I sub C 2 divided by I S 1 I S 2, okay. Very simple equation. We get rid of V Ts, we get rid of logs.

Student: (())(20:45)

Okay, I am coming to that. If we look because both of these transistors have to share the power. Q 1 has to work in the positive half cycle Q 2 would be in the negative half cycle. There is no reason why these two transistors should not be identical. In fact they have to be identical to have a symmetrical swing. The power supplies are identical. Q 1 and Q 2 have also to be identical and therefore I S 1 and I S 2 are equal. As far as I C 1 and I C 2 are concerned they should also be equal if we ignore I B 1 and I B 2, agreed?

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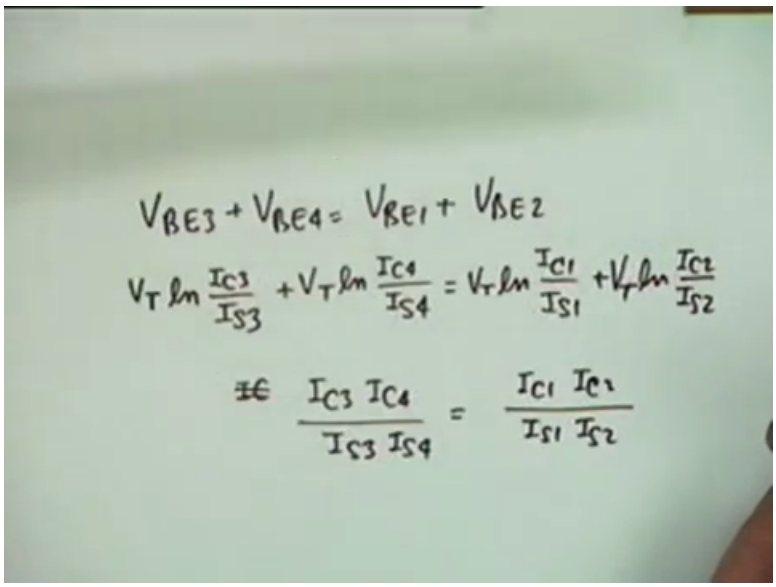

If we ignore this and therefore our collector current I sub C 1 which is equal to I sub C 2 would be given by what? My equation would be I C 1 squared equal I S 1 I S 2 divided by I S 3 I S 4 times I C 3 I C 4. Therefore my equation would be I C 1 equal to I C 2 equal to square root of I S 1 I S 2 divided by I S 3 I S 4 multiplied by square root of I C 3 and I C 4 where they should also be identical except for the fact that there is a base current also.

So approximately they should also be identical but let us put the approximation at a later point of time. We agree that I C 3 and I C 4 should be approximately equal.

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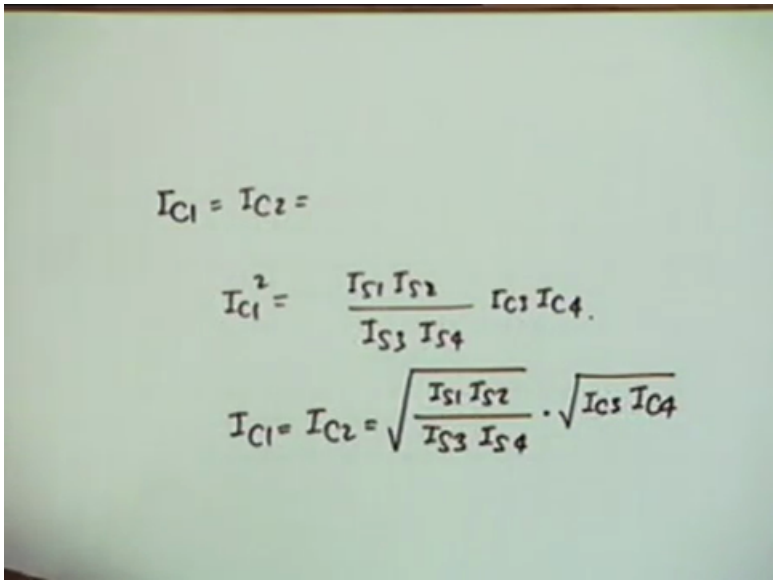

Now as far as the transfer characteristics is concerned let me go back the circuit.

Student: Sir, have we assumed that there is no current flowing through R L?

We are considering the DC conditions therefore V sub I equal to 0 should give V 0 equal to 0 and therefore no current, is that clear? The question is when we assume I C 1 equal to I C 2 these are DC conditions. There are no signal is applied. If V i equal to 0 then V 0 should be equal to 0 and therefore no current flows through this, so current must flow like this.

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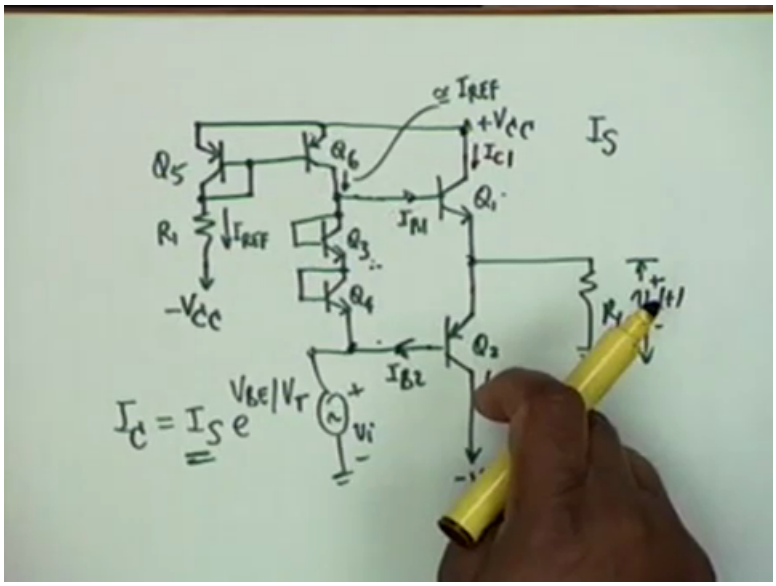

But I brought out this figure for a different reason. You see that if I go from ground via this path to ground again we can write a KVL and this KVL would be, excuse me, V 0. I am sorry, the KVL would be V i plus V B E 4 plus V B E 3. That would be equal to V B E 1 plus V 0, is

that okay? From which since the voltages are identical you get V i equal to V 0 minus point 7, agreed.

Similarly if you go via the alternative path , excuse me, if you go like this, the (())(24:30) half cycles V i plus V E B 2 would be equal to V 0 and therefore once again V 0 is V i minus point 7, is the point clear? In either cycle this is the story, okay.

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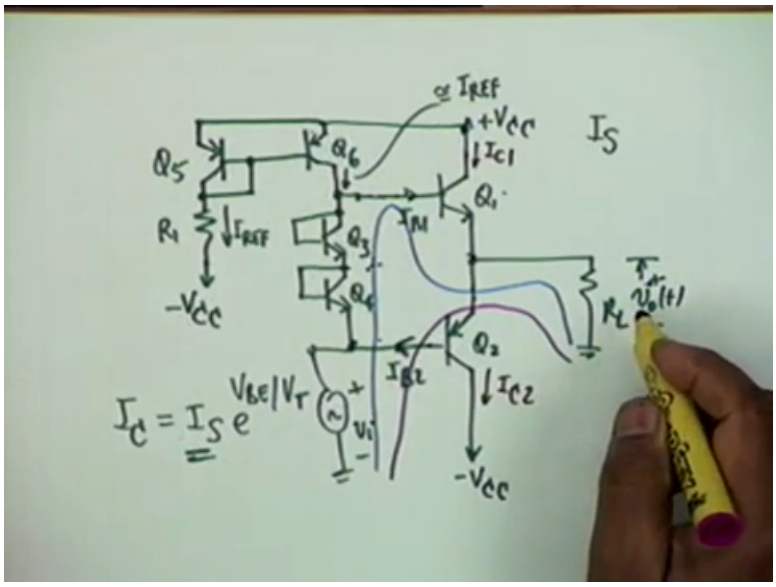

This was the same story earlier also that created a dead band but here it will not create a dead band. What I have is V i equal to, no a bigger point, V 0 equal to V i minus point 7, alright. Now if I draw the transfer characteristic you see that when V i equal to 0, V 0 is minus point 7. So the characteristic starts from here. When V i equal to point 7.

Student: Sir, is it V 0 equal to V i plus point 7?

That is correct. I made a mistake. It was the previous story. Previous story was V i minus point7. Now it is V i plus point 7 and therefore when V i equal to 0, V 0 is this. Thus the curve now, there is no dead band, the curve now, because we have shown that whether you go through Q 1 or Q 2 the relation is the same. So the curve now goes like this, okay. There is no dead band. This is V i and this is V 0, alright?

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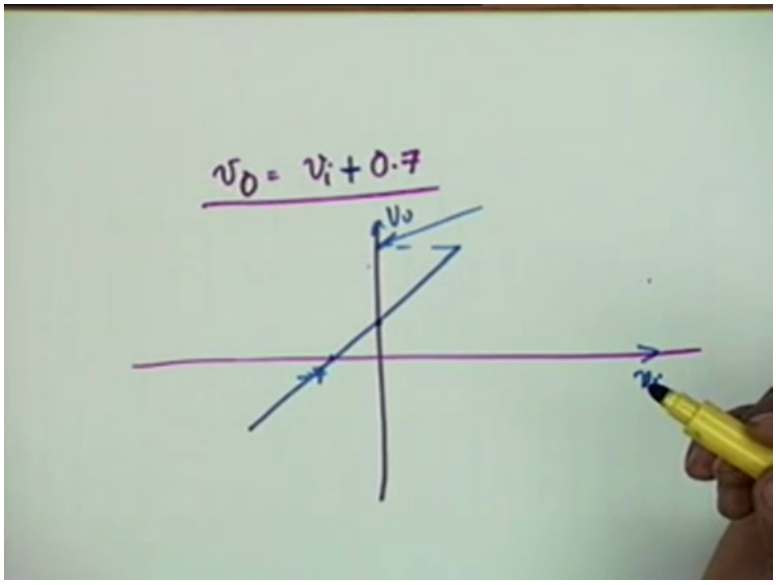

This maximum positive value of V 0 obviously if you refer to the circuit is V C C minus V C E sat. So the maximum value is still V C C minus V C E sat and it occurs at V i equal to V C C minus V C E sat minus point 7, agreed? And similarly the minimum value that can be reached is minus V C C plus V E C sat because for the second transistor which was the PNP it is V E C sat which is equal to point 2, okay. So this is how you can find out what the input voltage is.

This is exactly the negative of this, okay, for that particular input. You can now see that the swing is no longer symmetrical, is not it right? There is a slight off set here but the point is we do not mind a little less swing. But what we want is that there should be no crossover distortion. So this is a very small price to pay and in any case no power amplifier should be driven to saturation. So we will not go up to this limit anyway.

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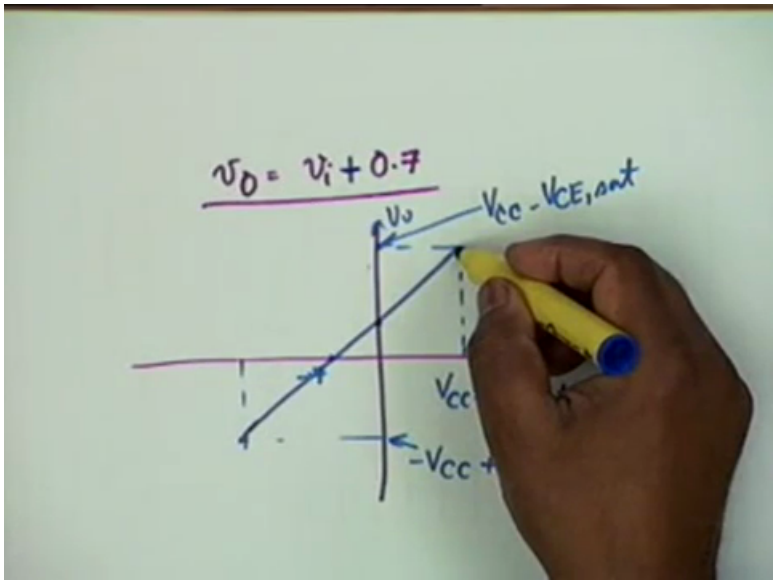

If we are somewhere in between then there is no problem, okay. We should not go to saturation. What we should do is to see in the CRO that the output waveform is approximately the same as the input waveform. That is there is no crossover distortion. Let us take an example and this operation is therefore called, it is neither class A not class B so it is called class AB operation. And class AB is specifically resorted to because of the problem of crossover distortion. What is the price that you pay?

Student: (())(28:39)

The price is that Q 1 Q 2 are on the verge of conduction therefore at the Q point there is a collector current and therefore there is an additional dissipation. On the other hand if you had biased at their cut off point then there would be no DC quotient current and there would have been no dissipation in the absence of a signal. It is only in the presence of a signal that there will be dissipation, not otherwise. But in class AB naturally because you have to tolerate an amount of quotient dissipation the efficiency will go down.

We will calculate efficiencies later but let us look at a later point. Suppose in this class AB circuit suppose plus V C C is plus 15, minus V C C is minus 15. Suppose V C C is 15 volt and R 1 is 47 K. R 1 is the reference resistor for the current mirror, okay. That current mirror I showed you a simple current mirror. It could be a wiggler source. If you require much less current it could be a wiggler source.

It could be a simple current mirror or it could even be, if you can tolerate a large resistance, it could even be a single resistor. But large resistance is never used even if you to use 20 transistors to avoid large resistance you will do that because the silicon area is much more

cost effective in terms of multiple transistors rather than a single large resistance, okay. I repeat this because these are the main principles followed in IC fabrication and followed for very important reasons. Important reason is saving money, okay.

Make it as cheap as possible and sell it for as higher price as possible, okay. That is the business technique. The question is to compute all quotient currents. All Q point currents are needed and it is given that Q 1 and Q 2 junction areas are 4 times the Q 3 to Q 6 junction area, okay. You are required to complete all the currents.

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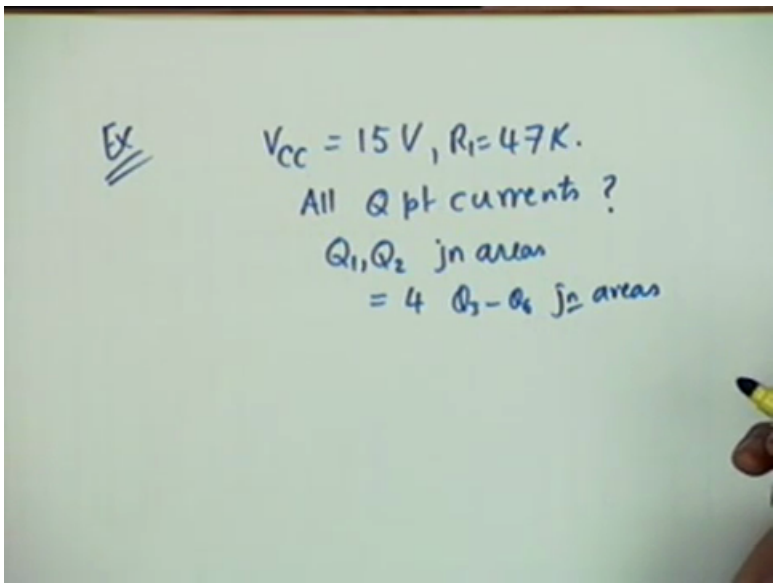

The first thing you do is to compute the I REF. the second part of the question is if beta NPN is 150, this is another thing I want to point out through this example. And beta PNP is 50. You might ask me they are identical transistor made on the same chip, how come beta NPN is greater than beta PNP? This is also a fact of life and that is why NPN transistors are preferred over PNP transistors. To get a high beta with a PNP transistor one has to spend much more than one does in an NPN transistor.

Even if made on the same chip they are 1 to 4 the spread in beta between PNP and NPN can be as large as 3 to 4, okay. This is also a fact of life. When I say identical you have to make special efforts to make them identical. You know in terms of AC parameters also, okay. So but in this particular situation it does not matter. Why does not it matter? In this situation of a class AB amplifier it does not matter. Even class B it does not matter whether beta PNP is 3 times less than beta NPN because they are emitter followers.

We are not asking for voltage amplification or current amplification. They are large signal amplifiers. All we want is that V 0 should follow V i. The power input does not have to deliver any power. All the power we shall extract from the power supply, okay. So under this condition if this is true, can I B 1 and I B 2 be neglected? This is the second part of the question. It is a simple example but it illustrates a number of points and that is why I take this example.

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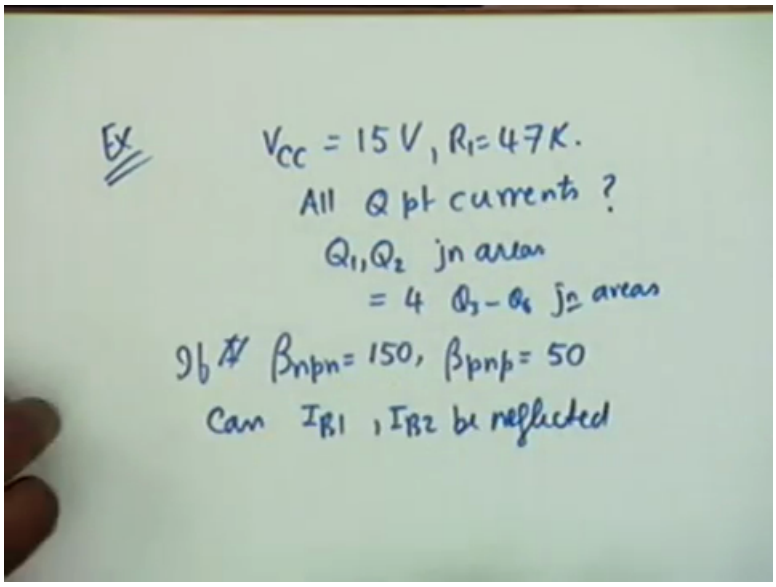

Now if you refer to this circuit back we have to find out all these Q point currents. The first thing we find is I REF, alright? And I REF obviously is 15 V C C minus, minus V C C that is another 15, okay. This voltage minus this voltage minus point 7, okay. Minus point 7 divided by R 1 is given as 47 K and this calculates out as 623 microampere. If this is I REF then obviously I sub C 3 we will examine that point about I B 1 and I B 2 later.

But I sub C 3 is approximately equal to I sub C 4 approximately equal to 623 microampere, both of them. Our point is to calculate I sub C 1 and I sub C 2 and that is square root of I S 3. I beg your pardon I S 1 I S 2. Let me write it down. I S 2 divided I S 3 I S 4 multiplied by square root of I C 3 I C 4. And since the transistors Q 1 and Q 2 at 4 times the emitter junction area this square root shall be simply equal to 4, agreed? 4 and this would be 623 microampere because we have assumed them to be equal and this calculates out as 2 point 49 milliampere.

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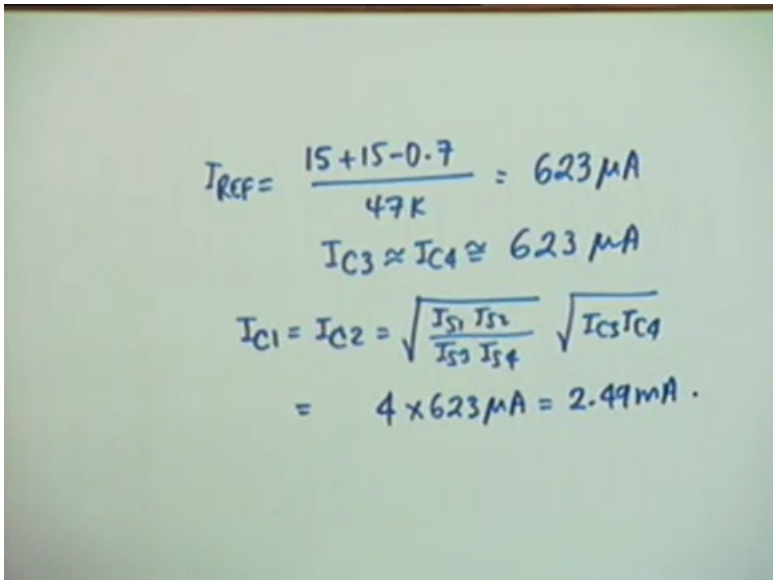

The next point is whether I B 1 and I B 2 could have been ignored. We have ignored this in calculation but justify the means. Let us see if this is I C 1 then I B is 2 point 49 milliampere divided by beta NPN which is 150 and this comes out as 16 point 77 microampere. Compared to 623 obviously 16 point 77 can be ignored, agreed? Similarly you calculate I B 2. How much? 3 times this that means 49 point 8 microampere. Even 50 microampere we could ignore compared to 623, okay. 1 is to 12 ratio we get.

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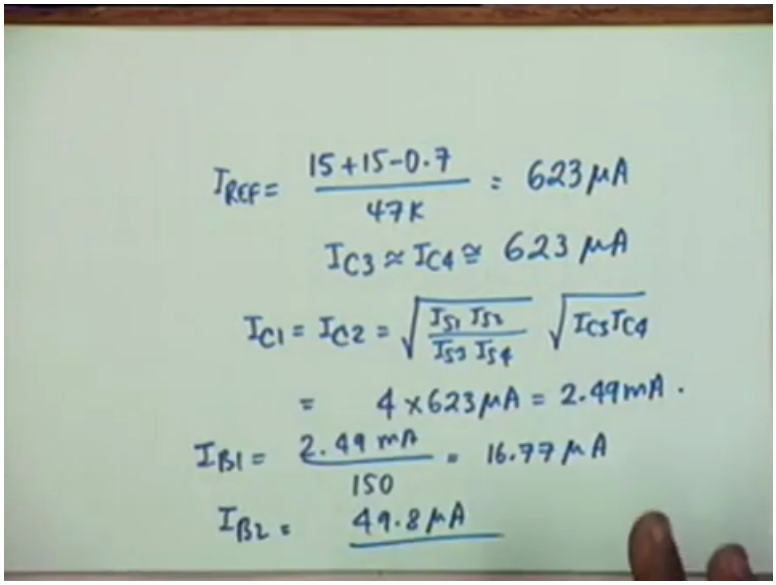

So in practice these approximations are indeed valid.

Student: Sir why it is the ratio?

Why? 50 microampere and 623 approximately 12. No, it is more than 12. More than 12. Yes, 5 times 12 is 60. So 62 must be more than 5 times 12, okay. The next point that we take up we have considered class AB. We will come back to class B and class AB when we calculate efficiency, okay. That means how much power is delivered to the load as compared to the power dissipated in the transistor? We would like zero power to be dissipated in the transistor. But you see even in class B the quotient dissipation is zero.

That is when there is no signal there is no dissipation. Actual class B suppose there is no crossover distortion, okay. It is not class AB so at the quotient point there is no dissipation. But when the signal comes, one transistor produces only one half of the sin wave. So there is an average current flowing in that transistor. Similarly the other transistor also has an average current and therefore when there is signal both transistors have a DC flowing through them and that causes dissipation.

That is the main reason for dissipation, agreed? The other parts of the circuit for example the two Q 3 Q 4 in the class AB. Q 3, Q 4, Q 5, Q 6 they are not required to supply large currents. They are typically small current carrying transistors and therefore the power dissipated in them although they do it continuously, the power dissipated in that is of no concern. It is insignificant compared to the output transistors. So what we will do in calculating efficiency is power delivered to the load.

Stripped definition is power delivered to the load, AC power. And obviously it is not the peak power it is the average power which is RMS value of the voltage multiplied by RMS value of the current if the load is resistive. If the load is reactive then we have to multiply by cosin of the angle between the two phases, okay. This is the average power dissipated in the load. That has to be divided. Strict definition is total power supplied by the battery. Therefore you have to put two meters at the plus V C C and minus V C C and measure the total.

But we do not have to do that because the current supply to other transistors would be very little compared to the current supplied to the main output transistor. So we approximate this by power dissipated in the output transistors. The total power delivered by the battery is approximately equal to the total power dissipated by the output transistors, approximately, okay. But that point later. What is so wrong about class A? Why not you say class A?

Class A has been used for voltage amplifiers, for current amplifiers, for small signal amplification, why not for power amplification? I told you the reason. What is the reason?

Student: (())(40:04)

At the Q point there is a dissipation. Even if there is no signal, the current flows and therefore there will be dissipation and that causes inefficiency. It could be as you will see later class a maximum efficiency is only 25 percent maximum. If you drive large enough voltages, large enough base currents, maximum that you can get that is for every watt that you deliver to the loudspeaker you have to be prepared to dissipate 3 watts in the transistor which is wasteful in terms of power. And elaborate cooling arrangements have to be done, okay.

But suppose it is an intermediate stage. Suppose you do not require large power. It is a small power device. For example an intermediate stage in an open where a little bit of power is to be delivered to the next stage, okay. Class A can be used. Not only that, if you are very fussy about music quality, even that avoidance of crossover by those transistors and all that may not be good enough. Then you have to go for class A and you have to provide a cooling mechanism.

You have to provide large fins for example for dissipating the heat. for quality music nothing like undistorted class A amplification even though the efficiency is less. However there are ways of reducing the dissipation and all that. So basically if it is a low-power power amplifier or a very high quality power amplifier, in terms of audio quality, in terms of the frequency response, in terms of total harmonic distortion THD, then class A is essential.

And in class A as I have said the conduction angle is 360 degree. That is the transistor conducts for the total input cycle. For a class A power amplifier as far as the circuit is concerned, in a discrete circuit there is no difference. You have those R 1 R 2 exactly like a voltage amplifier. You have the R C. Then you couple it to an R L and so on. But in a IC power amplifier obviously we cannot use so many resistors. We shall replace all of them by transistor except for perhaps one that is the current mirror.

No, R L is determined by your needs. R L is not integrated. there is an output terminal you connect your R L but that reference resistor is needed for the current mirror, okay. So now the other thing is in a voltage amplifier there is an R C as well as an R L. That is usually we use a common emitter but in a power amplifier to use a number of the resistor we do not want resistor.

We do not want voltage amplification and therefore we can use an emitter follower. So class A is also in integrated circuits not in ordinary circuit. In integrated circuit the class A power

amplifier is operated as an emitter follower and I will draw the circuit and explain what is happening.

Student: Excuse me sir.

Yes.

Student: Sir in this case there is two transistors having V C E of 15 volts across them.

V C E of?

Student: 15 volts across them because it is 15 and 15, 30 volts. So sir each one will have a 15 volts V C E.

Each one will have 15 volts, yes.

Student: Sir, can they stand?

They have to. We have to design such that they stand it, yes. If V C C is plus 15 in fact the transistor should be able to stand 30 volts. Ah! It is a very interesting point. I am glad you raised the question. You see in any I C design you have to take account of accidental short circuit. It may be done by lack of care or it may be because of statics, charge accumulation and things like that, okay. So if it is plus 15 and minus 15 each transistor V C B O. You understand what is V C B O?

Student: Collector base breakdown voltage.

Collector base breakdown voltage. V C E O, collector emitter breakdown voltage has to be greater than 30, alright. Because the other transistor maybe accidentally short. Then you have 30 volts across this transistor and this may be short because of charge accumulation for example, alright. With a little bit of cooling or exposure maybe the charge will disappear and then the transistor come back in its original shape, okay, right?

Now about this circuit and then I will draw the circuit and then I will quit for the next class. Plus V C C it is operated as an emitter follower and therefore the load is from here to ground, R L. And normally you expect V sub i from here.

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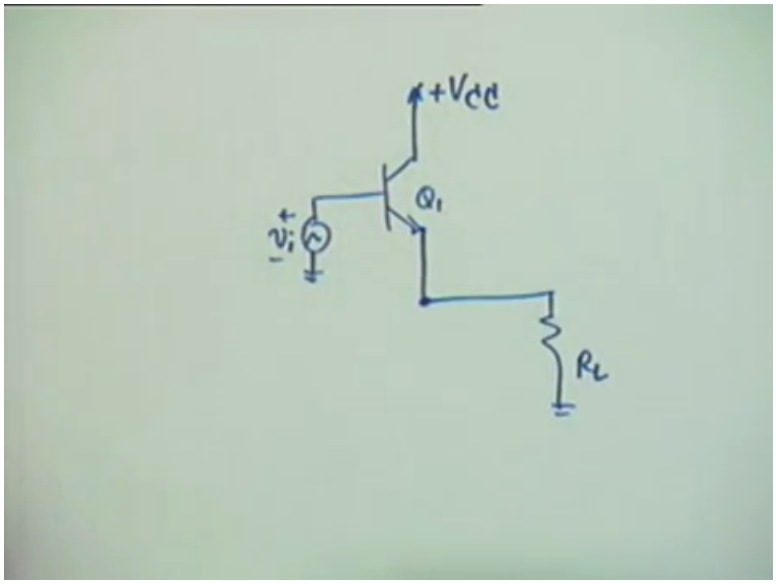

The biasing of the transistor is done by a current mirror. That is what I do is now you no longer require a PNP current mirror. You can do it NPN and if you can do it NPN, you should do it NPN, alright, because PNP has its own problems. So we require a current mirror, a reference resistor R 1 and this is I REF. Then you have this diode connected transistor. I am showing a simple current mirror. It could be a wiggler source also depending on what amount of current you require.

Now this would go to another transistor, the main transistor. Where would this go, the collector? I want to bias this transistor Q 1. That is correct. It would go to the (())(46:55) and these two are connected. They may not be connected they are maybe wiggler resistance here R W depending on what current you want .

This is the DC that flows. Where does this go? It is an integrated circuit. I do have minus V C C so I put it here. These transistors I will call them Q 2 and Q 3. You see the biasing? I have used only one resistor that is R 1 which can be a small resistor.

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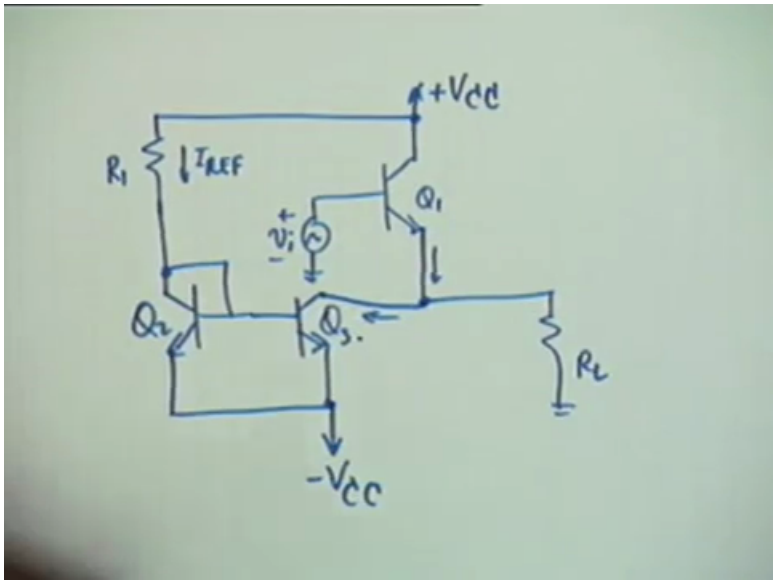

30 minus point 7 divided by R 1 will be I REF. And I REF is approximately the current that I want in V C C. That is all that I want and of course this voltage now Q 1 is to be prepared for a voltage of 30 volts across it, at least 30. It must be able to stand. We will analyse this circuit tomorrow.