Analog Electronic Circuits
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Lecture 25
FET Differential Amplifiers and Introduction to Power Amplifiers

This is the 25th lecture on FET differential amplifiers and we shall also introduce today power amplifiers that is large signal amplifiers. The circuit for FET we already drew. We shall draw a part of it today to start the discussion and this part is the initial part Q 1 and Q 2. This voltage is V G 1 and this voltage is V G 2. The two sources are connected together S 1 and S 2 and they are connected to a resistance R sigma. This current is I S S and this is minus V S S. The rest of the circuit is R Ds.

I could as well draw them. R sub D and this connect to plus V D D. I have not shown the source part. Let the two gate voltages be V G 1 and V G 2. Then the differential voltage applied at input V sub D is equal to V G 1 minus V G 2. It is the difference voltage applied between these two terminals and as usual as we did with the BJT amplifiers, in the FET also we find this difference V G 1 and V G 2 as V. I beg your pardon. This will be simply V G S 1 minus V G S 2, is that okay?

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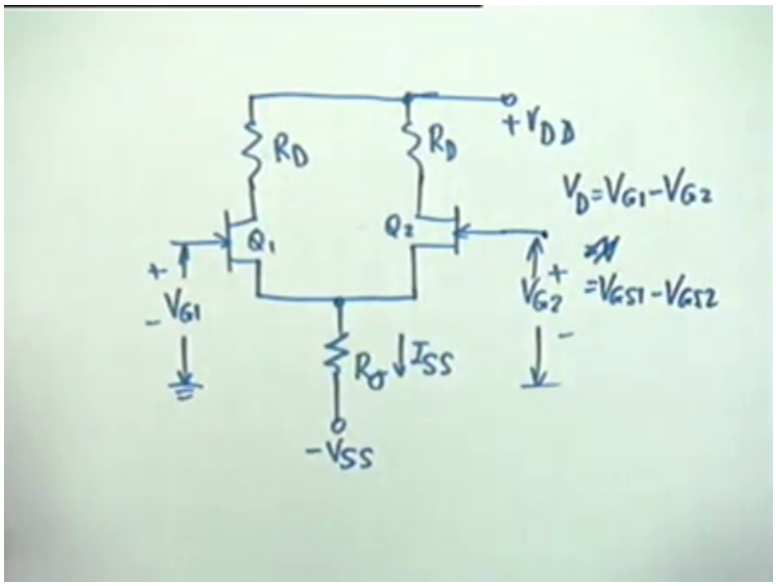

Student: Sir, R sigma sigma.

Okay alright. V sigma sigma and.

Student: R sigma sigma.

Okay, because two emitters are connected so instead of one subscript we use two. R matters but okay I agree. Do you see that V G 1 minus V G 2 is simply equal to V G S 1 minus V G S 2, okay? Is that point okay?

Student: Okay sir.

Right, now we are in discuss. Our purpose now shall be to express V G S in terms of I sub D because we want to calculate these two currents I sub D 1 and I sub D 2. Obviously one of the relation says that I sub D 1 plus I sub D 2 would be equal to I S S. There are no gate currents at all and therefore this is an exact relationship.

Student: Sir please tell again why V G 2 is V G S 1 minus V G S 2.

Oh! V G 1 minus V G 2 because this point is common so it is V G S 1 minus V G S 2, okay. This is V G S 1 plus minus and this is V G S 2 plus minus, okay.

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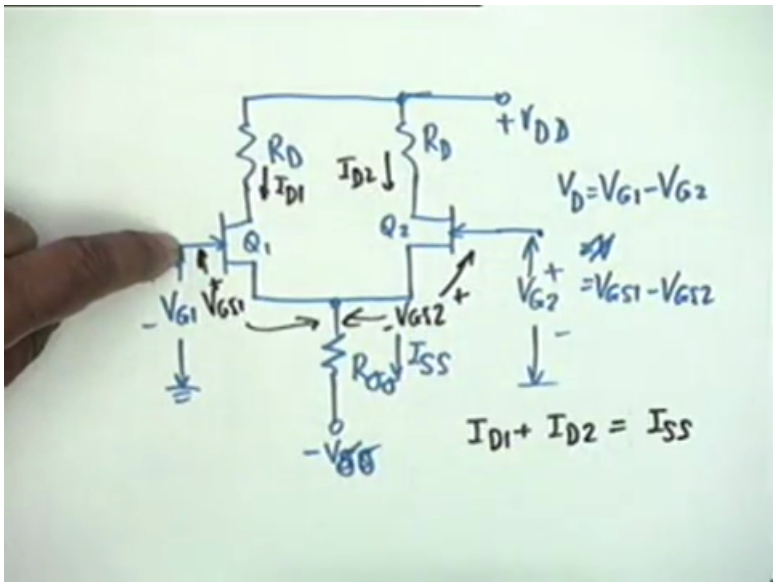

So it is the difference between the two. If I write KVL, V G 1 would be equal to V G S 1 minus V G S 2 plus V G 2 and therefore V G 1 minus V G 2 is equal to the difference between these two voltages and we obviously see that I D 1 plus I D 2, the two drain currents add up to I S S, okay. There is no gate current and therefore no assumption on beta or g m is necessary as was necessary in the case of BJT differential amplifier. Now we also know the current voltage relationship of a FET.

It is I D equal to I D S S 1 minus V G S divided by V P whole squared provided V D S is greater than V G S minus V P. And we assume that this is true. V P is obviously the pinch of voltage. And you see that I D equals to I D S S if V G S equal to zero, okay. That is if you recall the characteristics V G S equal to zero the value of the current is I D S S, okay. From this relationship we can find out V G S as equal to V P multiplied by, yes, 1. I do not want to do these algebraic steps. Yes, 1 minus I D by I D S S. No.

Student: (())(06:21)

Which one is square root?

Student: Sir I D by I D S S.

Okay, that is fine. And therefore if I substitute in the relationship for V D which is V G S 1 minus V G S 2 what I will get is V P. I am avoiding this algebraic steps, multiplied by square root of I D 2 minus square root of I D 1, okay, the whole thing divided by square root of I D S S. Is this relationship okay? Is it obvious?

Student: Yes.

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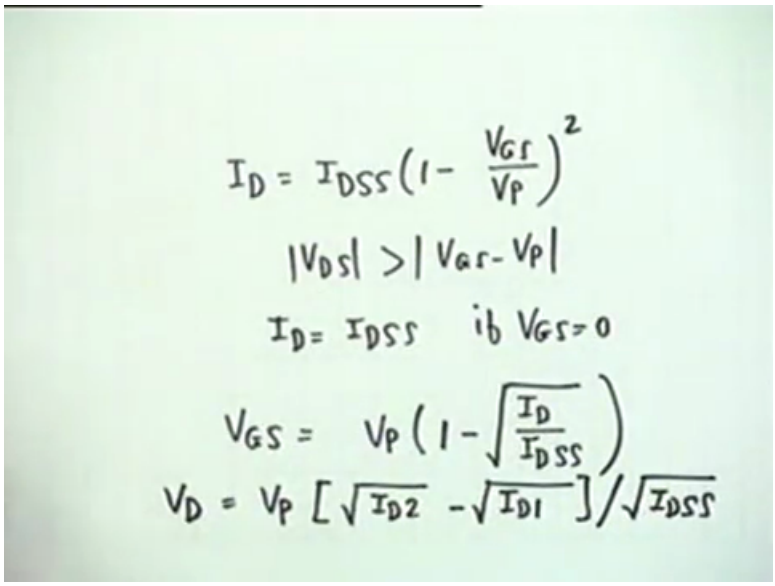

Alright, let me repeat this. V sub D equal to V P. Let me write it in a more clear fashion, multiplied by square root of I D 2 minus square root of I D 1.

Student: Sir it is an expression for V D.

V D, right, it is the expression for the input differential voltage, okay. And the other relation is I D 1 plus I D 2 is equal to I S S. These are the two relationships which when simultaneously solved will give you expressions for I D 1 and I D 2, okay. This is our aim to find out expressions for I D 1 and I D 2 in terms of V D, V P and I D S S and this algebra again I leave it to you. The values are I D 1 and 2 is equal to I S S by 2, 1 plus minus. It is not as simple as in the BJT case. It is somewhat involved.

V D by V P, distinguish between D and P, then twice I D S S divided by I S S minus V D by V P squared. Why does this square comes? Because we have squared this, okay. V D by V P squared multiplied by I D S S divided by I S S squared, curly bracket closed. To the power half and then this bracket closes. This is the expression.

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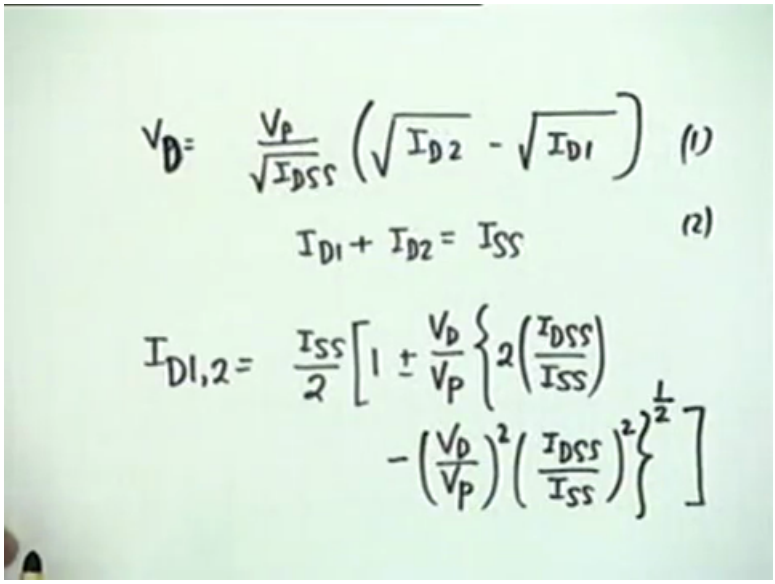

I argued to clear out this algebra and obtain this. Even though it is a horrible looking expression it turns out that if you plot I D 1 and I D 2 versus what is the variable? V D by V P then the plots are exactly similar to the plots for I C 1 and I C 2 versus V D by V T in the case of BJT. In other words one current increases, the other decreases. The plots are exactly similar. What you plot is V D by V P and you plot here I D 1 and I D 2. It turns out that these currents are very similar. I should not have drawn the, well okay.

This is zero for the current and zero for the voltage. I should have brought it here V D by V P, okay. And the two currents flow like this and the other one is like this. Exactly similar, one rises the other falls. This is I D and at V D by V P equal to zero, as you can see from this expression it is exactly I S S by 2, okay. So this current is I S S divided by 2.

The maximum is obviously I S S and we assume, you may or may not, I S S as I D S S. Then this current is exactly I S S, okay. Otherwise it will be modified by I D S S. But that is not important. What is important is that the plots are very similar, okay.

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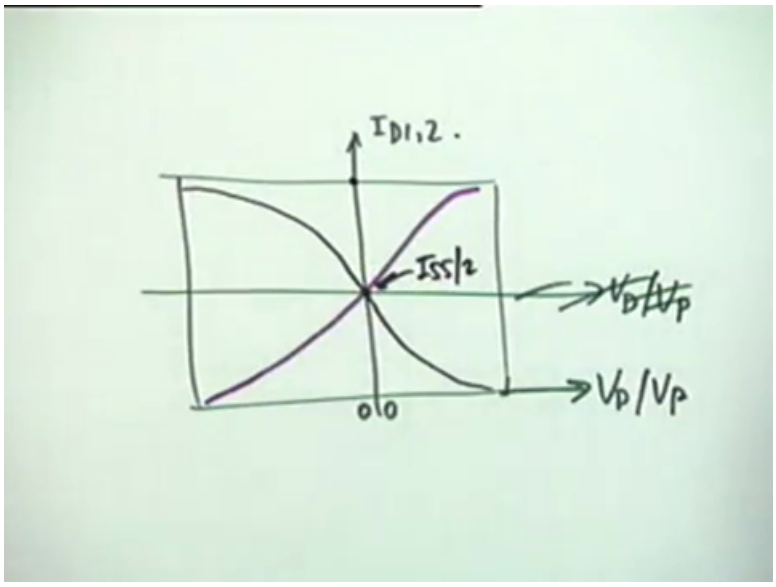

And therefore all that is said about BJT differential amplifier also applies here. In other words if I find out V O 1, no what did we say? V O D. No, first we have to find out V O 1 and 2. This should be V D D minus I sub D 1 2 times R D, okay. I was waiting for that. So my V O D is equal to V O 1 minus V O 2 which would be I D 2 minus I D 1 times R D. And it turns out , let me give you the expression by clearing the algebra.

This becomes equal to minus I S S R D V D divided by V P then within curly bracket twice I D S S divided by I S S minus V D by V P squared times I D S S divided by I S S whole squared, curly bracket closed to the power half. This is also a quiet involved expression and it is a quadratic expression.

Student: Sir, where is the bracket after 2 ending?

Oh! Yes, thank you.

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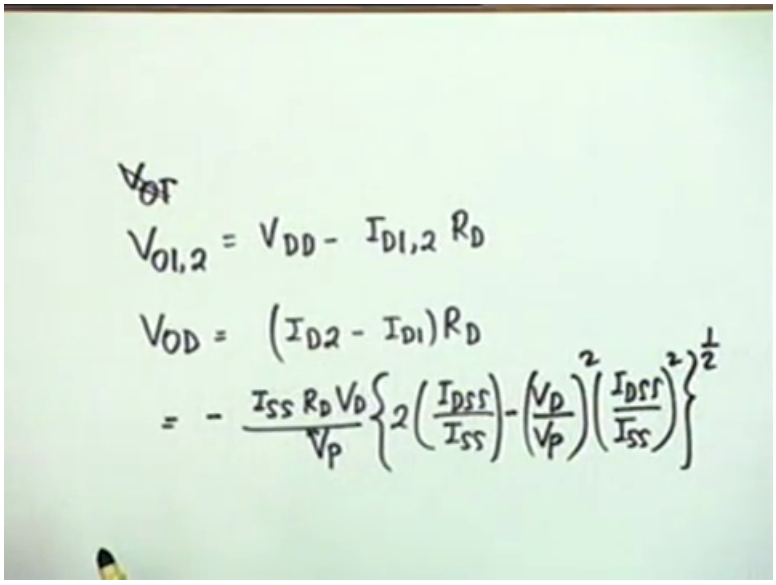

This comes from the expression for V G S 1 minus V G S 2. This comes from the same expression. The same expression is repeated here, okay. Now this is not a linear expression that is V O D does not vary linearly with V D, okay, with V D by V P because of this square expression here. It is actually a cubic. However near V D by V P equal to zero the expression is approximately linear exactly the same way as in a BJT, okay.

And if you plot V O D versus V D by V P it turns out that the situation is somewhat like this. It is very nearly linear and this voltage, can you guess what this voltage would be? No. Pardon me.

Student: I S S R D.

I S S times R D and this voltage is, in the BJT case it was I E E times R C and the other one was minus I S S times R D. And these limits of linearity, it is approximately linear, when V D by V P lies between minus point 5 and plus point 5, okay. So these are the limits of linearity of an FET amplifier. And yes, any question? Okay (ther) therefore we can find out the gain. Now how to find the gain? A sub D would be by definition V O D d divided by d V D and since this curve is approximately linear we evaluate at V D equal to zero, okay.

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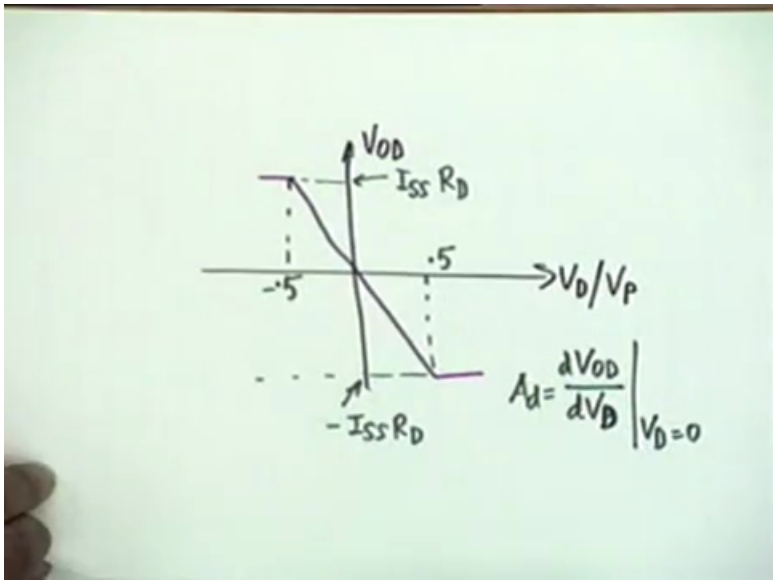

And if you do that, let us take the expression. Our expression is formidable looking expression V O D minus I S S R D V D divided by V P. Then twice I D S S divided by I S S minus V D by V P whole squared I D S S divided by I S S whole squared. I am repeating the same expression. If I differentiate this and put V D equal to zero obviously I do not have to differentiate this expression, is not it right?

You see it is V D multiplied by an expression containing V D. So it is a product of two functions. Differential coefficient of this which would be 1 multiplied by this at V D equal to zero, alright, so we will be left with only this term.

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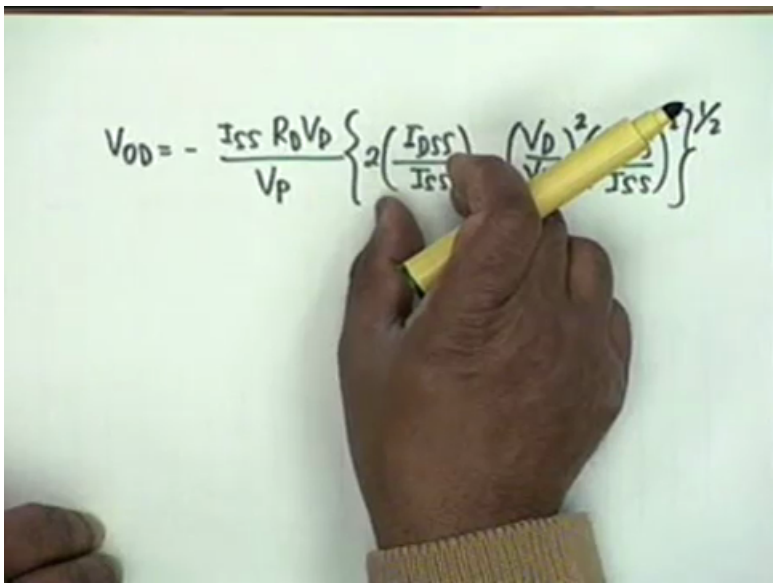

Student: Under root.

No under root. Yes it is under root, okay. That under root comes. The second term we will have V D here and since we are putting V D equal to zero we do not have to differentiate. These are tricks of the trade and you have to look at the expression and do and I can write this by inspection that is A sub d which is minus d V O D divided by d V D would be simply equal to minus I, pardon me.

Student: Why should there be a minus sign before the differentiation?

Oh! Why is there a minus sign? Because the slope is negative. Oh! I beg your pardon. A d is this, right. This is minus I S S R D.

Student: Sir there is no minus now.

Divided by V P.

Student: Sir, there is a minus.

There is a minus, okay. Where have I made a mistake? No I have not made a mistake except this one which I have corrected duly. This is minus I S S R D by V P, then square root of 2 I D S S by I S S. It comes from this expression and you see I S S occurs here. I S S also occur here so I can write this as minus R D by V P square root of twice I D S S times I S S, alright? This is the expression for the differential gain.

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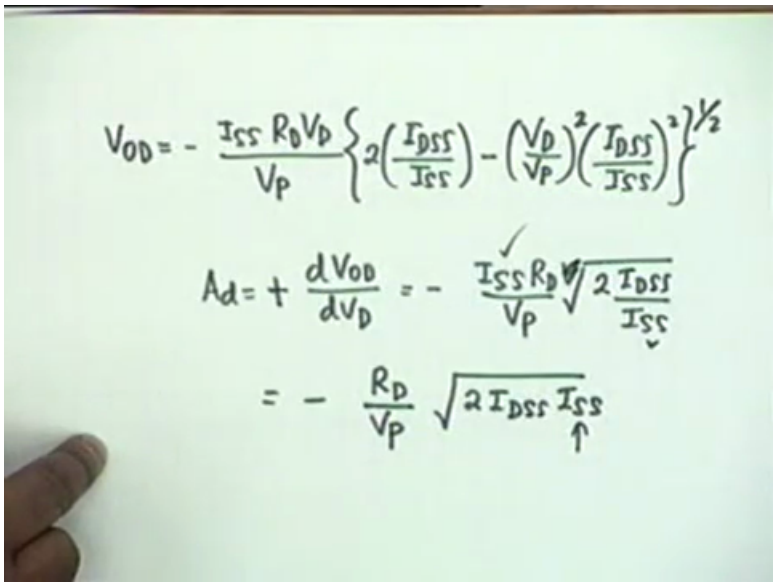

Now what is I D S S? I am sorry what is I S S? This is twice I D. Is not it right? I S S is twice I D. Both the currents are equal and therefore this 2 and 2 they come out so the expression becomes minus 2 R D by V P square root of I D S S times I D.

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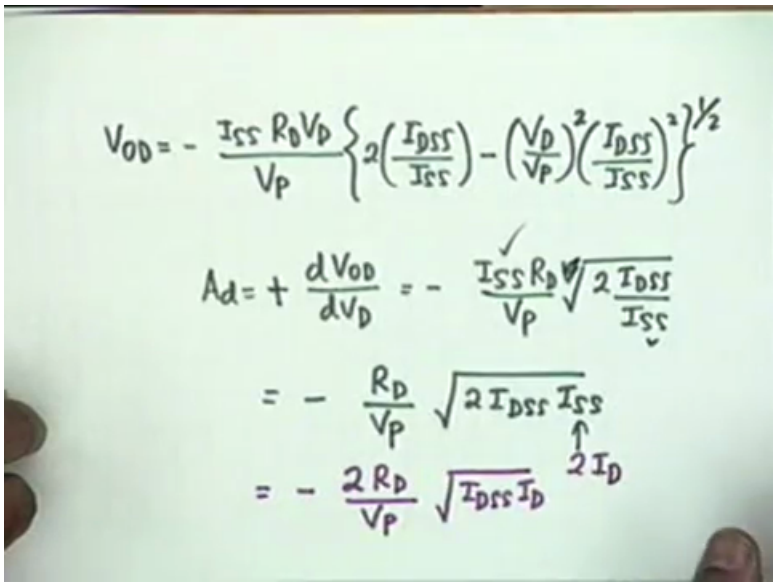

Now if you go back to the expression for current. What is current? I D equal to I D S S times 1 minus V G S by V P whole squared and find out g m. G m is d I D d V G S. You can show. We have shown this earlier. We can show that g m is simply minus 2 by V P square root of I D I D S S. Very simple, differentiate this and substitute for 1 minus V G S by V P, okay. Now if you compare this with A sub d. A sub d was twice minus R D times 2 by V P square root of I D I D S S.

Student: Excuse me sir.

Yes.

Student: Where is g m evaluated at what point?

At I D, at the Q point.

Student: Sir is there any value substituted in the (())(20:24)?

No, no value. You see if I differentiate this I get twice I D S S times this multiplied by minus 1 by V P, okay. And then this quantity 1 minus V G S by V P, I replaced by square root of I D by I D S S. That is how I get this expression, okay. And therefore you see that this is minus g m R D. I claimed yesterday that this could be the case. This is indeed the case. The rest of the

analysis as you must have guessed except for this nonlinear voltage current transfer relationship.

Student: (())(21:09)

G m is positive.

Student: G m is negative.

Pardon me.

Student: G m is negative sir.

G m would be negative, yes that is correct.

Student: No sir g m would be positive.

Student: What is the significance of negative conductor?

Student: Sir V P is negative.

So?

Student: So it will come out as positive.

Student: Sir, g m becomes positive.

In the expression, this expression is correct.

Student: Yes sir. (())(21:59)

One at a time. What is the question? This should be plus. No, I have made a mistake about the sign previously somewhere else. Maybe in V O D. Somewhere I have made a mistake about the sign. Anyway you clear this out. This is correct, this minus sign is correct, okay, minus g m R D. Now what was the question? What is the significance?

Student: Sir, how can the conductor be negative? G m is negative.

G m is not negative. You see V P is negative so g m is positive. But g m can be negative. You should not worry about g m being negative. What does that imply?

Student: Sir, current is not there.

No, okay. You see it is not the current and voltage across one port, across the same terminal, it is a transfer relationship. So all that it means in the current direction is (())(23:06). But here g m is not negative, it is positive.

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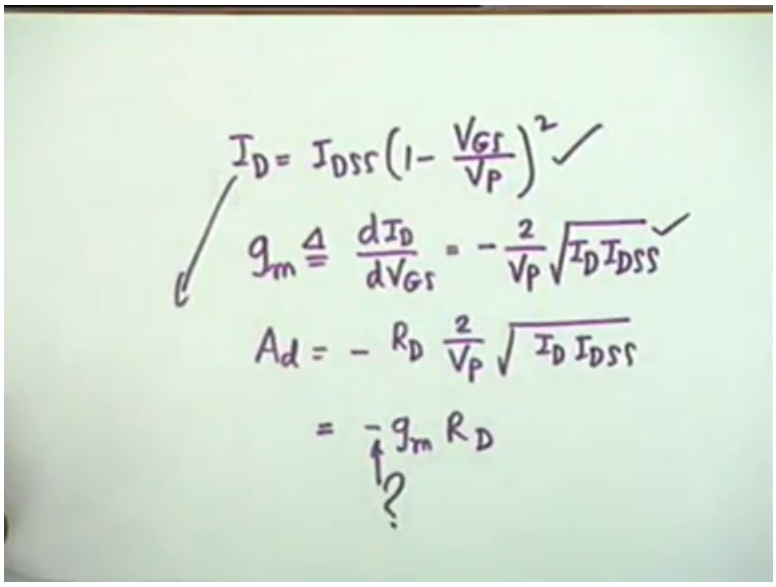

I have made a mistake previously with regards to the sign of V O D. That is right. V O D should have been positive and that is how this has come out wrong . This expression is correct. On this page whatever I have written is correct, okay. Please do correct the previous sign. Now I could have continued with the analysis of BJT differential amplifier but since the results are absolutely identical I would not repeat that. As I said we will illustrate with the help of a couple of examples in the problem session.

Now it is time to go to power amplifiers. So far we have talked only about small signal amplifiers. Small signal amplifiers basically are voltage amplifiers or current amplifiers and we found out voltage gain, current gain, input resistance, output resistance, in the case of differential amplifier, common mode gain, differential mode gain, the C M R R and things like that because nowhere did we ever mention the question of power.

Now it is time because amplifiers have to deliver power, a stereo for example. The usual wattage that you get in the market which is also very harsh to hear in a room like this is 30 watts. There are stereos available with 200 watts or more than that, even more than that, okay. I do not know what people do with them but if you want music well 200 watt is not the power. But anyway since that is the market force and we are being driven by market forces we should know how to design large signal amplifiers.

Even 30 watts is a large signal and you have to make very careful designs. Now power amplifiers basically we shall consider two kinds, one is for integrated circuit application and the other is for discrete circuit application. Obviously if we use a loudspeaker and the transformer with 200 watts, obviously IC is not the answer. IC power amplifiers deliver basically powers of the order of milliwatts, maximum of 2 watts. What is the limitation? Limitation is power dissipation.

If you want to deliver a large power you also have to be prepared to dissipate large power and ICs cannot dissipate large power unless you put a small fan inside or some other cooling device, okay. There are cooling devices at gigahertz range for example, you have to pass chilled water, okay. And there are special silicon tunnels dugged through it by integrated circuit technology to cool the device. But we are not going to that. We will consider powers of the order milliwatts in IC power amplifiers.

And in discrete power amplifiers watts ranging to, let us say maximum about 200 watts, alright. We shall consider both of these types of amplifiers but since we have started our previous discussion with differential amplifier which forms a part of an operational amplifier or input stage of almost any integrated circuit be it a phase detector or a phase lock loop whatever it is, differential amplifier.

Let us continue with this. Let us first discuss what should be the output stage of a typical, let us say integrated circuit analog integrated circuit like an (())(27:08). Therefore we first consider IC power amplifiers. And the emphasis on IC power amplifiers is as little power dissipation as possible, as few resistances as possible, as small resistances as possible, number of transistors no constrain. You can use almost any number, okay.

Now in integrated circuit power amplifiers the output load resistance would be of the order of let us say 100 ohms to maybe 1 K. Power amplifier maybe to drive a small motor or to drive something else. Maybe to light a lamp, an indicator and things like that, power amplifier is needed.

On the other hand if you go for large power than the usual application is a loudspeaker and therefore the output resistance, the load resistance shall range from 4 ohms to about 16 ohms, okay. Four speakers in series or two 8 ohm speakers in series. This is the usual range of load.

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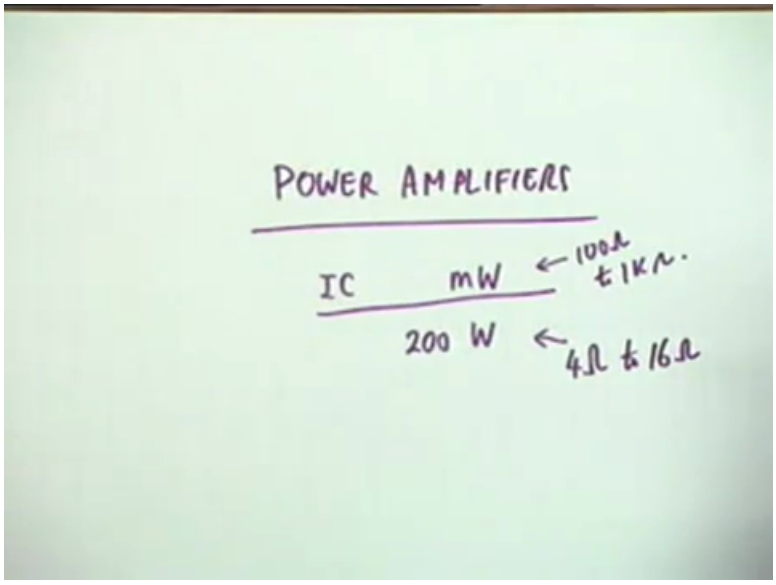

Obviously if you want power and if you like to drive large currents to the load, okay, large current which means that the voltage peak to peak swing should be as large as possible. And if you refer to the usual load line obviously the swing cannot exceed V C C, the power supply, alright.

And if you want distortion less power amplification with a single device then obviously your Q point has to be somewhere in the middle of the load line so that the swing on this side is V C C and the swing on this side is zero but it cannot be exactly zero, it must be limited to point 2. That is V C E sat. If we go beyond that then there will be distortion. Now obviously with such large voltage swing that would be distortion. Distortion would be affect of life but we do not want it, okay. We do not want distortion.

Therefore we shall limit our operation to as little distortion as possible. Whereas with a voltage amplifier, distortion is banned. We do not want any distortion, will make careful designs so that the signal is indeed small compared to the value of the Q point. The signal would be limited to let us say this range. On the other hand for a power amplifier we go to larger ranges.

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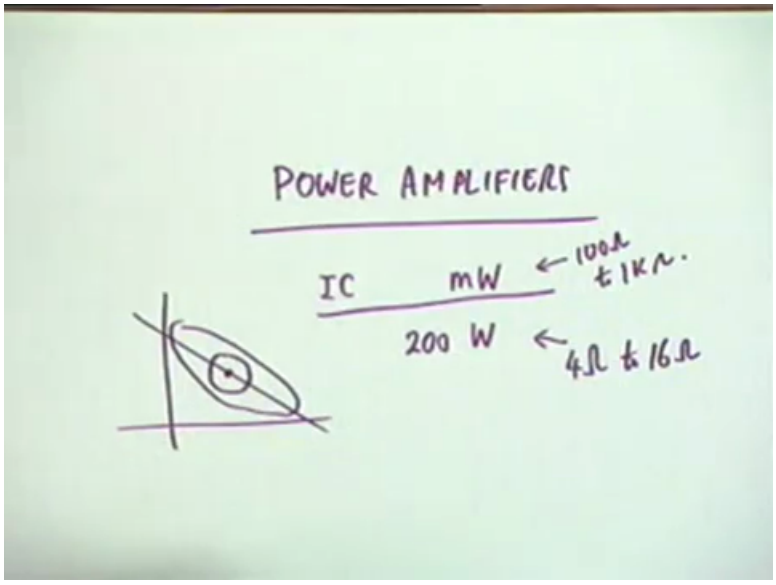

Even if we do not touch cut off and do not touch V C E sat, there is distortion because the characteristics are not absolutely parallel to each other and there are small bends here, there are small bands here also when you go to large voltages because it goes towards breakdown, okay. So in large signal amplifiers distortion will be there as compared to small signal amplifiers.

And we shall have to design the circuit so as to minimise this. We can only minimise this, we cannot make it equal to zero. In integrated circuit power amplifiers obviously the swing can exceed V C C. There are two supplies V C C and minus V E E and therefore the effective supply is V C C plus V E E and the effective swing can go to V C C plus V E E.

This is a small difference but that is not of much concern. Now we go back to the load line. If the Q point is somewhere here and the signal is such that the operation does not shift beyond the cut off or beyond the saturation line, obviously current will flow in the device for the whole cycle of the input.

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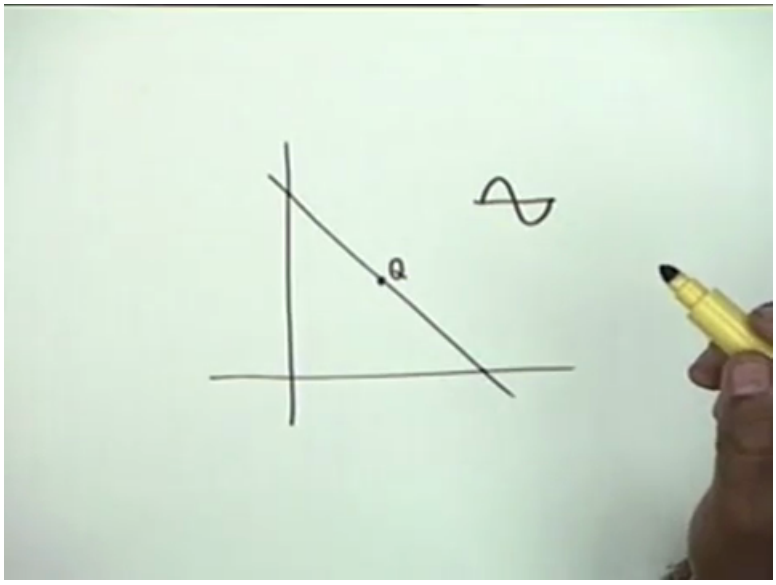

We take the input as sinusoidal, okay. Take the input as then sinusoidal throughout if this input is plotted versus theta then theta equal to 360 degrees. That is during the total swing of the input, the output current shall flow, okay. If the current flows in the device there are operating points where the current will not flow for the total cycle, okay. If the current flows for the whole cycle then you call it a class A operation. These are historical names, class A.

On the other hand if the Q point is here at the cut off point that is at the quotient condition no current flows in the collectors of the device then this is called a class B operation. Obviously in class B the conduction angle theta is 180 degrees. It is only for one cycle, okay. Depending on whether it is a phase change or not it is only one cycle of the input that the current will flow in the device.

Obviously if we want the device to make distortion less power amplification obviously we require two devices. One will conduct during the positive half and the other will conduct in the negative half and we shall have to combine them in some manner. We have to combine them in some manner so that the output looks like the input, okay.

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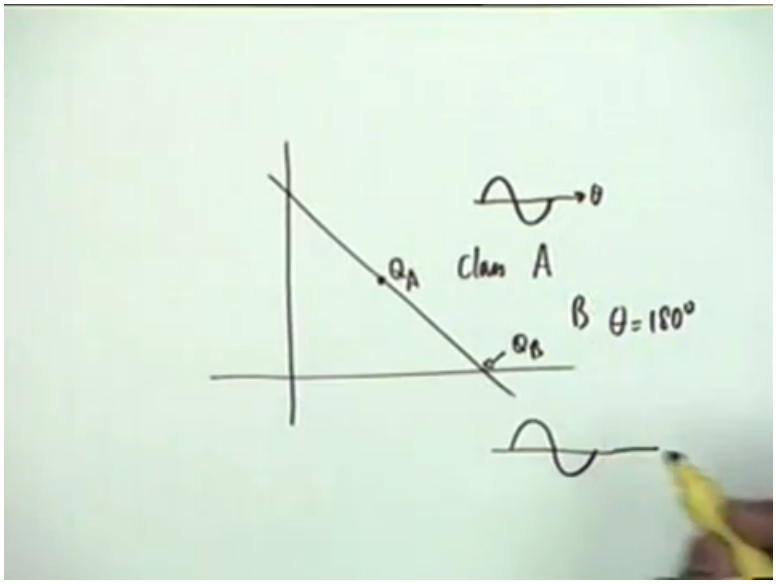

If it is simply one cycle then obvious halfway rectifier rather than an amplifier. But it is our purpose to amplify this and to be able to deliver large amount of power to the load and well class B where the conduction angle for each device is 180 degrees that is half of the cycle, either the positive half or the negative half, there are two devices needed and historically these type of operation using two devices is known as a push pull operation. One pushes the other pulls, okay.

There is no other significance of this term. This was coined by one of our forefathers and we have stayed with it, okay, just like your father gave you a name without an affidavit you cannot change it. Even that is not very desirable, it is not very ethical. That is questionable. But now suppose the Q point is now somewhere here beyond cut off then obviously the conduction angle would be less than 180.

That is only during part of a half cycle the device will come back and obviously there will be heavy distortion, okay. Maybe the device conducts only for this part and the output current swing shall be like this. This is the input, the output current swing will be like this.

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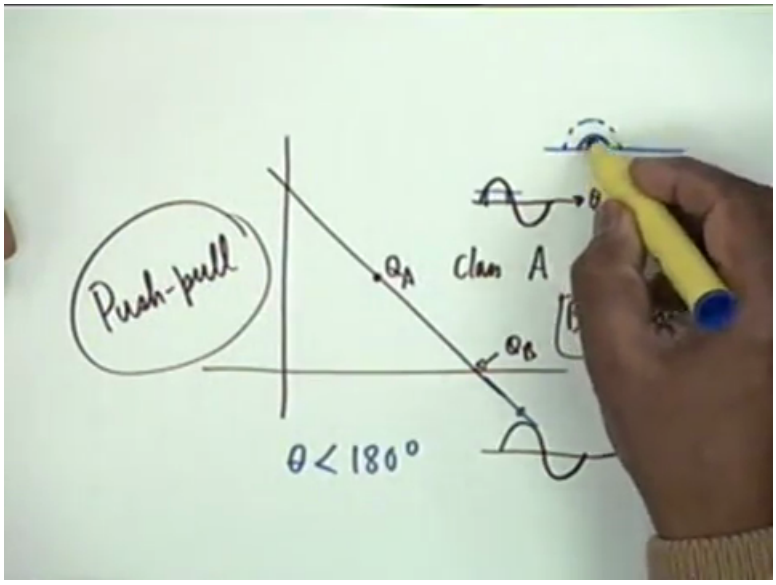

Output current will flow only for part of a half cycle and obviously you shall have a heavy distortion. Now this type of operation is called class C operation despite the fact that it introduces heavy distortion is also used. In fact in large power applications at radio frequency this is important point. Frequencies must be high enough. At radio frequencies class C operation has to be distorted to.

The amplitude modulated transmitter, the radio transmitters use class C power amplification because of high efficiency. Larger the power, larger will be the power dissipation also and therefore if the devices do not normally conduct and they conduct for as short a time as possible, the power dissipation will also be small, okay. And therefore class C operation is used in radio frequencies and the distortion that originates from there is avoided by using instead of the usual resistive load, a tune circuit in the collector.

And the output is taken from here. The tune circuit has the property that it is a band pass filter. That is if the Q is very high then the tune circuit response will be something like this.

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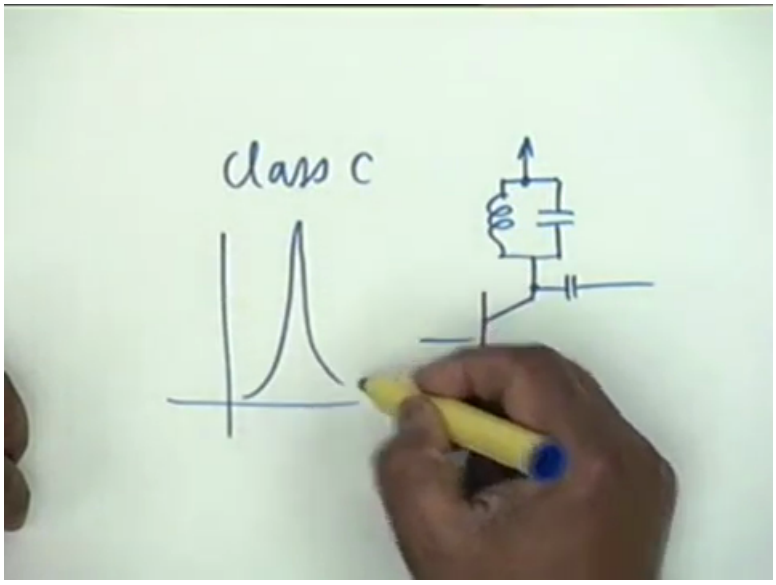

So it is only a band of frequencies around the centre frequency which would be amplified by this amplifier, okay. You see a current swing like this, when it passes through the tune circuit, the tune circuit offers an easy pass to frequencies beyond the centre frequency. And to centre frequency it offers a high resistance which means that the voltage developed here, excuse me, would be mainly of a frequency that we want.

It is because tune circuits can be used that class C amplifier can be used, not otherwise, is the point clear? The effective load here is very small, approximately zero for frequencies other than the tune frequency, other than the resonant frequency. Yes?

Student: (())(37:56)

Load is very high for the resonance frequency. For the frequency at which that is omega 0 is 1 over square root L C, what is the impedance of this? Infinity. Unfortunately no inductance can be made without a resistance and therefore it is 1 by R square root L by C. This is impedance. So at the resonance frequency the impedance is very high and the gain is minus g m times effective load.

Effective load is very high for that particular frequency and any such currents swing can only be decomposed into the fully A series of which the fundamental will be the one which you want to amplify, okay. So with the help of a tune circuit class C power amplifier operation is possible with minimal amount of distortion and this is the standard practice in any radio transmitter, in any large power amplification at radio frequencies this is the standard practice.

Class C operation is somewhat beyond the scope of this analog electronics class but if time permits we will have a look at it at a much later point. The usual power amplifier that is used in integrated circuit is class B because of its high efficiency, class B. Where does the efficiency arise from? Because under quotient condition there is no current. I sub C is equal to zero and therefore there is no dissipation at the Q point.

The point Q is at the cut off point approximately and the circuit I had already given this circuit in one of the tutorial sheets. This simple circuit for a class B power amplifier using integrated circuits is this. That we have two transistors, one NPN and the other PNP in a complementary symmetry. That is Q 1 and Q 2 are otherwise identical, alright.

And the collector current of Q 1 flows through Q 2 normally if it is class A operation. But in class B the node is connected here and since it is an integrated circuit we should not use any capacitor. So the node is connected directly to the common emitter point.

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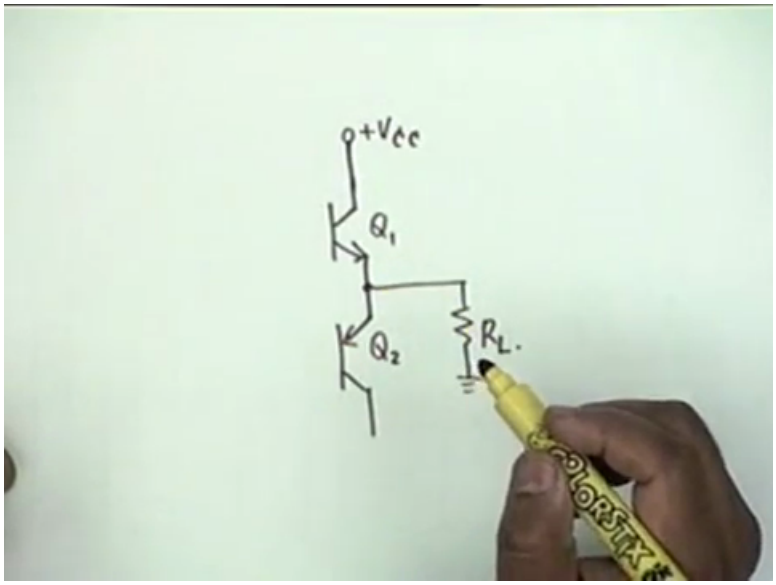

The two emitters are connected together. Shall we call it emitter coupled? No, in a differential amplifier we call it emitter coupled because we will see that there is no coupling. When Q 1 conducts Q 2 is off. So Q 1 current does not go through Q 2, okay. This is R L and the input, two bases are connected. The input signal is also applied directly while this goes to minus V C C. The two voltages have to be identical now. We do not have a choice.

The two supplies have to be identical in order that distortion less operation is possible. The input we cannot apply for a capacitor for integrated circuit and therefore the input is applied

directly here. We assume that the input is sinusoidal then we shall see what kind of distortion arises.

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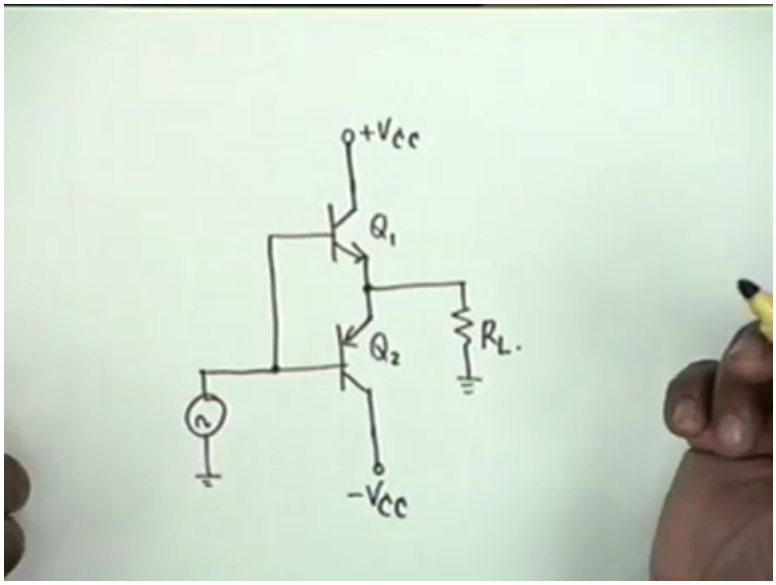

Now there is a deviation from the usual practice of notations. In small signal amplifiers we could work in terms of phases.

Student: Sir you said that input cannot be applied through a capacitor.

Yes, because I am talking of an integrated circuit power amplifier IC.

Student: But still the input you are providing from outside.

Input we are providing from outside, okay, we will not use a capacitor. That will reduce the cost and if you use an external capacitor well that is a large capacitor. It may be 50 times the size of the I C chip. But space is a problem. You want to send this in a satellite. You cannot use it, capacitor. Not only it is ugly looking but we do not mind to use it but the space, the volume that it is occupying. I can pack in much more because every milligram put into a satellite counts, the load. It is called the payload as it is called, okay.

So we do not use a capacitor. Now as I said there would be a deviation from the standard practice of nomenclature. As I said in small signal amplifiers we use the phases. So use capital V subscript small i, capital V subscript small o. Now since we have to be concerned with distortion we must follow the output signal point to point and therefore we must bring back the time.

And so we say our input is small V i t and the output is small V o t, okay. We go back to the time domain. No longer the Fraser, no longer the Laplace domain, we go back to the time domain. In the large signal case it has to be done because otherwise we will miss that time exploration of the signal, okay, how the signal changes with time. And we will use this notation that V i t is equal to capital V i m, the maximum value, let us say sin of omega t and often we will replace omega t by theta.

The output signal similarly if it is sinusoidal, okay, there is a big if, we shall call this V o m sin of, not necessarily omega t, there can be a phase change, so sign of omega t plus let us say some phase phi. This should be our notation, okay

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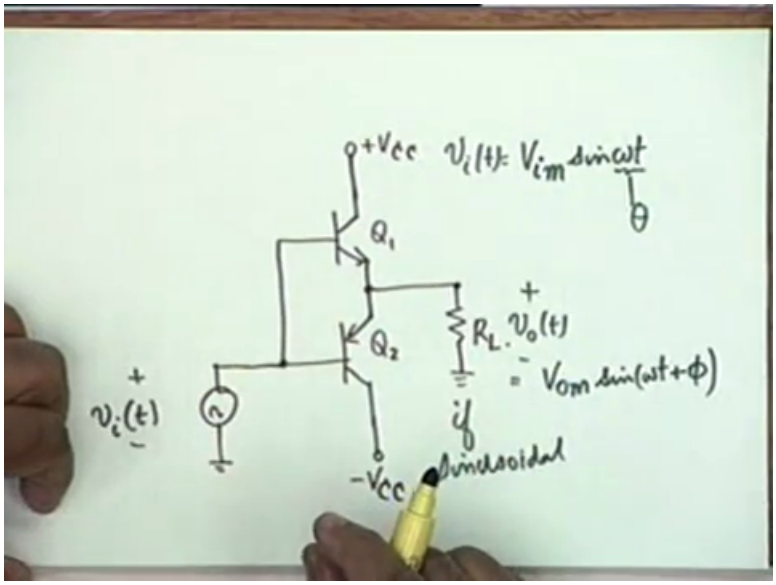

Now let us look at the operation of the circuit. The two transistors as I said are perfectly matched, okay. When V i t is 0 both Q 1 and Q 2 shall be off. When V i t is 0 both Q 1 and Q 2 shall be off because there is a voltage. For Q 1 to conduct this voltage must be V B E on, okay. And for this transistor to conduct this voltage V B E must be greater than.

Student: (())(45:36)

So instead of talking about V B E we will talk about V E B for transistor Q 2. We have to have (())(45:46) now. V E B 2, which will be a positive quantity. V E B 2 has to be greater than V E B 2 on which is approximately point 5 volt, okay. Therefore when V i is 0 there is no question of conduction of Q 1 and Q 2 both are off. When V i increases and touches the value of V B E on, when V i increases in a positive direction and gets the value V B E on, Q 1 starts conducting.

And when Q 1 conducts Q 2 obviously must be off. So the current that comes from here I C 1 let us say I am using this as the total current but you know under quotient conditions the current is 0 and therefore this is also the signal current, alright. I C 1 comes here, Q 2 blocked so it does not find the path here. It has to flow through R L, alright. Is that clear? Okay.

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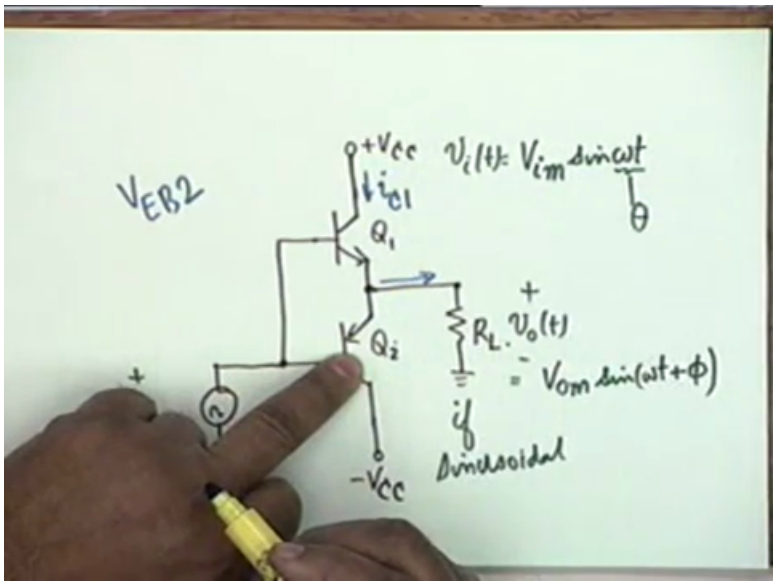

You also notice that when V i t is positive and greater than V B E on, the transistor Q 1 acts as a emitter follower, is not it right? There is no load here. The load is at the emitter and therefore this is an emitter follower and therefore the voltage, let me put this, V i t greater than V B E on. V i t would be equal to V B E 1 plus V 0 t, is it clear? The output shall therefore be less than the input by this amount V B E 1. When it goes into the active region V B E 1 will exceed point 5, it may go right up to point 7.

In order not to confuse the main issue we will assume that V B E 1 on and active are the same, approximately point 7. If it is not you can take care of it, okay, to simplify the analysis, alright. Now what can be the maximum V 0? Pardon me. Maximum V 0, I am increasing V i so that V 0 can be increased. But what can be the maximum?

Student: V i max minus point 7.

That again depends on V i. Suppose V i is unrestricted.

Student: Sir V C C (())(48:46)

That is correct. The maximum value can be V C C minus V C E sat. Under this condition when the maximum is reached what is the input maximum? V C C minus V C E sat plus V B E 1, agreed? Under this input the output can reach (())(49:22), agreed?

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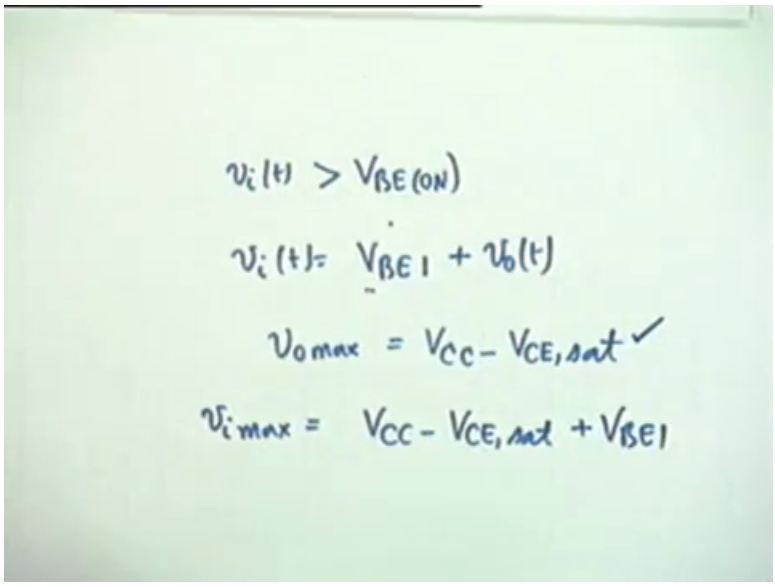

Now what is this value? This is greater than V C C or less than V C C.

Student: Greater.

Greater than V C C and V C C usually is plus minus 15. We hardly ever require a 15 volt signal at the input and therefore V i max (())(49:44) to a value less than V C C. In other words the transistor Q 1 should not be allowed to go into saturation, is the point clear? Okay. Theoretically our maximum output is V C C minus V C E sat. That is the transistor Q 1 has been allowed to go into saturation. But you know in the saturation region there are distortions and therefore we do not allow it to go there.

And this is logical because this voltage shall be reached when the input reaches its maximum possible value. That is V C C minus V C E sat plus V B E 1 which because V C E sat is of the order point 2 and V B E is of the order point 7 is greater than V C C. The practical situation is hardly ever we shall require an input signal which exceeds the V C C. Where is the input signal derived from? For a power amplifier where is the input signal derived from?

Student: Preamplifier.

From a preamplifier which is a voltage amplifier. And in a voltage amplifier we do not allow the output swing to go right up to V C C and therefore it does not arise in practice. Even if it

arises in practice we shall limit it. Why shall we limit it? Because it will cause distortion, okay. Now if this point is clear then one should be able to guess what the characteristics would be if I plot V 0 versus V i when V i is positive. You see V i does not conduct till a value of point 7. Q 1 does not conduct till V i reaches a value of point 7.

When V i exceeds point 7 what is the relationship? The relationship is this, V i is equal to V 0 plus V B E 1. V B E 1 is a constant therefore the slope of V 0 versus V i curve shall be unity, okay. Therefore it rises like this.

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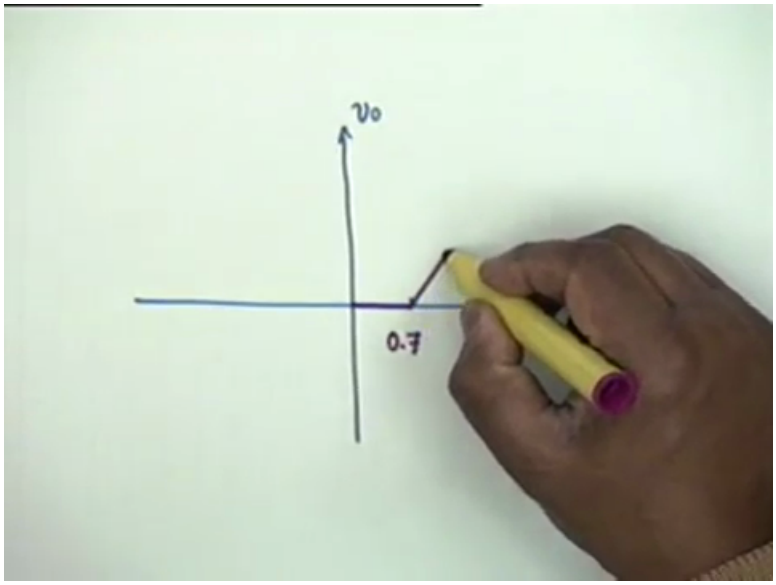

Now how long can it rise? The maximum obviously shall be reached here. This is V C C minus V C E sat, okay. And at what value is this reached? This is reached at V C C minus V C E sat plus point 7. I am taking the numerical value, okay, is the point clear? The transfer characteristic.

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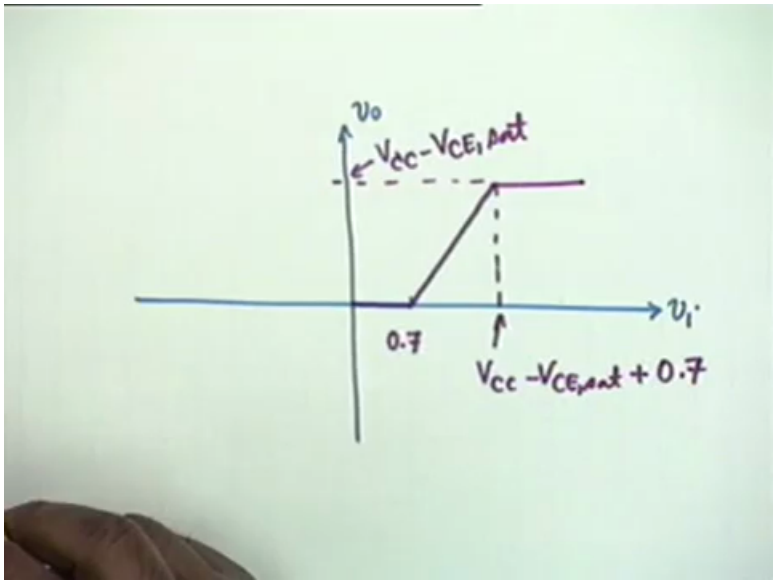

Student: Sir what if we take point 8?

You do not we take it. You take point 8. I do not mind. I have taken point 7 as a typical numerical value . I could have taken point 5 also but the phenomenon is independent on what you take. The phenomenon that occurs which you will see now. Now I go back to this circuit. If V i t now becomes negative, okay, if V i t decreases to a negative value then obviously Q 1 cannot be on, Q 1 shall be off and when V E B 2 on exceeds because we have taken it to be a positive value, alright.

When this exceeds point 7 then Q 2 conducts and Q 2 conducts like this. The current now flows from here via this to the negative V C C and this is why this is to be identical to plus V C C because Q 2 conduction and Q 1 conduction must be absolutely symmetrical. Any asymmetry will cause a distortion, okay. So it conducts like this and you see V 0 t will also be negative now because the current is flowing like this, okay.

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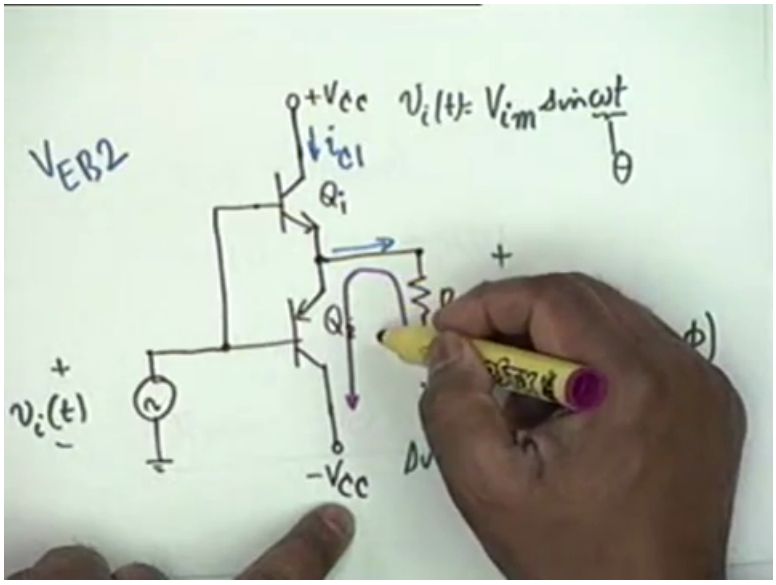

And the relationships are exactly similar. That is the slope shall again be 1. In other words the characteristic if I draw it on the other side it would be minus point 7 and then it will go like this and saturate at, can you tell me what this value would be?

Student: Minus V C C.

Minus V C C.

Student: Plus V C E.

Plus V C E .

Student: Sir minus V E C.

V E C sat, thank you. V E C sat, that would be a positive value, then minus point 7.

Student: Not minus point 7.

Student: Sir no minus point 7.

Oh! That is (())(55:01), agreed. So it can reach only this.

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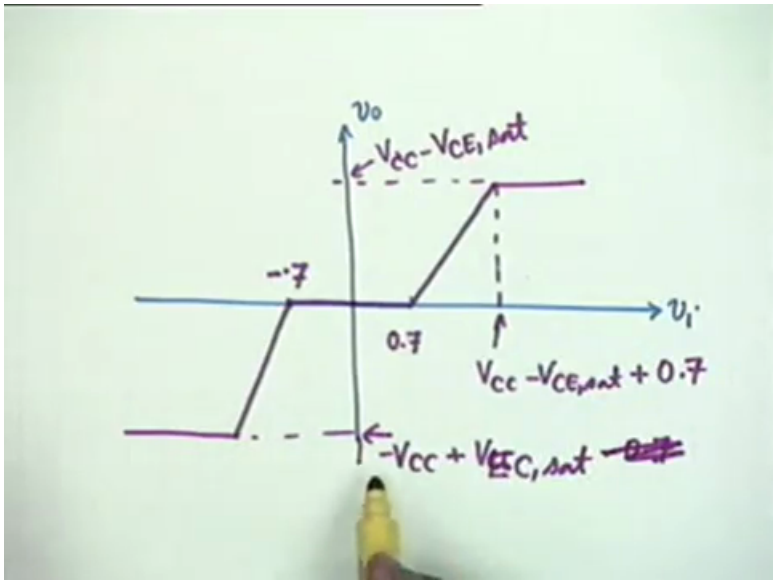

Then the input under this condition would be minus V C C then.

Student: Plus V E C.

Plus V E C sat minus point 7, okay. Yes?

Student: Is this characteristic independent of beta of the transistor?

Is this characteristic independent of beta of the transistor? Yes, it is independent beta of the transistor because in an emitter follower we have written the emitter follower relationship. So between V 0 and V i we have not considered. It is independent of r pie, independent of g m, it is independent to everything.

Student: Sir, can we use different transistor?

Pardon me. If you use different transistor then you are in a mess. We will not use different transistor, okay. Now what I want to point out to you is the following that there is a region in the transfer characteristic which is a dead band, there is no response. If V sub i lies between minus point 7 and plus point 7 there is no response. It is only after that that the output voltage follows the input voltage. This is called a dead band. Dead band is approximately of width 1 point 4 volt.

Now what it means is that if the input voltage lies between minus point 7 and plus point 7 no current flows either in Q 1 or in Q 2. Which means that if my input voltage is like this then I draw a point 7 line and a minus point 7 line the output current shall flow only from here to here and from here to here, okay.

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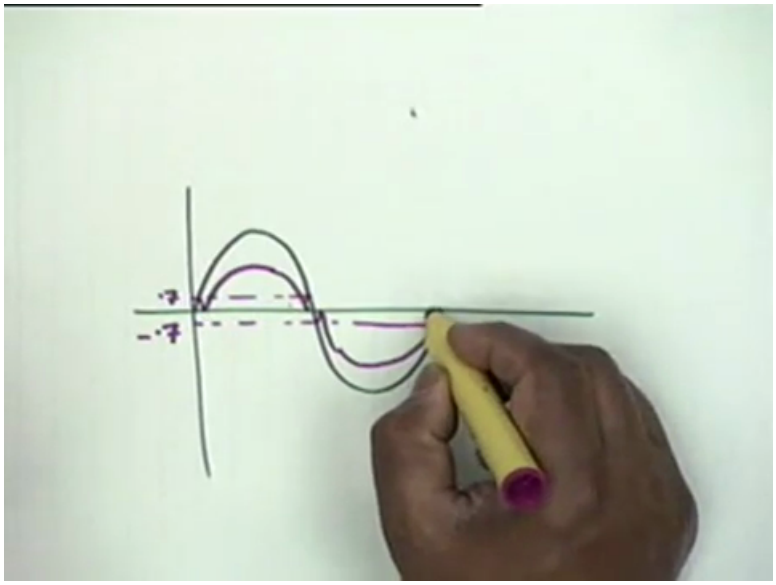

At this crossover region when the input voltage crosses from positive to negative, no current flows. So the current waveform if I draw it independently it will.

Student: Sir what are the labels for the X and Y axis?

Oh! This is V i or current versus time.

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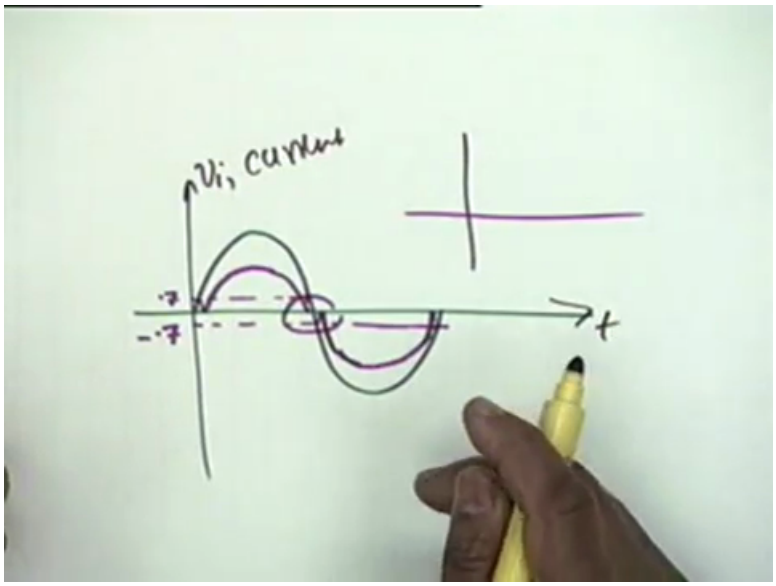

Student: Sir, is this similar to class C operation?

Quiet so. This is similar to class C operation. There is a band that is the input current waveform will now look like. This is the current waveform by Q 1 and by Q 2. The current

due to Q 1, current due to Q 2. The load current, the current that flows in the load will look like this, waveform. Obviously this waveform is a very distorted as compared to the input waveform and this distortion occurs when input voltage crosses over from a positive value to a negative value. So this distortion is known as a crossover distortion, okay.

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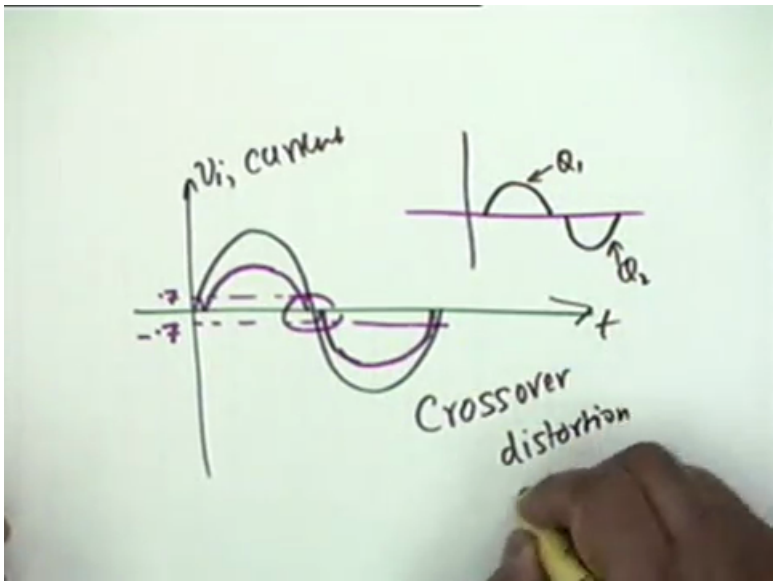

And one of the obvious ways to get over crossover distortion is to change the Q point. If we maintain Q 1 V B E 1 at point 7 and V E B 2 also at point 7 then this distortion shall not occur. It is also true that the crossover distortion, how do you think it will depend on the amplitude of V i? If V i increases will the crossover distortion increase or decrease?

Student: Decrease.

It will decrease. We shall show it next time.